SYNOPSYS®

DATASHEET

# Avalon

## CAD Navigation and Debug Solutions for Failure Analysis

## Overview

Avalon software system is the next-generation CAD navigation standard for failure analysis, design debug and low-yield analysis. Avalon is a power packed product with tools, features, options and networking capability that provides a complete system for fast, efficient and accurate investigation of inspection, test and analysis jobs. Avalon optimizes the equipment and personnel resources of design and semiconductor failure analysis (FA) labs by providing an easy-to-use software interface and navigation capabilities for almost every type of test and analytical failure analysis equipment.

Avalon enables closer collaboration of product and design groups with FA labs, dramatically improving time to yield and market. Avalon can import CAD design data from all key design tools and several user-proprietary formats while providing visual representations of circuits that can be annotated, exploded, searched and linked with ease.

## Benefits

- Improves failure analysis productivity through a common software platform for various FA equipment
- Significantly decreases time to market with reduced FA cycle time
- Faster problem solving by cross-mapping between device nodes to view all three design domains (layout, netlist and schematic) simultaneously
- Increases accuracy of FA root cause analysis using advanced debug tools
- Single application that overlays images from various FA equipment on to design layout
- Secure access to all FA information using KDB™ database
- Design independent system that supports all major layout versus schematic (LVS)
- Complete access to all debug tools critical to failure trace, circuit debug and killer defect source analysis
- Simple deployment setup with support for Linux and Windows
- Seamless integration with legacy Camelot™ and Merlin™ databases
- Ease of conversion for layout, netlist and schematic data and establishes cross-mapping links between each data entity

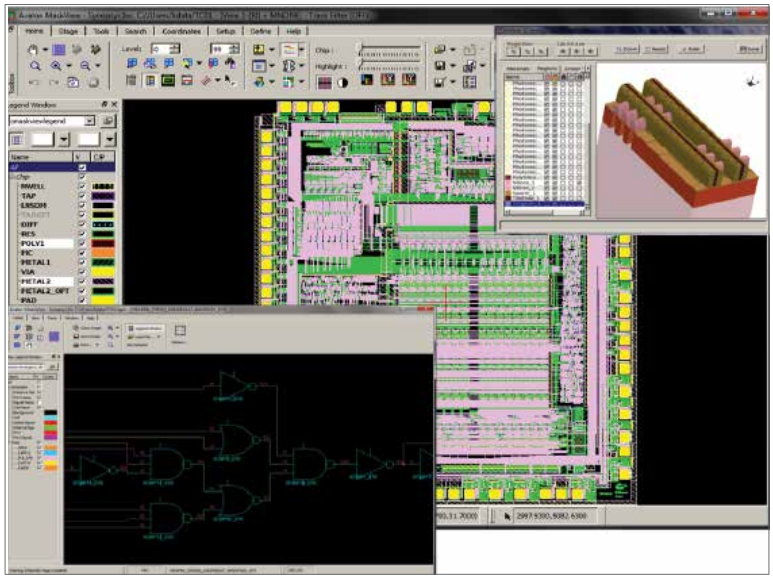

Figure 1: Avalon CAD-navigation system integrating layout, signal tracing and 3D view

## Supporting all CAD Design Data

Synopsys is committed to being the leading provider of software solutions that links all CAD design data. Avalon is a comprehensive package that reads all EDA tools and design data from verification systems and several user-proprietary formats. The KDB™database is designed to interface with all key design formats.

Today, there are more EDA developers and more verification package choices; Synopsys is the only company that supports all of them.

- LVS Conversions: Cadence (Assura, DIVA), Mentor Graphics (CheckMate, Calibre), Synopsys (Hercules, ICV)
- Netlist Conversion: SPICE, EDIF, OpenAccess
- Layout Conversion: GDSII, OASIS®

The highest priorities for Avalon users are faster data accessibility, support diverse failure analysis equipment and availability of debug tools. Avalon provides the optimal solution for both small and continually-expanding FA labs and design debug teams. The Avalon database is design independent and offers a superior level of data consistency and security. The unique design of the internal database schema guarantees compatibility with decades-old databases. This is an indispensable feature for all failure analysis, QA and manufacturing organizations especially in the automotive industry.

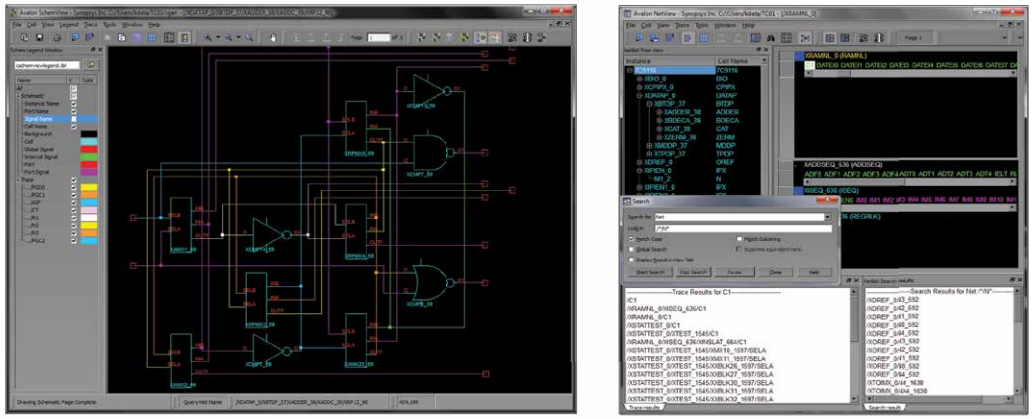

Figure 2: Avalon SchemView and NetView provide an easy way to navigate inside circuit schematics

## Providing Critical Analysis Functions

In addition to its CAD navigation and database capabilities, Avalon's analysis features have become indispensable to the FA lab. Different viewing options are critical in tracking potential failures and determining the source and origin of killer defects. Avalon includes special schematic capabilities and layout features that are invaluable to FA engineers as they debug chips manufactured using new processes.

Avalon View Only Client consists of maskview, netview, schemview, i-schemview, K-EDIT, defect wafermap and 3D-SAA. The list below details some of the most commonly used applications.

**Defect Wafer Map** integrates defect inspection data with the device CAD design using the defect coordinates to navigate an equipment stage and pinpoint the defect for closer inspection and characterization. Avalon sorts defects by size, location or class, as well as layout location and allows the user to define custom wafer maps. Additionally, users can classify defects, attach images and write updated information to the defect files.

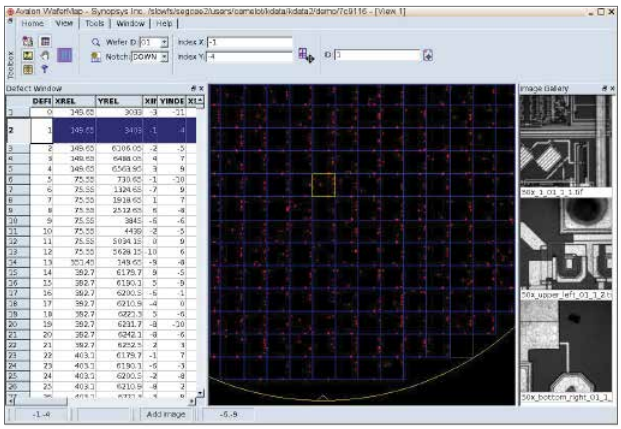

Figure 3: Defect Wafer Map pinpoints defects for closer inspection

**SchemView** provides tracking of potential failures through visualization of the chip logic. Cross-mapping of nets and instances to the device layout and netlist, SchemView helps determine the source and origin of chip failures. SchemView helps determine the source and origin of chip failures. The entire design is displayed in cell hierarchy format, allowing push-down to a transistor level.

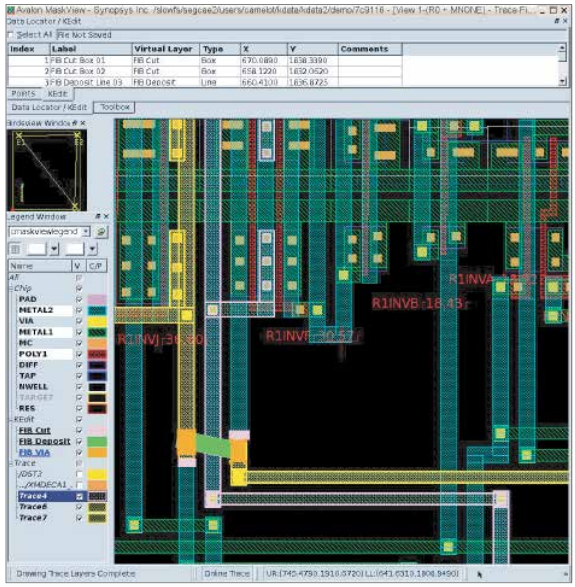

Figure 4: K-Edit allows collaboration between design, fab and lab

**I-Schem (Interactive Schematic)** creates a schematic from a netlist in a net-oriented format allowing forward and backward tracking to locate a fault. Features like Add Driver or Add Input Cone allow for quick analysis and verification of diagnostic results in scan chains.

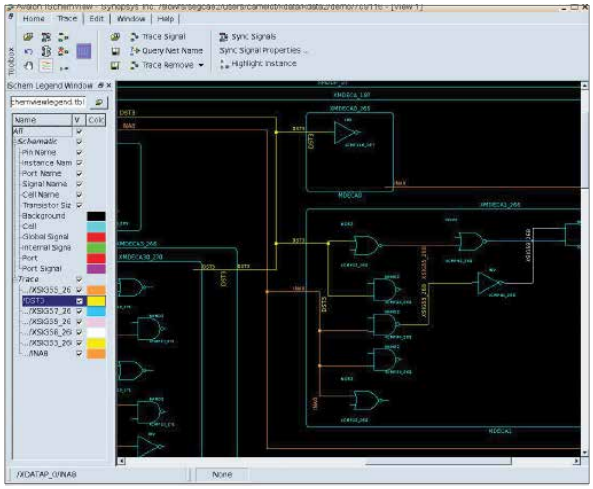

Figure 5: I-Schem creates a schematic from a netlist

**K-Bitmap** allows equipment CAD navigation when analyzing memory chips by identifying the physical location of failing memory cells. It eliminates tedious screen counting by converting the logical addresses, or row and column coordinates, to the physical location.

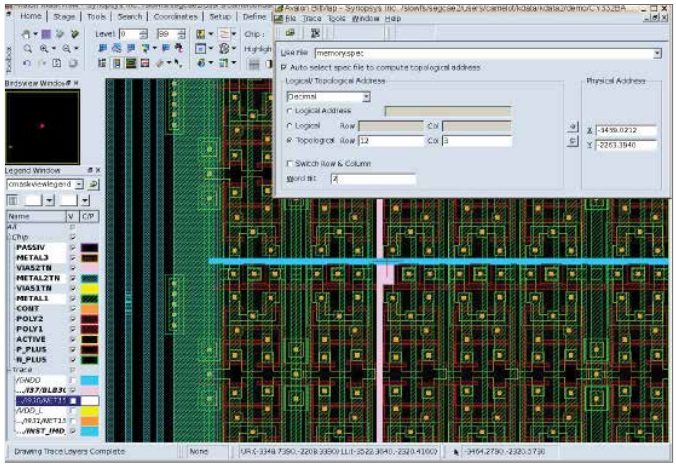

Figure 6: K-Bitmap identifies the physical location of bit addresses in memory devices

**3D Small-Area Analysis** provides a three-dimensional cross- section capability to FA engineers, enabling faster localization of circuit failures to accelerate IC manufacturing yield improvement.

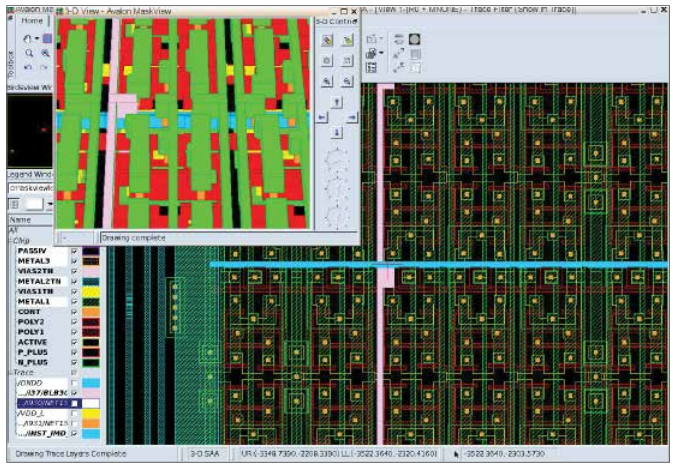

Figure 7: 3D Small-Area Analysis enables faster localization of circuit failures

**Hot-Spot Analyzer** allows user to draw regions on the layout that correspond to hot-spot regions (emission spots) to detect the crucial nets. It finds the nets in each hot-spot region and plots a pareto graph of nets crossing one or more hotspots which helps to easily locate the killer net.

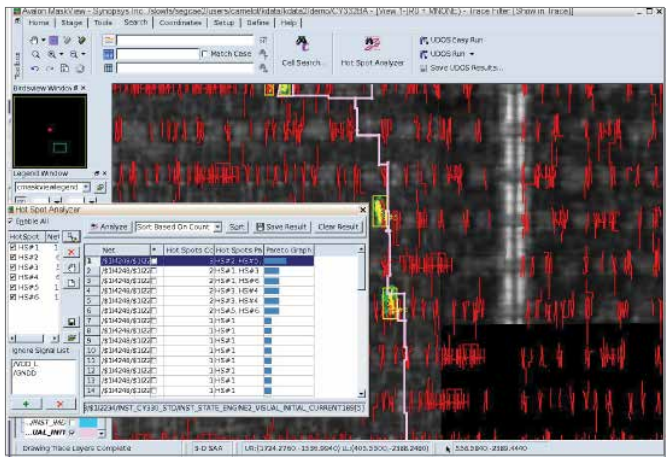

Figure 8: Hot-Spot Analyzer displays number of nets in a hot spot

**User-Defined Online Search (UDOS)** allows users to search a small area of a die for unique polygon features, repeated features or lack of features. Applications include, but are not limited to, FIB-able regions, repeaters, pattern fidelity and lithographic applications.

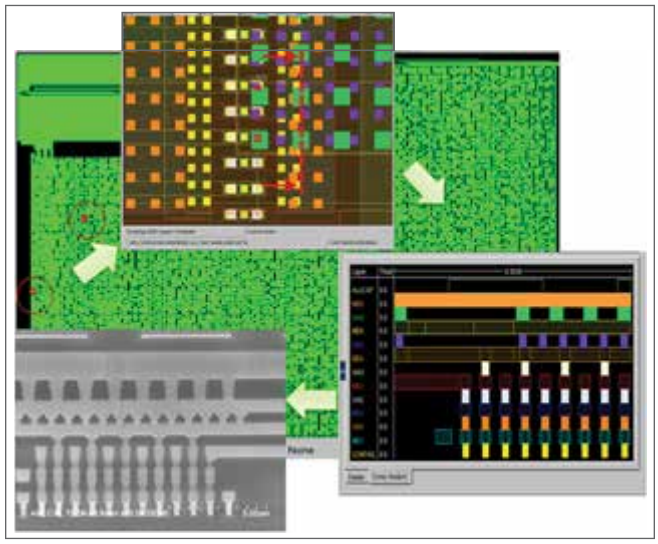

Figure 9: User-Defined Online Search (UDOS) finds easy-to-access traces

**Passive Voltage Contrast Checker (PVC)** quickly and accurately validates the integrity of a circuit's conductivity and provides detailed information for identifying suspect faults at via or metal traces

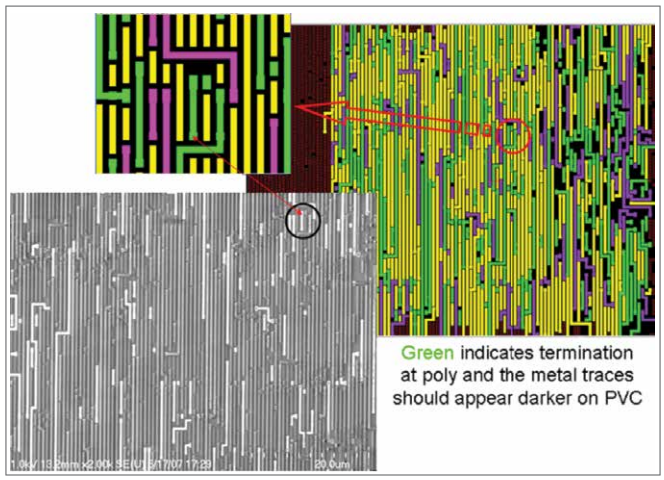


Figure 10: Passive Voltage Contrast (PVC) Checker identifies suspect vias or metal traces

**Electronic Virtual Layer** marks objects to represent net connectivity during a FIB deposit or cut using KEdit. The online trace will simulate the new connectivity to the virtual layer. PVC checker could be used on this virtual layer to simulate the crack or short.

**Check Adjacent Nets** allows logical analysis of nets. This command line tool finds the adjacent nets which are within user-specified threshold distance to find shorts.

**Export Partial Layout** enables the customer to share partial layout data with service labs without compromising the IP of the product.

**Image Mapper** automates the image alignment process in Avalon Maskview and saves a lot of time and effort spent in manual alignment.

**Advanced 3D Viewer** displays real time 3D view of the selected layout area. It shows each process step in the 3D view for which it uses the process data along with design data. It zooms into smaller details and helps to minimize unintended consequences during FIB cuts due to underneath high density structure.

## Avalon Solution

Avalon brings all the advantages of enterprise-wide computing for FA of the chip. Avalon is an open architecture system that connects users over local and wide area networks for seamless integration and database sharing. Instrument integration throughout the fab and other locations throughout the enterprise enables viewing, modifying, characterizing and testing the same wafer location with different instruments, or the same location on wafers at different facilities using the same chip design.

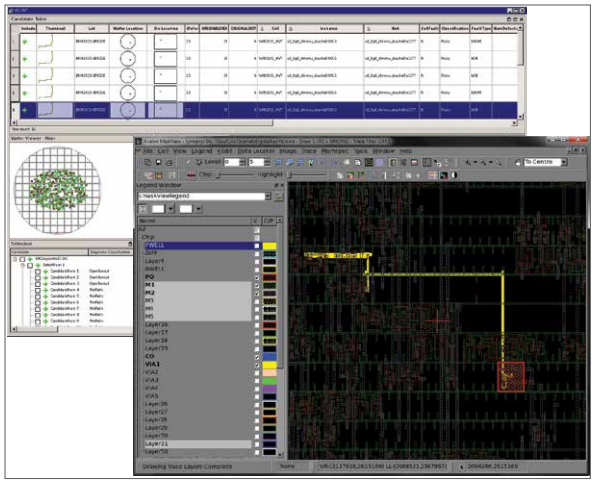

Figure 11: Avalon's open architecture integrates with Synopsys' Yield Explorer

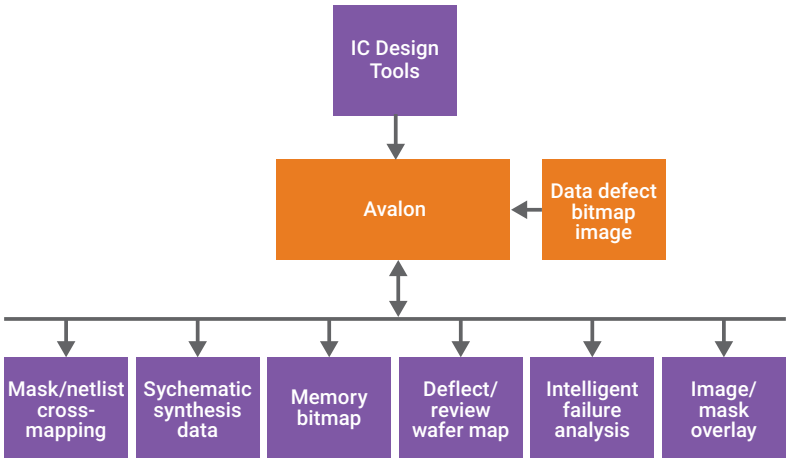


Figure 12: Avalon server solution

## Comprehensive Library of FA Tool Drivers

Avalon provides navigation with almost every equipment used in the FA lab. With a continued commitment to support drivers for all types of test and analysis equipment, Synopsys will continue to develop driver interfaces for new tools as they are introduced to the market, as well as the next generation of existing tools.

## Equipment Supported by Avalon

- Analytical Probe Stations
- Atomic Force Microscopes
- E-Beam Probers
- IR Imaging
- Mechanical Stage Controllers
- Emission Microscopes
- Microanalysis Systems
- FIB Workstation
- Laser Voltage Probe
- LSM
- EDA LVS
- Microchemical Lasers
- OBIC Instruments
- Optical Review
- SEM Tools
- Photon Emission Microscopes
- Laser Scan Microscopes