Numerical Simulation of Metal Interconnects of Power Semiconductor Devices

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***Abstract*—This paper presents a methodology and a software tool – R3D – for extraction, simulations, analysis, and optimization of metal interconnects of power semiconductor devices. This tool allows an automated calculation of large area device Rdson value, to analyze current density and potential distributions, to design sense device, and to optimize a layout to achieve a balanced and optimal design. R3D helps to reduce the probability of a layout error, and drastically speeds up and improves the quality of layout design.**

I. Introduction

The layout of metal interconnects, bond pads, and wirebonds (or bumps/balls) of large-area power semiconductor devices has a profound effect on metal debiasing, and device on-resistance (Rdson) [1-4] and reliability (electromigration). Metal interconnects resistance is especially critical in large-area devices designed to have a very low (up to a few tens of milliohms) ON-resistance value (Rdson). Existing parasitic extraction tools or field solvers cannot handle realistic layouts due to the complexities of the size and geometry of the layout and multi-dimensional nature of the current flow. On the other hand, analytical and spreadsheet models, while being useful, can not accurately capture complicated current flow patterns in devices with complicated top metal layouts constrained by the package, wirebonding, or ball array requirements. The purpose of this paper is to introduce a new software tool (R3D) for simulation, design, and optimization of power device interconnects.

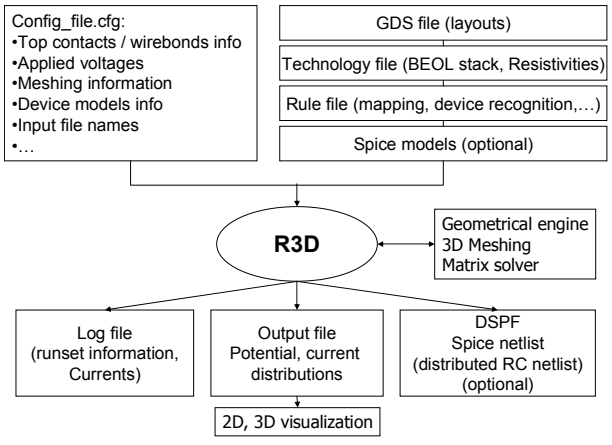


Figure 2. R3D simulation flow diagram (for DC simulations).

II. Simulation Method and Flow

The simulation flow of R3D is illustrated in Fig.1. R3D reads in a standard layout file (GDSII) or database, process technology files, and generates a 3D model representing all resistive elements of the structure (metal layers, vias/contacts, wire bonds/balls, and device cells). It's worth noting that a capability to read standard data files simplifies, streamlines, and speeds up the process of setting up the simulation flow, as well as minimizes the possibility of a human error. The structure is discretized using a 3D mesh, with distributed device instances (SPICE models) connected to the metal mesh through contacts. Current transport equations are solved using a finite difference method to simulate a DC condition with user-specified voltages applied to wire bonds or bond pads. R3D calculates the distributions of potential and current density in all metal layers, vias, contacts, and devices, as well as the currents through wire bonds, and provides the device Rdson value. For transient simulations, R3D generates a SPICE netlist with a distributed RC model that enables a circuit simulation of power ICs with distributed devices.

III. Accuracy Validation

The accuracy of R3D was confirmed by comparing simulation results with the measurement data of test structures (device arrays with different top metal bus length) (see Fig.2). As can be seen from this plot, R3D is providing

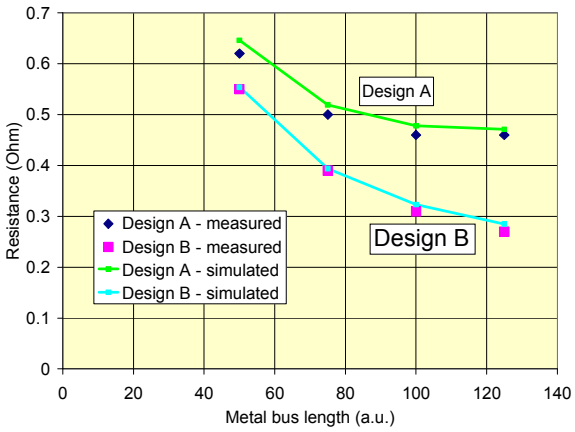


Figure 1. Comparison of R3D simulation results with measurement data for test structures.

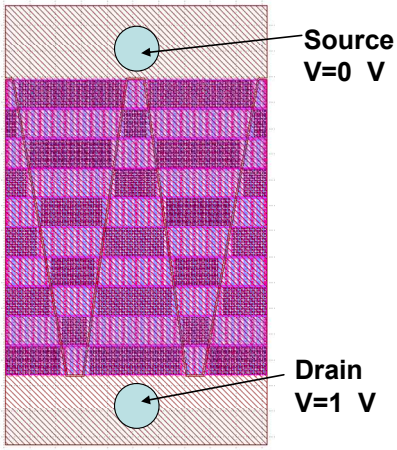


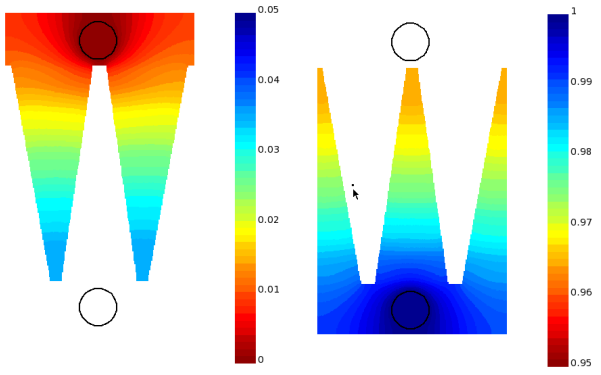
Figure 3. Typical layout of power semiconductor device.

both excellent quantitative agreement, and correct trend predictions. Layouts with a highly resistive (aluminum) top metal layer (design A) do not benefit from increased device area, since Rdson becomes limited by the metal resistance. These devices are facing a "scaling limitation" [1]. On the other hand, design B with a low resistance top metal (thick copper) avoids the scaling limitation, and allows further reducing device resistance.

R3D accuracy has been verified on over a hundred of different power devices having different layouts styles, wirebonding schemes, using both lateral and vertical architectures, and fabricated with different technologies. The agreement was always within the statistical spread of the process variations.

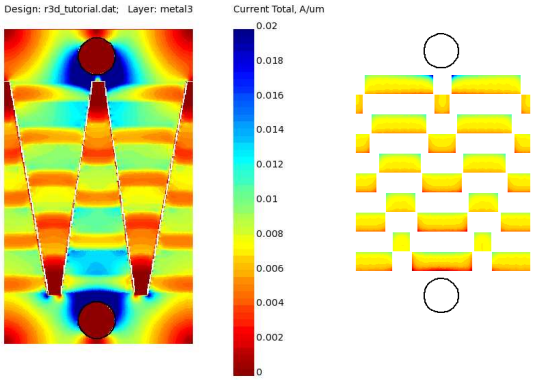
IV. Simulation Results

Fig.3 shows a typical layout of power MOSFET with three metal layers and trapezoidal top metal fingers. R3D simulation conditions corresponded to the Rdson measurements conditions (nominal Vgs and small Vds voltage).



(a) (b)

Figure 4. Potential distribution in the top metal layer for (a) source and (b) drain nets. Wirebond locations shown by circles.



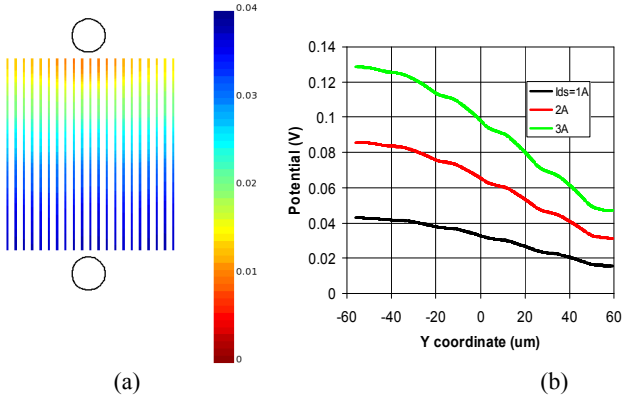
(a) (b)

Figure 5. Current density (a) in the top metal layer and (b) in via2 layers.

Potential distributions in the source and drain nets (top metal layer) are shown in Fig.4, and the distributions of the current density in the top metal layer and via2 are shown on Fig.5.

Analysis of these distributions allows a better physical insight into device operation, and provides a visual aid to explore and optimize layouts of interconnects. The short turn-around time of R3D simulations allows to perform "what-if" analysis to optimize the layout, and to explore Rdson sensitivity to individual resistance components. Automatic identification of regions with high current densities helps to improve the design robustness for electromigration and thermo-mechanical problems.

Fig.6 illustrates a possibility of using interconnect simulations for designing current sense points. Since in the linear regime (ON state) the voltage drop on the interconnects is proportional to the current, one can easily identify the points in M1 or M2 layouts where potential can be used for measuring (or sensing) the large area device current. Similar analysis also helps to identify an optimum location for a sense transistor (a small cell used for current measurements, operating under the same voltages as a large array) to provide current-independent matching.



(a) (b)

Figure 6. (a) Potential distribution in source net (metal 1 layer) and (b) its 1D cross-section in the leftmost metal line for different current levels (enabling current sense point design).

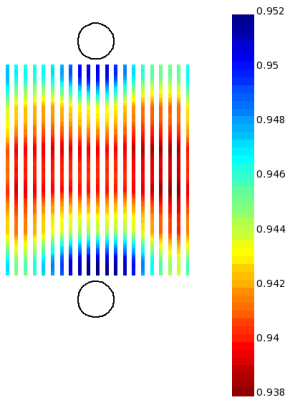


Figure 7. Drain-source voltage (Vds) distribution over the device area.

The distribution of Vds (drain-to-source voltage on device terminals) over the power device area is plotted on Fig.7. Vds displays a maximum near source and drain bond pads, and a minimum in the area between the bond pads, as expected. Analysis of Vds and Ids distributions over the device area provides both qualitative and quantitative estimate on how balanced the design is, i.e. how uniformly the current is distributed. The uniformity is controlled both by metal and via layouts, and by the topology of the source/drain wire bonds.

V. SENSITIVITY ANALYSIS

A typical problem faced by a layout engineer or power IC designer is: what is the contribution of each resistive component to the total device ON-resistance – device/channel, contacts, metal 1, via 1, etc.? Having an answer to this question is important for proper focusing the efforts on layout optimization. For example, if Rdson sensitivity to the top metal sheet resistance is small, it would not make sense to replace the top metal by a lower resistive metal by increasing its thickness or by replacing aluminum layer by copper.

R3D uses a small-signal analysis that provides an automated way to calculate the sensitivity of Rdson to individual resistive components (see Fig. 8). This pareto chart helps to identify the most critical resistive components (M3 and device, in this case) to effectively reduce Rdson. The same analysis provides an automated way to decompose the total Rdson value into device resistance and interconnects resistance.

VI. LAYOUT ERROR CAPTURE AND CORRECTION

The layout of a large-area power transistor is a very complicated system, containing thousands or even millions of elements – metal lines, vias, contacts, etc. The layout is usually created manually or semi-manually, and as a result there is a high chance to make an error. Capturing layout errors by visual inspection using a layout editor is a very tedious and complicated task. On the other hand, the automated rule check and layout-versus-schematics systems

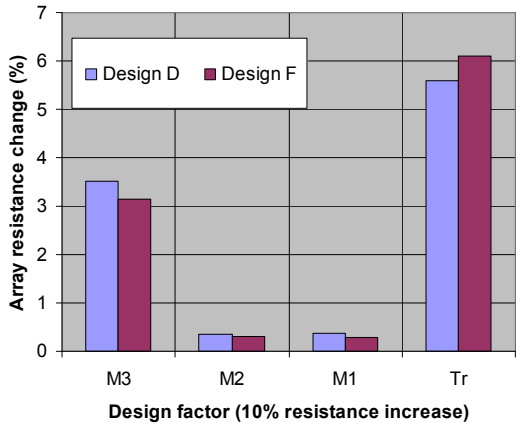


Figure 8. Sensitivity of Rdson value to individual resistance components (M3, M2, M1, and device).

(DRC and LVS) may miss the layout problem (for example, missing via array, or two metals being connected by only one via).

R3D software has been proved to be very effective as a post-layout verification tool. A visual inspection of the color plots of potential and current density distribution allows to immediately identify the problems in the layout – such as discontinuities, current crowding, excessive potential drops, and so on. This might help to avoid costly silicon respins. As an example, Fig. 9 shows an Ids current distribution through the device terminals (a) before and (b) after the layout modifications. The layout modification added more vias

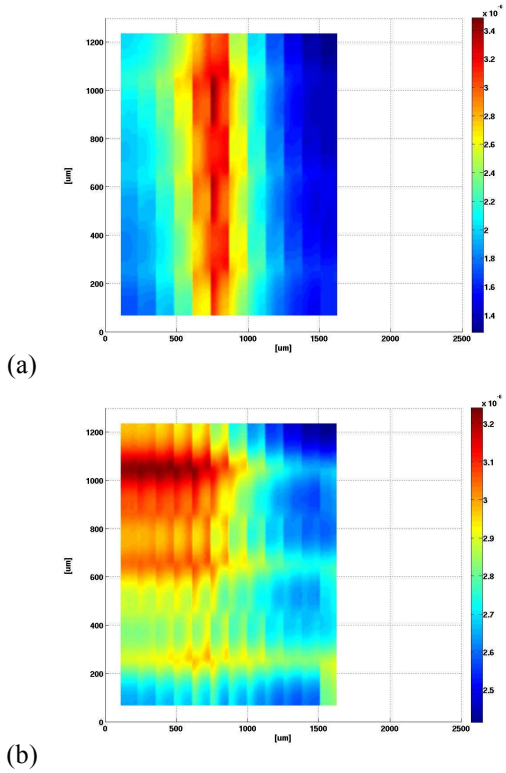


Figure 9. Source-drain current (Ids) through the device (a) before and (b) after layout modification. Modified layout provides a much more uniform current distribution.

between the two top metal layers in the areas outside the pads (in the original layout, these vias were omitted by a mistake). This modification lead to a much more balanced design (more uniform Vds and Ids distributions over the device area), and to an Rdson improvement by over 20%.

VII. CONCLUSION

In this paper, a new software tool – R3D – for simulation and analysis of power transistor interconnects has been presented. R3D has been proven to be very useful in an industrial environment for design and optimization of large area devices (gate width of up to 2 m, and device areas up to ~2x2 mm^2) with different layout styles and fabricated using different technologies.

VIII. REFERENCES

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