

# **VMM User Forum: Methodology Beyond Base Classes**

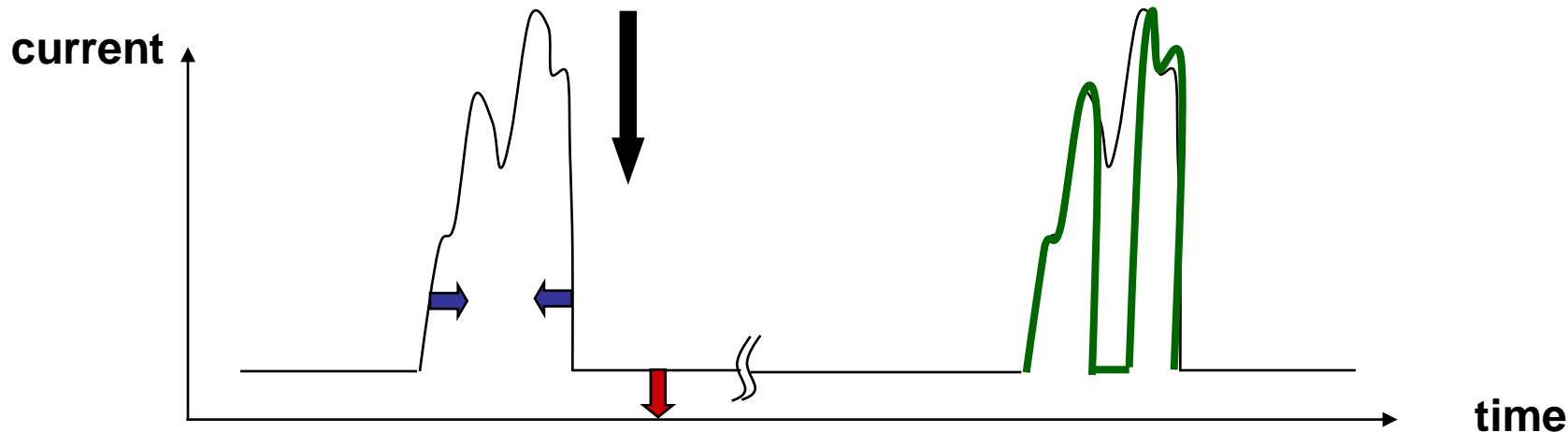
## **Low Power Verification User Experience**

Renesas Technology Corp.  
Yoshio Inoue

6/11/2008 VMM User Forum at DAC 2008

# How to improve standby time for mobile phones

## Operation at Standby



**Technology 1 : Reduce dynamic power**

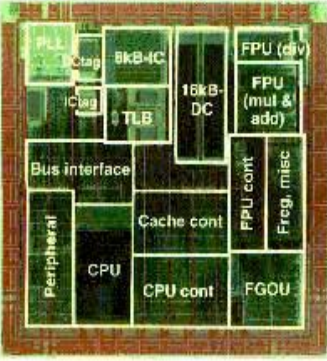
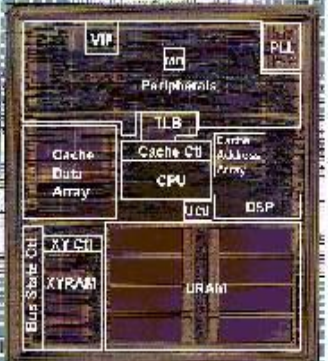
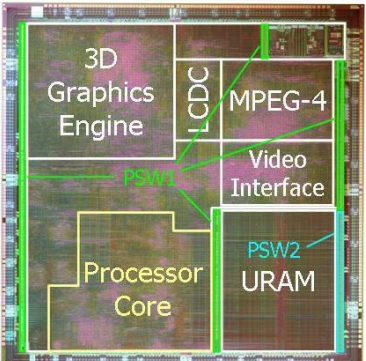

**Technology 2 : Reduce static power**

**Technology 3 : Reduce start up time**

**Technology 4 : Increase standby time  
= Reduce wake up time**

**Technology 5 : System level approach :  
Battery improvement, Power shut down for other  
parts, use low power devices.... etc.**

# Evolution of low power technology

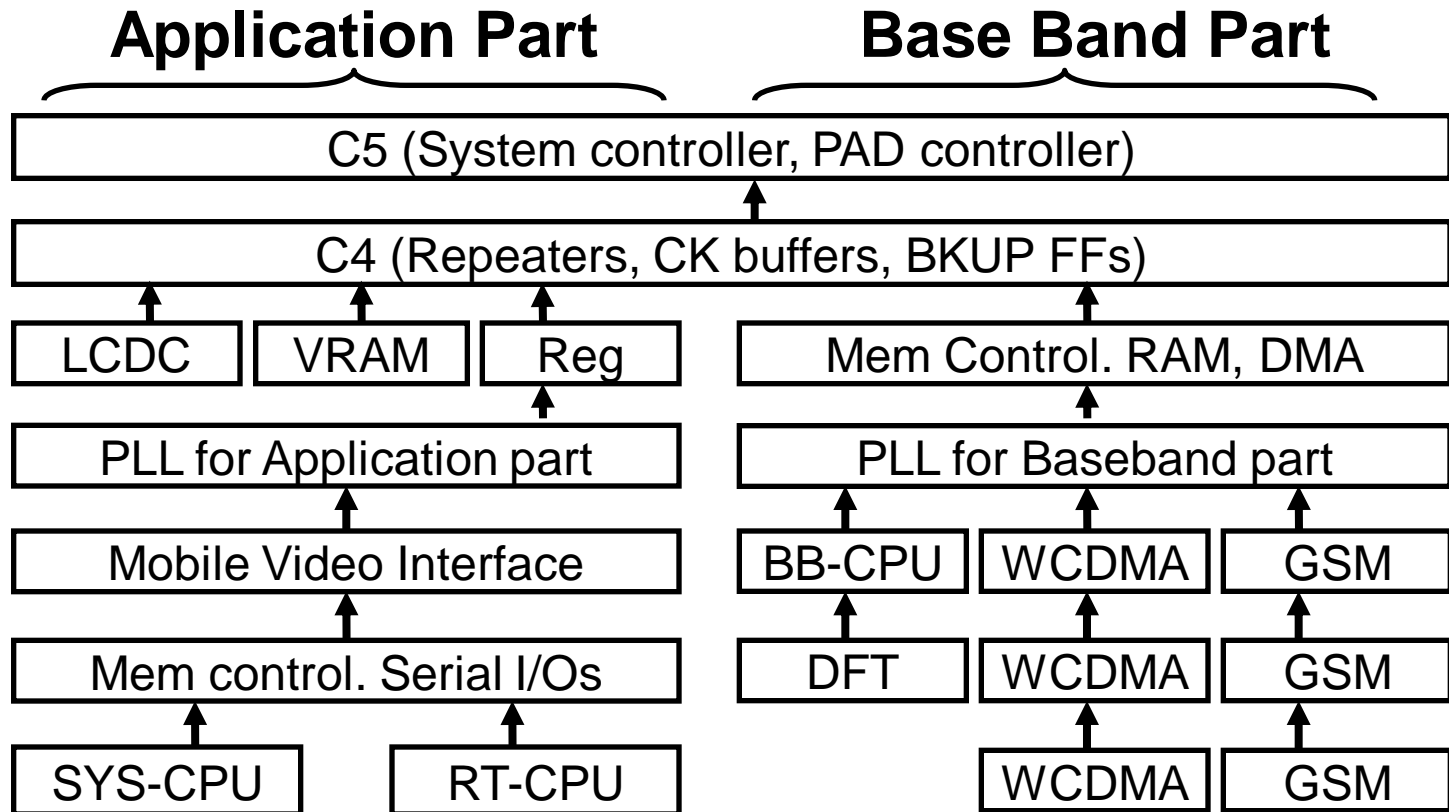
ISSCC98	ISSCC02	ISSCC04	ISSCC06
 <p>0.25um</p>	 <p>0.18um</p>	 <p>0.13um</p>	 <p>90nm</p>
<b>CPU</b>	<b>CPU +SRAM</b>	<b>CPU +SRAM +IP's</b>	<b>3 CPU +Systems</b>
<b>@Clock Stop</b>	<b>@Power Off</b>	<b>@Data Retention</b>	<b>@Active Power-Off</b>
<b>Back Bias</b>	<b>U-standby (Logic Off)</b>	<b>R-standby (Data Retention)</b>	<b>Hierarchical Power Domain</b>

Reference: T. Hattori, et al., "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor", ISSCC visual supplement, P444-445, Feb. 2006.

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# Hierarchical Power Domain Structure

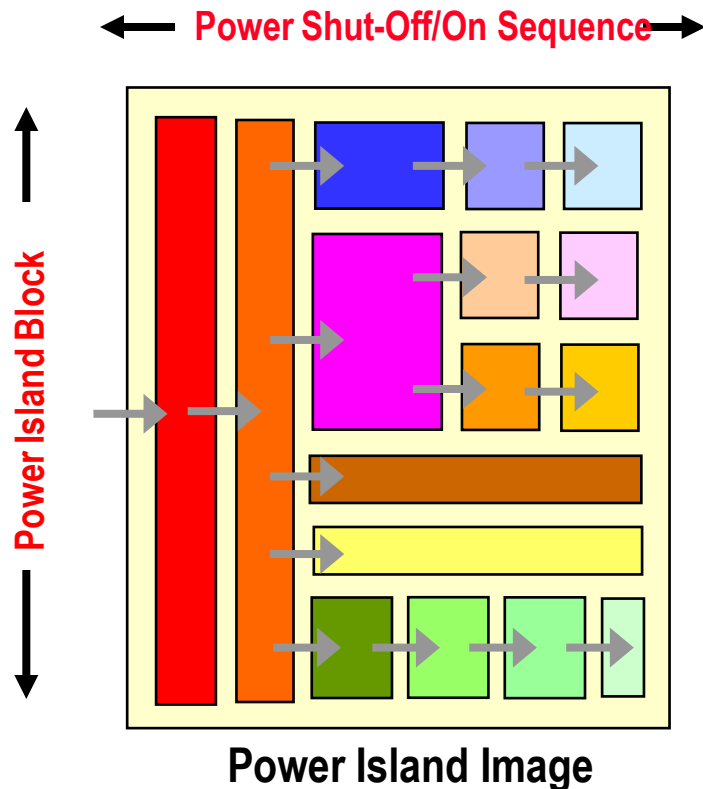
- Minimize mIO Cells for avoiding floating Signals
  - Taking Account for Functional dependency of Activating
- One-by-One Power on to avoid rush current



Reference: T. Hattori, et al., "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor", ISSCC visual supplement, P444-445, Feb. 2006.

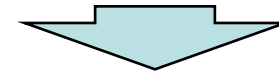
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# Power Shut-Off / On Sequence Definition Issue



Renesas power management scheme consists of  
“Power-On/Off Sequence (Horizontal Axis)”  
“Domain Island Block (Vertical Axis)”,  
2-Dimensional Structure

Total On/Off combination amounts ;  
over **36000** (**Comprehensive**)



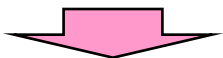
**UPF/CPF Requires;**

Over 36000 lines of sequence definition  
+ Power Domain (Island) Definition  
+ Isolation cell definition (Massive number of nets....)

- Infeasible to describe power shut-off specification with UPF / CPF
- UPF / CPF cannot describe power restoration time
- Requires support for both VDD and VSS shutdown
- Isolation cell varieties (especially Latch type) is necessary

# Power Shut-Off / On Sequence 2D Definition (Example)

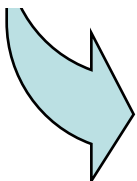
Comprehensive  
Power Domain  
state definition



Prevents Missing  
States



Optimization by tool



Reduction of Power  
domain and Sequence  
relationship



Ease of Verify

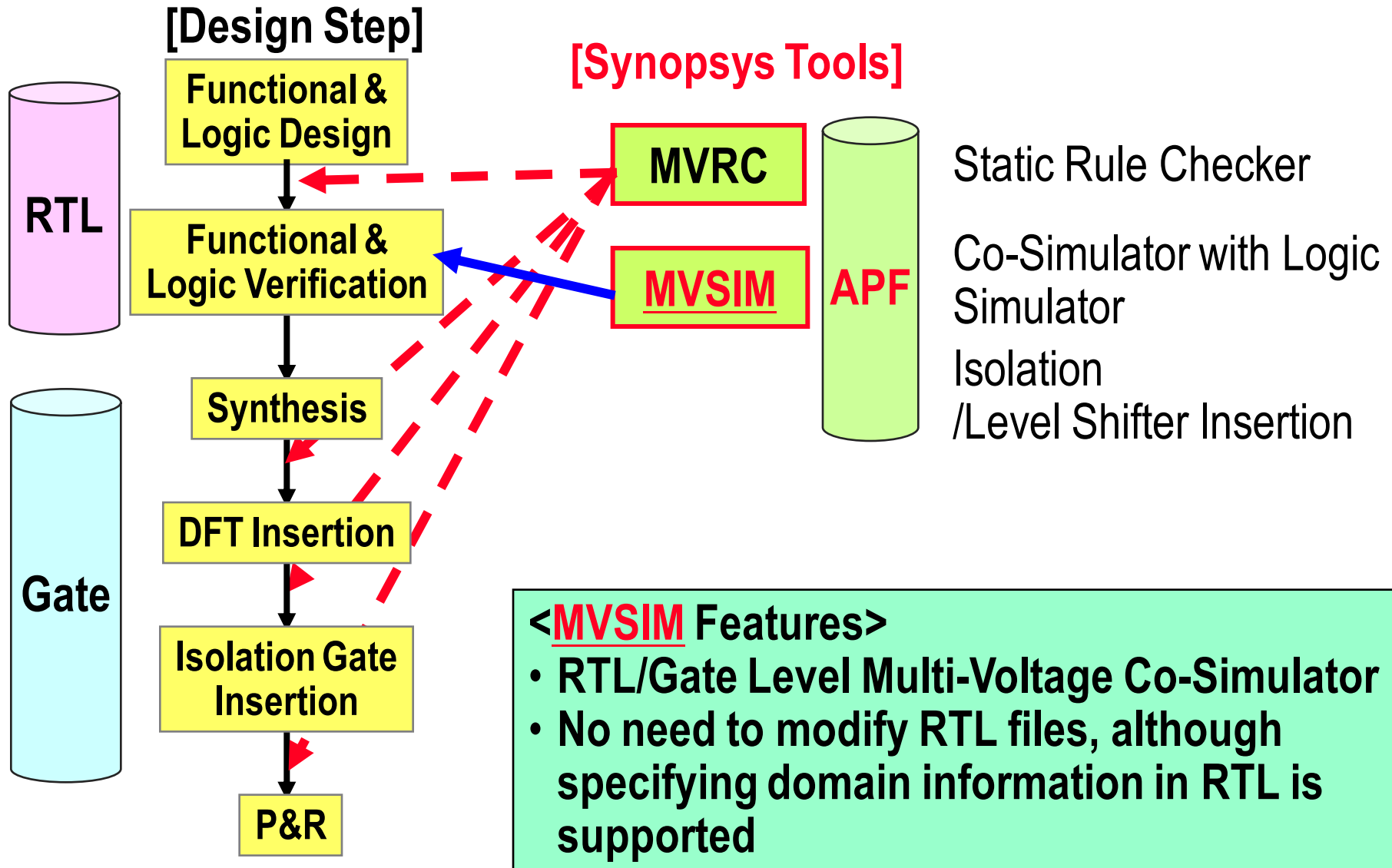
```
LSI.rails = { C5 C4, A4LC, A4MP, A4MV, A4GP, A4S, A4R, BA4, A3SP, A3SM, A3RM,  
             A3RP, BA3, BW3, BG3, A2RG, BW2, BG2, A2RL, A2SL, BW1, BG1 };  
LSI.state ["S-1"] = { 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-2"] = { 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-3"] = { 1, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-4"] = { 1, 1, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-5"] = { 1, 1, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0 };  
:  
LSI.state ["S-35998"] = { 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 1, 0, 1, 1, 0, 1, 0, 1, 0, 1 };  
LSI.state ["S-35999"] = { 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 0, 0 };  
LSI.state ["S-36000"] = { 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 0, 1 };
```

```
LSI.rails = { C5, C4, A4LC, A4MP, A4MV, A4GP, A4S, A4R, BA4, A3SP, A3SM, A3RM,  
             A3RP, BA3, BW3, BG3, A2RG, BW2, BG2, A2RL, A2SL, BW1, BG1 };  
LSI.state ["S-01"] = { 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-02"] = { 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-03"] = { 1, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-04"] = { 1, 1, 1, 1, 1, 1, 0, 1, 1, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1 };  
:  
LSI.state ["S-44"] = { 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 1, 1, 1, 1, 1 };  
LSI.state ["S-45"] = { 1, 1, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0 };  
LSI.state ["S-46"] = { 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1 };
```

# Verification Items and Corresponding ArchPro Tool

Verification Items	Corresponding ArchPro Tool
Missing and Incorrect Isolation	MVRC, some cases MVSIM
pdnAck power off dependency	MVRC, sequencing with MVSIM
Clock gating to off islands	MVSIM
Isolation on reset	MVRC
Hierarchical, non hierarchical relationships	MVRC
Low VDD Stby state RAM access	MVSIM
Power ON sequence initiated by Reset	MVSIM
Missing Reset during Power ON sequence	MVSIM
Micro-architectural problems	MVRC
Correct # of clocks	MVRC
Correct # of resets	MVRC
Check if instances, protection-gates in correct islands (ie island-partitioning)	MVRC
Correct Rails, islands	MVRC
CPG powered OFF, Reset Check	MVRC

# ArchPro Tool Overview (Design Flow)



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**Renesas Technology Corp.**

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