

Need for a Low Power Verification Methodology

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Evolution of power at ARM

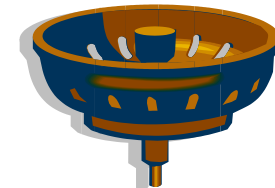
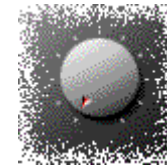
- Always been a 'low power' focused company
- Last but one generation cores had WFI (wait for interrupt)



- Then came IEM (intelligent energy management)



- Then came leakage management extensions for IEM



Validation Complexity

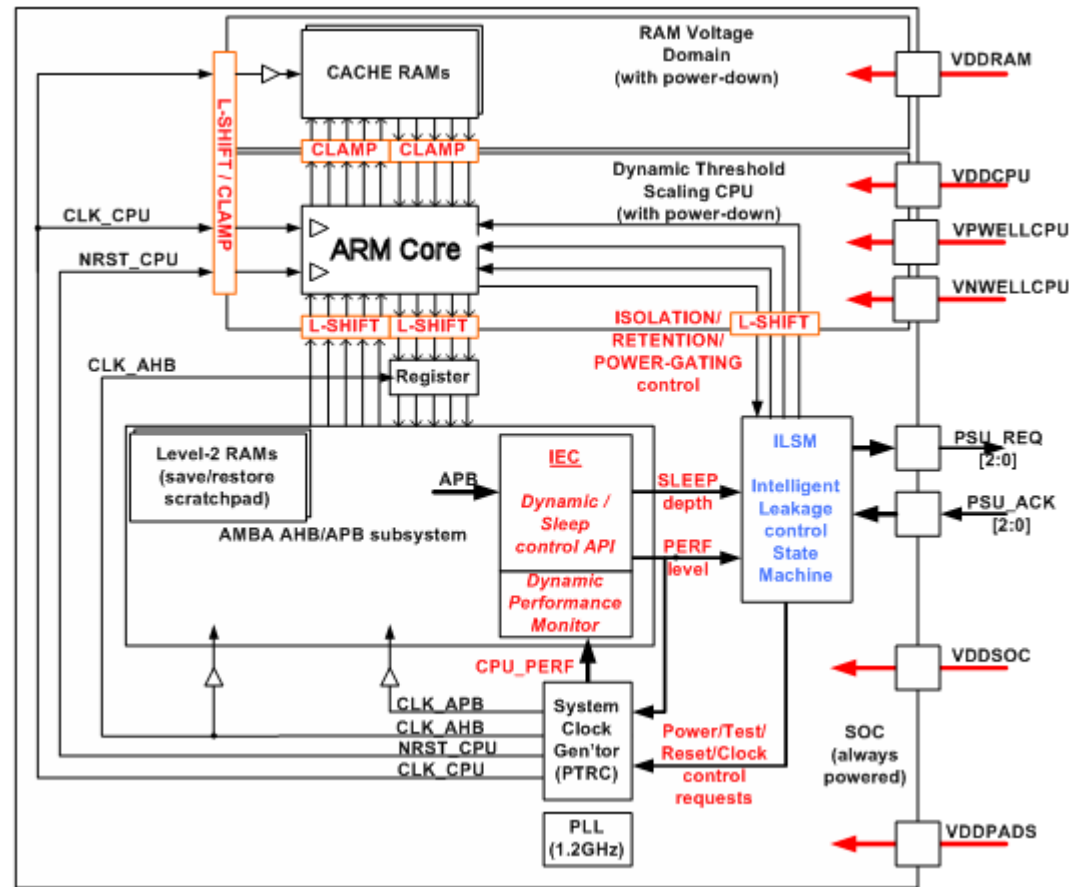


Some details on validation complexity

- Early cores had only one power domain
 - No additional testing required – always on
 - ARM926EJ-S and later cores added WFI
 - A small amount of additional testing, but nothing too complex
 - IEM enabled cores started adding power domains
 - ARM1176JZF-S first multi-voltage IP (3 domains) + Async Bridges
 - Async AXI slices adds significant verification & validation challenges
 - Cortex-A8 has 5 power domains (configurable by the implementer)
 - So potentially 32 simulation models to compile and run
 - MP can make matters worse
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- But we have it easy compared to our partners building complex SoCs

The Reference System Design

- Joint dev with Synopsys
- Multi-Voltage design
 - DVFS w “IEM” control
 - Hardware retention
- Leakage Mitigation
 - HALT – freeze clock
 - SRPG – freeze state
 - Scan Hibernate PG
 - Shift state in/out
 - SHUTDOWN
 - Software checkpoint
 - Well Back-bias (implemented for the 90G case study)



How methodology helps

- Standard way of describing power domains
 - We can use for all our internal development
 - Simplifies validation of the design prior to release (with the correct tooling)
 - Allows everyone to talk the same language
 - Eases trial implementation burden
- Will make it easier for our partners
 - Allows partners to integrate quickly into their SoCs
 - Allows the use of more advanced 'pre-tested' power flows
 - Eases SoC implementation burden
- This is why we partnered with Synopsys on VMM-LP
 - Gives the design community an invaluable resource
- Time to market improvement

Conclusions

- Complexity of power implementations is increasing
 - From our core perspective
 - From partner SoC implementation perspective
- Standard power descriptions enable understanding and temper complexity
- A well defined methodology allows broad acceptance of technology