

# XA Option for HSPICE and NanoSim

## Raising the Bar for Circuit Simulation

### Overview

*Low-power, high-performance designs drive the increasing integration of analog functionality onto mixed-signal SoC designs. An ever-increasing cause of failure is tuning analog circuitry to meet specifications. With the growing cost of nanometer mask sets, analog tuning can no longer be performed over multiple respins.*

*Verifying that analog content meets specifications and that a mixed-signal design will produce high yield needs to be completed before the first tapeout. Verifying analog and mixed-signal designs including post-layout parasitics and accounting for process variations demands high-capacity, high-performance, SPICE-accurate simulation capabilities.*

The XA simulation technology is the next-generation transistor-level simulation engine that delivers SPICE accuracy while maintaining FastSPICE performance and capacity with time to results (TTR) never seen before. Numerous revolutionary patentpending technologies, including dynamic partitioning and autodetection enable SPICE-like accuracy while delivering over 50x performance improvement over SPICE without any tuning. The XA simulation technology is a full-featured stand alone transistorlevel simulation engine designed to augment NanoSim® and HSPICE® as an add-on option addressing the need of NanoSim and HSPICE users for SPICE accuracy without any tuning.

### Key Benefits

- ▶ Unprecedented TTR on all circuit types
- ▶ FastSPICE performance and capacity delivering SPICE-accurate results
- ▶ Predictable and repeatable results using a single, easy-to-use accuracy setting that can be set globally or locally
- ▶ Highest accuracy setting runs the same as SPICE
- ▶ Superior capacity due to unique hierarchical data storage structure
- ▶ Revolutionary built-in simulation intelligence for identifying circuit topologies
- ▶ Optimized simulation technology for sub-90nm designs
- ▶ Enables full-chip functional verification of AMS SoC designs with post-layout parasitic elements
- ▶ Advanced array and RC optimization techniques provides superior capacity for simulating post-layout parasitic databases

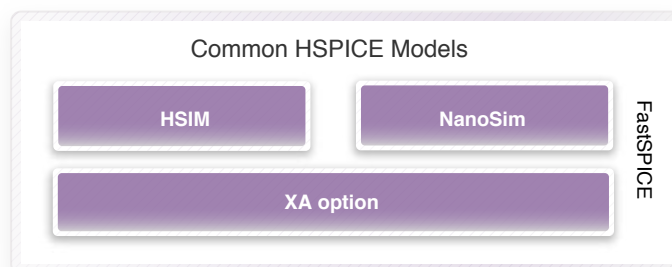


Figure 1: Synopsys' Comprehensive FastSPICE portfolio

	XA	FastSPICE	SPICE
Phase-Lock Loop	2.5 days	~24 days	n/a
Switching Regulator	48 mins	4.1 hrs	24 hrs
Driver	58 mins	5.4 hrs	14.1 hrs
Charge Pump	3 mins	4 hrs	13 hrs

Figure 2: Accelerated simulation of analog and mixed-signal designs

## Accelerated Simulation of Analog and Mixed-Signal Designs

The XA simulation technology is well suited to simulating analog and mixed-signal circuits with non-ideal power supplies. Low-power designs require tightly regulated supply rails and verifying that mixed-signal designs startup correctly requires long transient simulations. The XA simulation technology with SPICE-accurate, high-performance transient analysis enables customers to simulate large analog designs requiring lengthy startup times. In addition, the XA simulation technology is well suited to simulating PLL lock times and switched-capacitor circuits.

## Post-layout Parasitic Verification

The XA simulation technology provides designers with various back-annotation options. The fully extracted parasitic database can be simulated directly or back-annotated to the ideal schematic netlist at any level of hierarchy. In addition, a unique integration with StarRC™ provides an efficient extraction and back-annotation flow that accelerates the verification of your designs while including post-layout parasitic data.

## SPICE-accurate Signoff Confidence

Full Support for SPICE algorithms such as Newton-Raphson and LTE enables the XA technology to achieve SPICE accuracy. Designers can configure their simulations to utilize a mixed set of accuracy settings to achieve the optimal simulation time, but verifying with SPICE accuracy that blocks under test meet design specifications.

## HSPICE Common Model Library

Synopsys transistor-level simulators all share a common HSPICE® model library. This ensures that all Synopsys transistor-level simulators use the same model equations and therefore eliminate any model correlation issues. A common library ensures that all simulators pick up model updates at exactly the same time.

## The XA Option Supports:

- ▶ HSPICE and Eldo Netlist Formats
- ▶ HSPICE Common Model Library
- ▶ Eldo models
- ▶ SPF, DPF and SPEF parasitics netlist formats
- ▶ OUT, WDB and FSDB output formats
- ▶ VCD and VEC Stimulus input formats
- ▶ TCL scripting

## Platform Support:

- ▶ SUN 32/64
- ▶ LINUX 32
- ▶ AMD 64