White Paper

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Save Time and Money with CustomSim Native Circuit Checks

Find Electrical Rule Violations and Power Management Failures Before Tape-out

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Introduction

Consider the number of checks that an IC design team has to go through before tape-out. In each company, chip failures ultimately translate into additional checks in the sign-off flow. Technology and design trends are responsible for further increasing the number of checks. In the design flow, mature solutions exist for verifying compliance with physical design rules (DRC). However, when it comes to verifying electrical rules, the solutions have been piecemeal and, in many cases, homegrown. This is because individual electrical rules need to be checked at different phases of the design either in schematic or layout, requiring knowledge of circuit functionality, operating regions, and physical design. Until now, no single solution has been available that can address all of these individual checks across the complete design flow and provide the capability for designers to add additional checks through a programmable interface. Often, it has only been possible to check for certain failure mechanisms by eyeballing the design or manually inspecting layout—a process that is time-consuming and error-prone.

The CustomSim™ circuit simulation solution introduces native circuit checks into the AMS domain, providing a single solution for electrical rule checking. In this white paper we will discuss some examples of the failure mechanisms that are detected by the native circuit checks, how native circuit checks enable verification of power management techniques, as well as discuss how customized checks can be implemented.

Electrical Rule Circuit Checking

The CustomSim native circuit checks provide a comprehensive set of static and dynamic checks. These checks are invoked at different stages of the design cycle including pre-simulation design analysis, DC static analysis, transient dynamic analysis, and post-simulation waveform analysis, as illustrated in Figure 1. The inputs to these stages include the design, extracted post-layout data, and the native circuit check command file. This solution increases productivity by providing a number of predefined checks that can be used immediately, as well as allowing for customizations using the extensive command syntax. Typical examples of violations that designers can check for are:

- Maximum ratings for safe device operation
- Incorrect substrate connections
- Excessive leakage due to erroneous connection between different supply domains
- Potential leakage path due to floating gates
- Standby current estimation

Quite possibly the single largest contributor to the introduction of these checks has been the introduction of power-management techniques to address low-power concerns. Complex power-management schemes employ a number of techniques, such as dynamic voltage scaling, multi-V_T devices, dynamic frequency scaling, and power gating to reduce power consumption. These techniques can introduce errors which are difficult and often impossible to detect with circuit simulation alone. Using native circuit checks, designers can increase verification coverage by employing high-speed static checks for additional verification prior to tape-out.

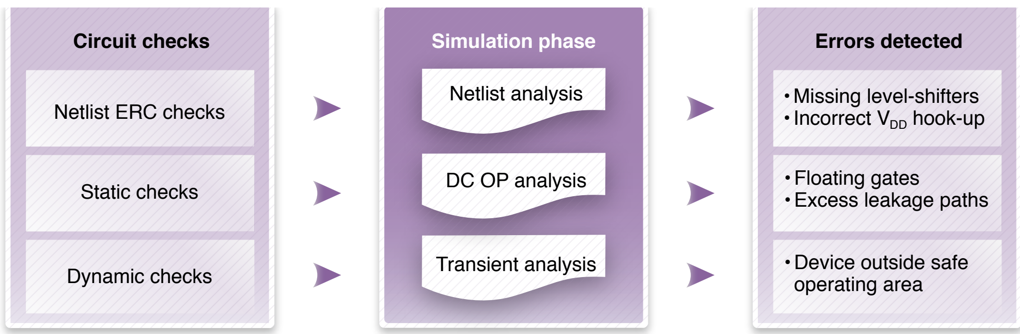

Figure 1: Native circuit checking flow

Maximum ratings for safe device operation

A long time ago designers could take comfort from the fact that it was nearly impossible to exceed the maximum device ratings for safe operation. Using only a single power supply on-chip, as long as V_{DD} and V_{SS} were maintained within a well-defined range it was safe to assume that as long as devices passed DRC and were sized within range then violating the safe operating region would not be possible. However, with the introduction of multiple supply domains and the fabrication of multi-V_T devices, as well as the significant reduction in device geometries, it became all too easy to violate a device's safe operating area.

CustomSim provides the ability for design teams to define the safe operating region (usually translated from the foundry's DRM) for all on-chip devices and then continuosly monitor to ensure that none of these devices exceed the maximum ratings for safe device operation. Special conditions can be applied on a per-instance basis. Users can choose to automatically stop the simulation when a violation occurs or wait until completion and browse a violation report that identifies which devices and over what period of time the safe operating region was exceeded.

Detecting excess leakage current

Excess leakage current is defined as unwanted or unexpected leakage. Figure 2 illustrates a typical situation where excess leakage current can occur due to a partially-conducting PMOS device connected between multiple power supply domains. Transient simulation alone is costly and time-consuming to identify these types of errors and offers very limited coverage.

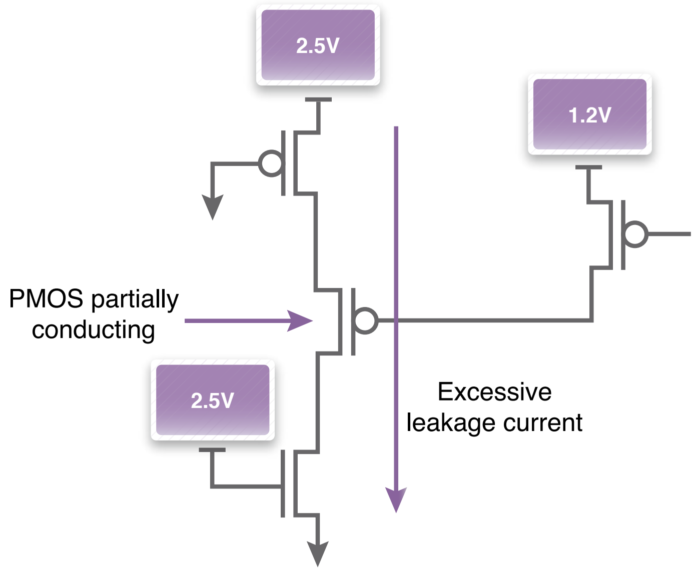

Figure 2: Unwanted leakage current due to partially-conducting PMOS

Symptoms of excess leakage current manifest themselves after tape-out when silicon is being tested. These could be slow current spikes during standby mode. Exacerbating the problem is the random nature of leakage current—symptoms could be seen only on specific parts and at different times of the product life cycle. Once identified, the symptom itself is hard to debug, and transient simulation alone is not sufficient to reproduce the observed effects due to the dependency on process parameters, wafer lots, and temperature.

Other causes of excess leakage current include, but are not limited to, floating gates (transistors being driven from high impedance nodes) in standby mode, resulting in the possibility of driving inverters and other logic gates at mid-rail and inadvertently forward-biasing of bulk diodes due to incorrect substrate connections. These situations are very difficult to identify using transient simulation since transistor-level simulators will always converge on a voltage value for high-Z nodes, and in the majority of cases this could be either logic '1' or logic '0'. Figure 3 illustrates a typical situation where high-Z nodes can cause unwanted leakage current.

CustomSim native circuit checks provide a number of commands and checks to rapidly identify all of these situations. Designers can configure a static check to rapidly analyze all substrate connections during DC operating point analysis to verify that bulk terminals are connected to the correct supplies. To check for floating gates, an additional command can be configured to activate a check during standby mode for any DC paths between two user-defined power supplies. The check will report DC paths as well as any MOS gates or BJT bulk terminals that are connected to high-Z nodes. As with all other checks, designers can elect to terminate simulation when one of these situations occurs or wait until the completion of the transient run to analyze the native circuit check violation report. Instead of relying on transient simulation alone, using these checks guarantees much wider coverage and faster identification of violations.

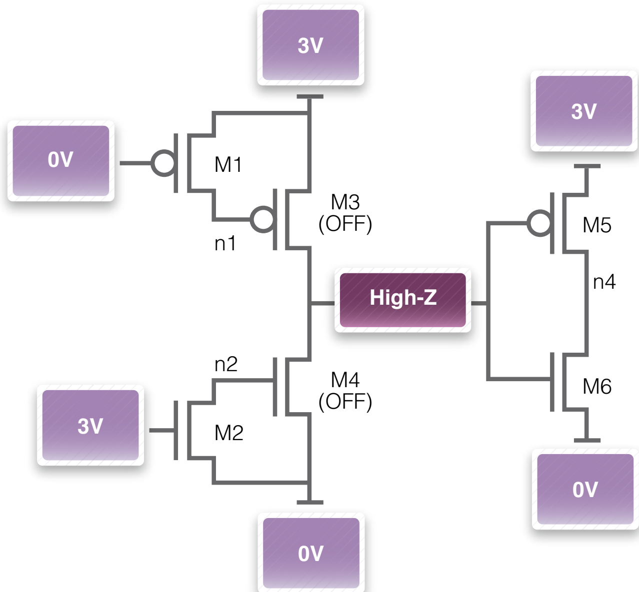

Figure 3: Leakage due to high-z node in standby mode

Static and dynamic signal integrity checks

Cross-coupling between logic signals can cause noise-induced switching. Parasitic capacitors are the primary source of cross-coupling connections. Since the current through a capacitor is directly proportional to the rate of change of the terminal voltage, fast rising or falling nodes (aggressors) cause noise glitches on the opposite terminal that can affect timing and possibly switch logic.

CustomSim's native circuit checks provide additional checks that monitor delay paths connected to parasitic coupling capacitors and monitor fast rising or falling nodes, and estimate the magnitude and impact of the noise glitch. The checks are both static and dynamic, initially checking for noise glitches and then monitoring nodes dynamically for cross-talk effects.

Waveform Post-processing

Depending on an organization's design flow or verification methodology, it may be necessary for a set of dynamic checks to be run on simulator output data rather than during a simulation. This can be due to a number of reasons; in some cases a priori information of which signals or devices need to be checked is not available and can only be determined after simulation. Therefore, instead of re-running the simulation, designers can simply run the appropriate checks on the simulation waveform output data. Many other reasons exist for this need, so the CustomSim solution provides the added capability for designers to run dynamic checks by post-processing of simulation waveform data.

Conclusion

In this white paper we have discussed a number of electrical rule violations that can cause chips to fail at some point in their life cycle—be it during the initial wafer testing or much later in production usage. Many of these failures are very difficult to debug and the later they are found the more expensive they are to fix. The CustomSim solution provides a comprehensive set of static and dynamic checks that can check for electrical rule violations, power management failures or topology errors during the design phase and detect many of these errors prior to tape-out.

The native circuit checks increase productivity through automation with a built-in set of static and dynamic checks for designers to take advantage of without additional effort. Designers can improve confidence through increased error coverage utilizing high-speed static checks in addition to the increased accuracy delivered by the dynamic checks. Checks are applied at a number of different phases during the design and simulation cycle, including netlist read-in, DC operating point analysis, transient simulation, and post-simulation waveform processing. Once detected, each violation can automatically stop simulation or the native circuit checking can generate a violation report that can be analyzed to identify areas of concern that may cause chip failure.

CustomSim's native circuit check has helped many designers find potential failures in their designs and is now an established part of their sign-off flow.

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