

IC WorkBench

High Speed Layout Visualization and Lithography Analysis

Overview

IC WorkBench (ICWB) is a powerful, hierarchical layout visualization and analysis tool with GDSII/OASIS viewing, layout editing, and high-speed lithography simulation and analysis. IC WorkBench is designed to address a variety of lithographic applications including: Mask Synthesis flow development, OPC model development and calibration, lithography verification error analysis, design rule creation and validation, yield and printability optimization of critical cells, and new process development.

IC WorkBench provides qualitative and quantitative information on wafer imaging characteristics under varying parameter and process conditions.

High Speed, High Capacity Viewing and Editing

ICWB builds on a solid foundation of fast GDSII/OASIS viewing and editing tool designed to handle the geometrically increasing file sizes of advanced process nodes. ICWB loads gigabytes of data in minutes and has an unlimited file size capacity on 64 bit platforms. Fast zooming and panning ease exploration and analysis of the largest GDS patterns. In addition, ICWB can overlay two layouts in a single view without merging the underlying GDS files.

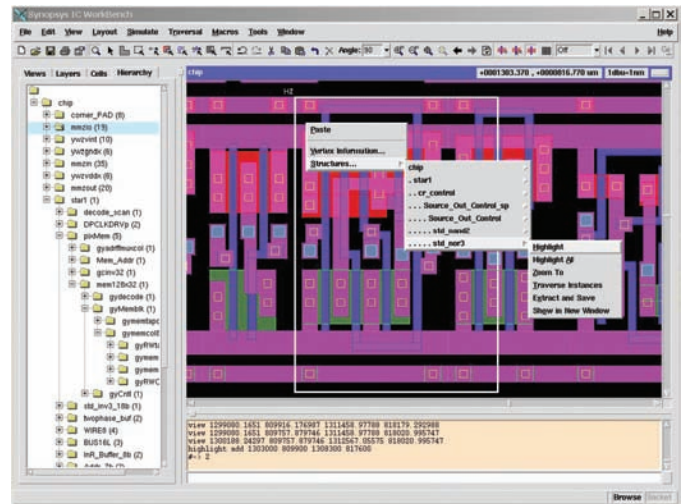


Figure 1: Probing hierarchy from layout view with context sensitive pop-up menu for cells

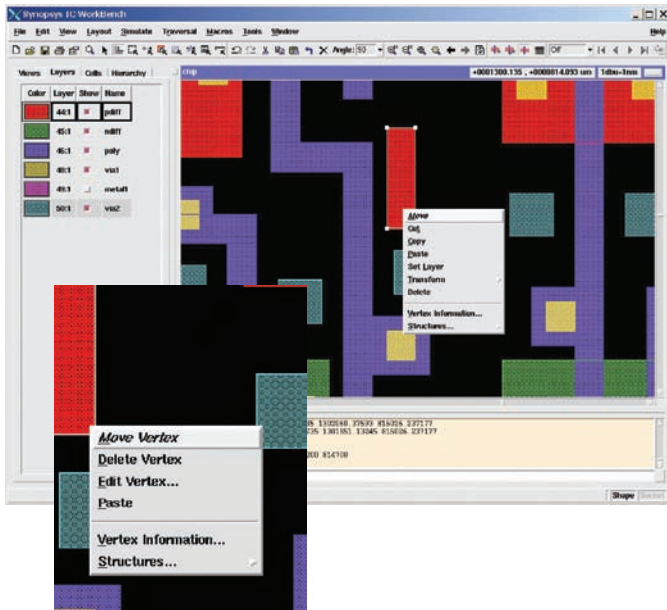


Figure 2: Polygon and Vertex editing functions

Powerful Standard Tcl/Tk Scripting Command Language

ICWB commands and functions are built on the widely used, standard Tcl scripting language. The powerful scripting capability within IC WorkBench enhances interactive operation by enabling custom commands and functions to be created and accessed as macros. In addition, the Tcl scripting command language enables batch mode operation to support automation of any functions that can be conceived in the language. The GUI can be extended using TK.

In addition, to support advanced power-users, the command language can be accessed via a Socket Interface. The Socket Interface enables API-like connections to other tools for development of more sophisticated and custom applications and flows.

Accurate, Programmable Lithography Simulation

ICWB reads the industry leading, highly accurate Progen model files to ensure accurate, fast simulation. Progen models are the standard Synopsys lithography simulation models used across the entire Synopsys DFM tool suite to ensure excellent correlation and simulation closure across the DFM flow. IC WorkBench supports contour, pseudo-color aerial image, slice, and numerous quantitative simulation functions. The Macro Command Language can be used to automatically run and disposition pre-defined assessments. IC WorkBench can also read in, overlay, and align SEM images to compare to the layout and simulations.

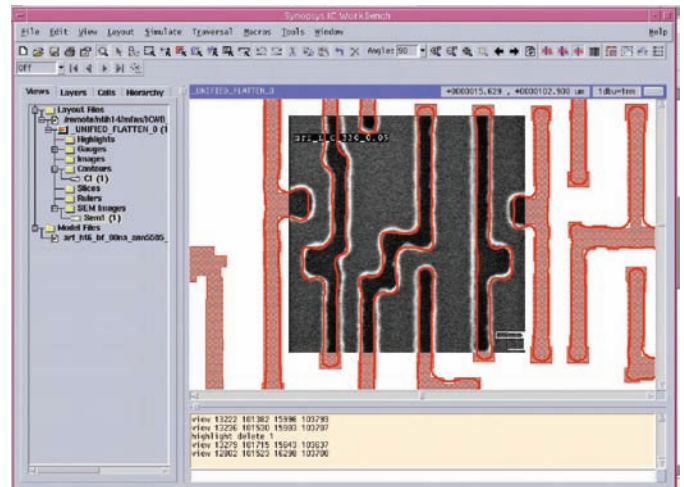


Figure 3: Overlay SEM image to compare to the layout and simulation

Advanced Usability Features

IC WorkBench implements the latest in user interface technology. These technologies are architected to make the powerful ICWB capabilities easy and intuitive to use. Key features include:

- Support for user and site level customization
- View Manager
- Hierarchical folder representation of all objects including layouts, gauges, contours, aerial images, and models
- Context-sensitive Bubble on-line help
- Browser-like forward and back view history
- Undo and redo
- Rich context-click information available, such as hierarchy information from a cell or polygon
- Fast loading of GDSII using cache file
- User mappable hot-keys for most commands
- User customizable toolbars
- Custom buttons to run user-created macros

Common Analysis Tool for Mask Synthesis and Lithography Verification

IC WorkBench is the common, central, interactive analysis tool for the Synopsys DFM tool suite. Layout viewing, silicon simulation, and related interactive measurement and analysis are central to all aspects of the development and production operation of a Mask Synthesis and Lithography Verification flow. For this reason, IC WorkBench integrates smoothly with the Synopsys DFM suite of tools such as Proteus and SiVL. To ensure modeling and simulation closure, IC WorkBench and all the Synopsys DFM tools use the same highly accurate Progen models and simulator.

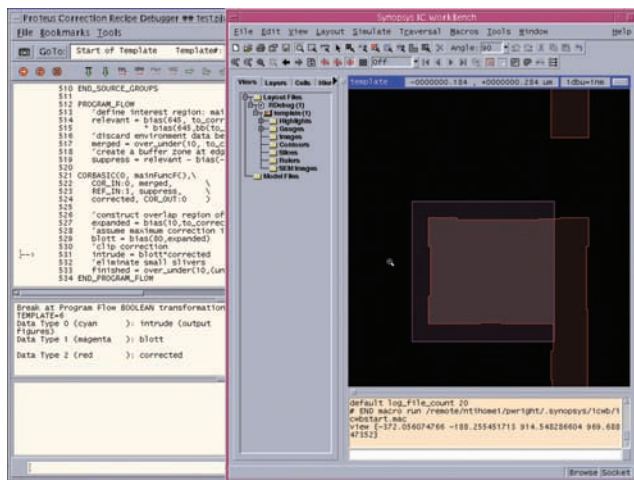


Figure 4: Proteus recipe debugger with IC WorkBench interactive viewing of results

Mask Synthesis Flow Development

IC WorkBench provides key functions needed for development, qualification, and production operation of the Mask Synthesis flow and models. IC WorkBench links directly to the Proteus Recipe Debugger and runs simultaneously to provide a powerful, interactive recipe debugging capability. As the debugger executes the recipe, the portion of the recipe being executed is highlighted in the debugging window and IC WorkBench provides a simultaneous view of the actual OPC/RET modifications being made to the pattern being operated on. When the debugger has paused execution, the result can be simulated to determine the effectiveness of the recipe and models. In addition IC WorkBench can make programmable measurements and plots of the target and corrected patterns as well as the simulated wafer image. Simulation capabilities include contour generation, intensity field display, and pseudo-color imaging.

Examples of Mask Synthesis flow and model development and production operation applications using IC WorkBench and Proteus include:

- Quickly debug and optimize Proteus recipes through a direct link to the Proteus recipe debugger

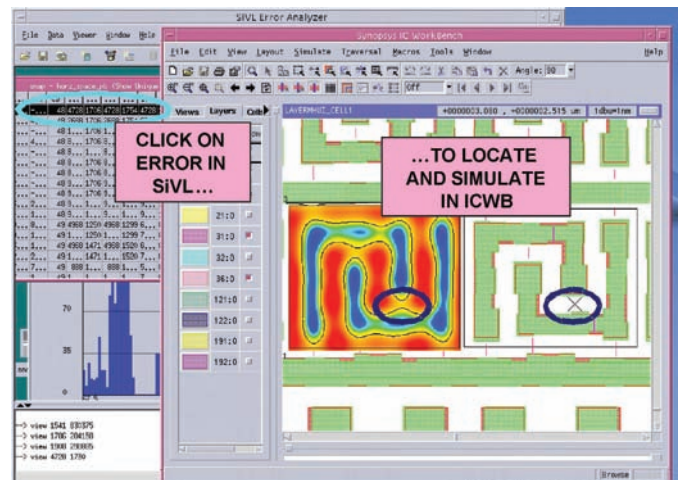


Figure 5: IC WorkBench integrates tightly with SiVL to speed error location, analysis, and dispositioning

- Easily create automated experiments involving large numbers of measurement sites and model conditions with batched assessments and with a macro record and save feature
- Interactively create and manipulate layout patterns to explore advanced OPC, PSM, Off-Axis Illumination, and other wavefront engineering techniques
- Optimize process conditions for OPC by simultaneously evaluating and comparing OPC performance under different model conditions
- Evaluate the effectiveness of different RET strategies

SiVL Error Analysis

As with the Mask Synthesis tools, IC WorkBench and SiVL smoothly connect and interoperate to create a single, powerful environment for developing and running a Lithography Verification flow. As users sort, filter and evaluate errors using SiVL, IC WorkBench moves to the error locations and provides needed visual confirmation through display of the actual target and corrected pattern and simulation of the wafer image.

Production-Proven Technology

IC workbench is production-proven since the 180nm node is used for advanced 45nm technology and beyond at the world's leading semiconductor manufacturers.



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