



***Improving Design Turnaround Time
with In-Design Physical Verification***

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Company Structure



Wireless

Automotive, Consumer, Computer and Communication Infrastructure ("ACCI")

Industrial and Multisegment Sector ("IMS")

Major Product Lines

Home Entertainment & Displays

Computer & Communication Infrastructure

Automotive Products Group

Analog, Power and MEMS

Microcontrollers, Memories and Smartcards

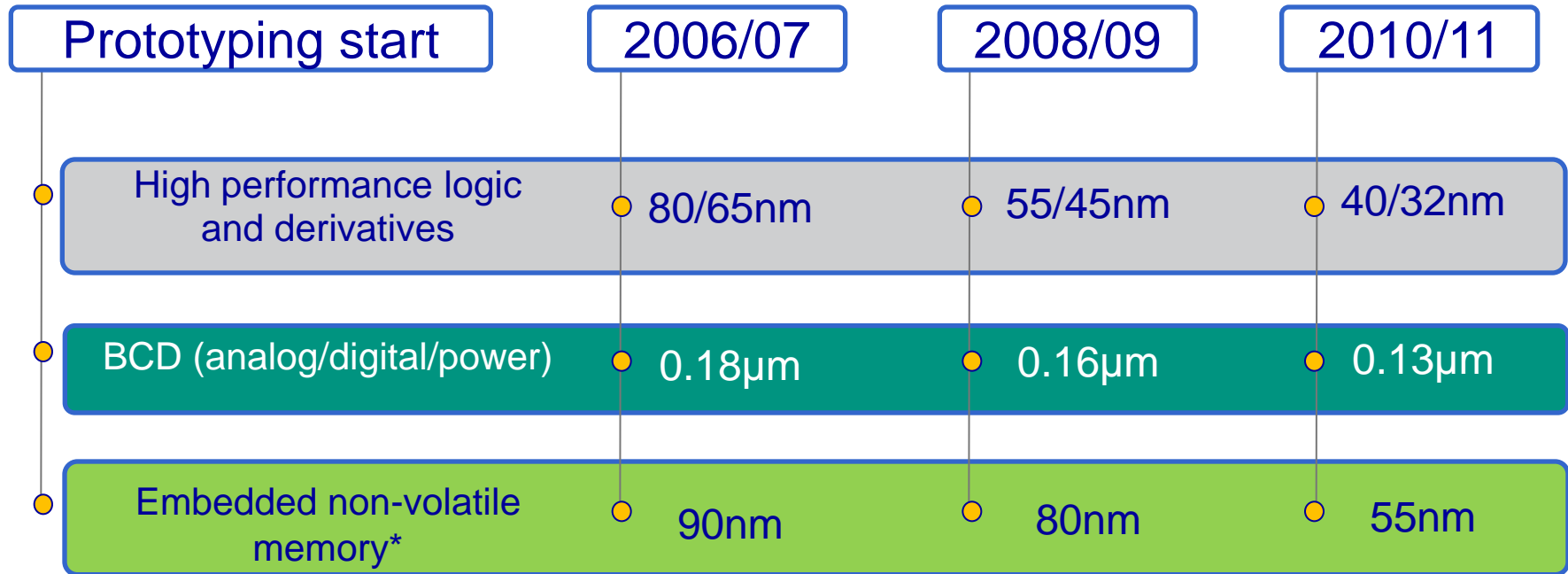
Products



Major Customers

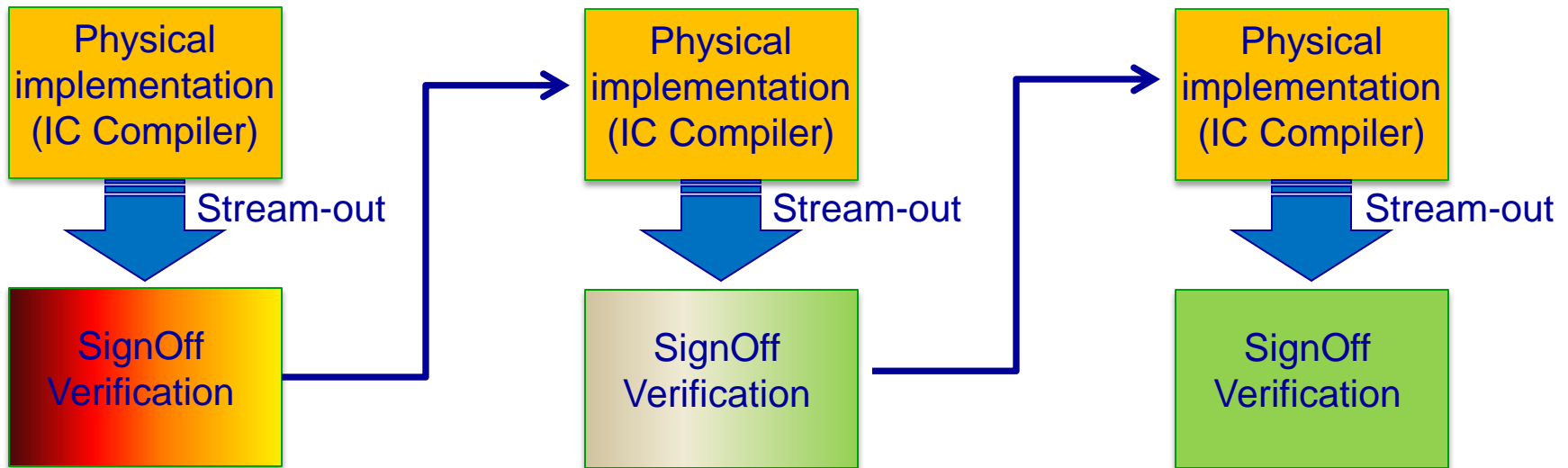


A Leading Portfolio of Technologies



* Logic with Embedded Memories

Traditional Flow: Implement-then-Verify



Incremental detection of:

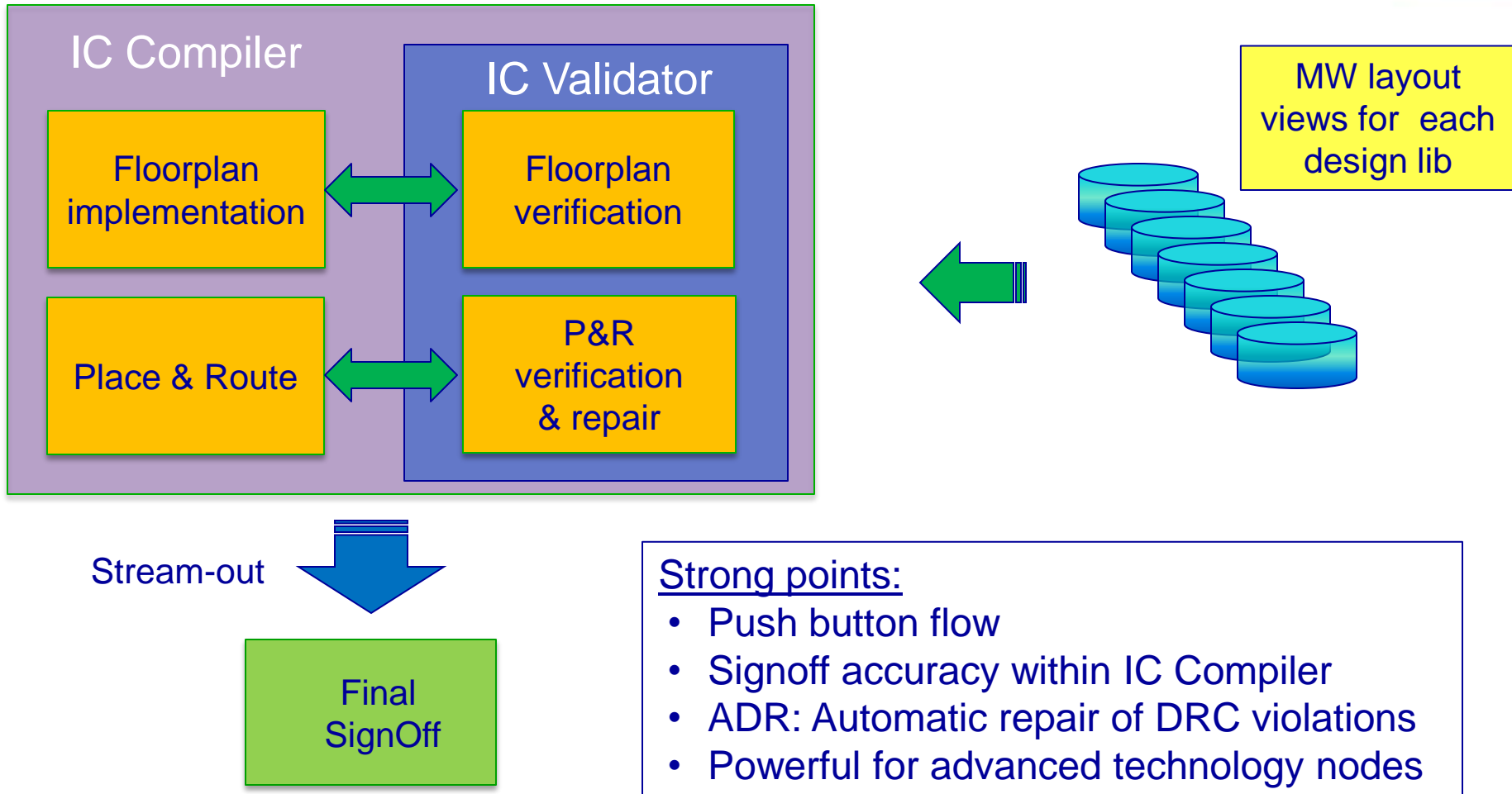
- Power grid DRC errors
- Wrong Cell Orientation
- Latch up errors
- Missing contacts
- Routing DRC errors

Flow limitations:

- Possible impact on floorplan
- Violations discovered late
- All fixes are manual
- Multiple stream-outs

Many Iterations Causing Up to 3 Week TAT Delay

In-Design Physical Verification (PV) Flow

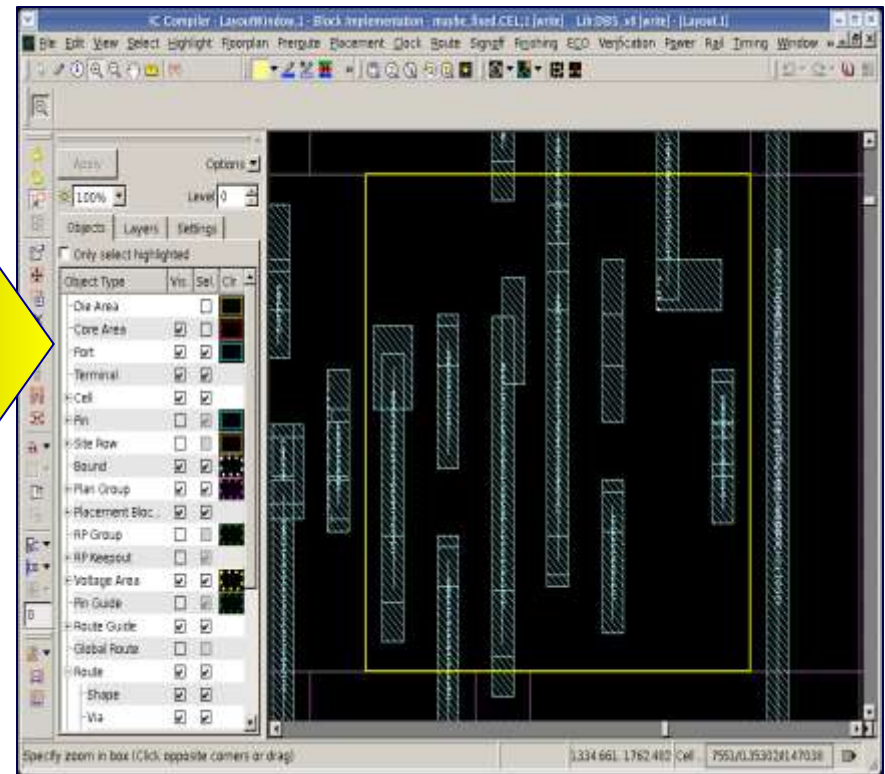
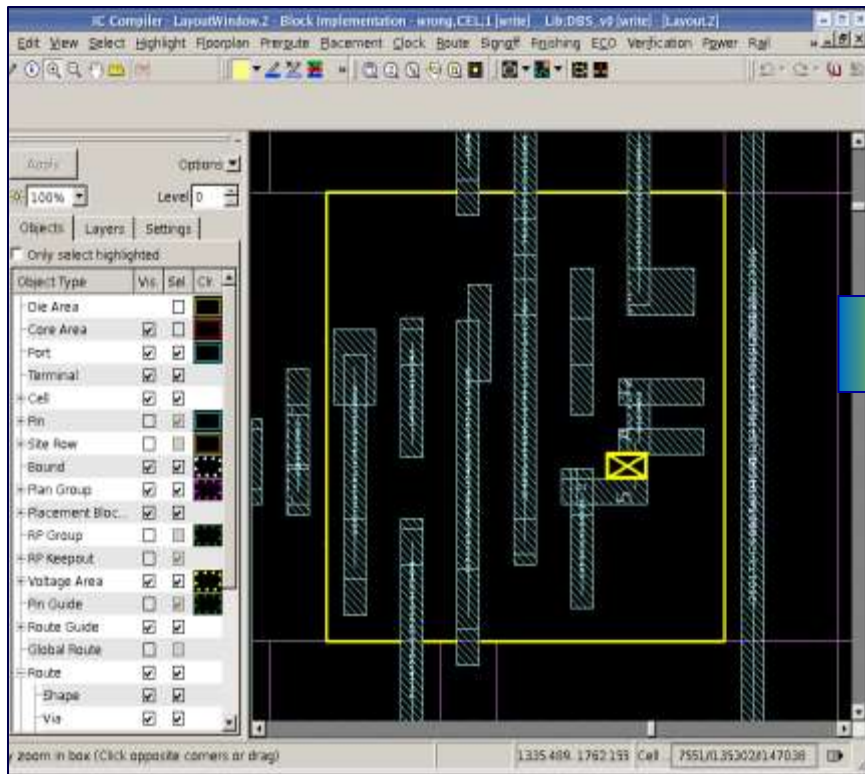


Qualified and Deployed In-Design PV at 65 & 40nm

Results: Automatic DRC Repair (ADR)



- Early 45nm 320K instance block
- Advanced spacing violation (corner-case rule)
- Automatically repaired 136 violations in 5 min (ZRoute time)

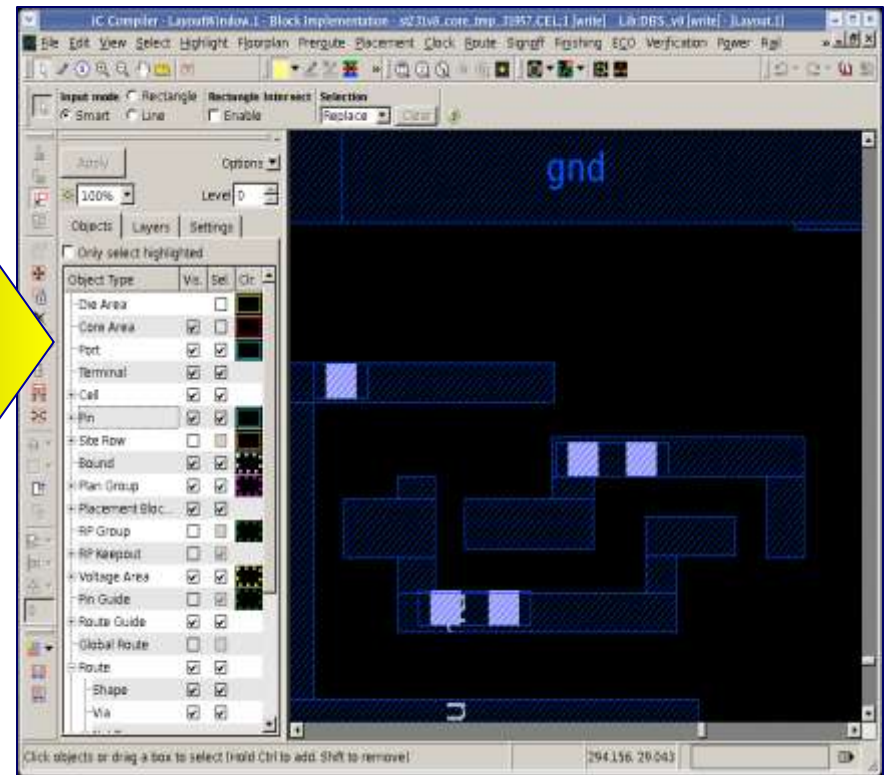
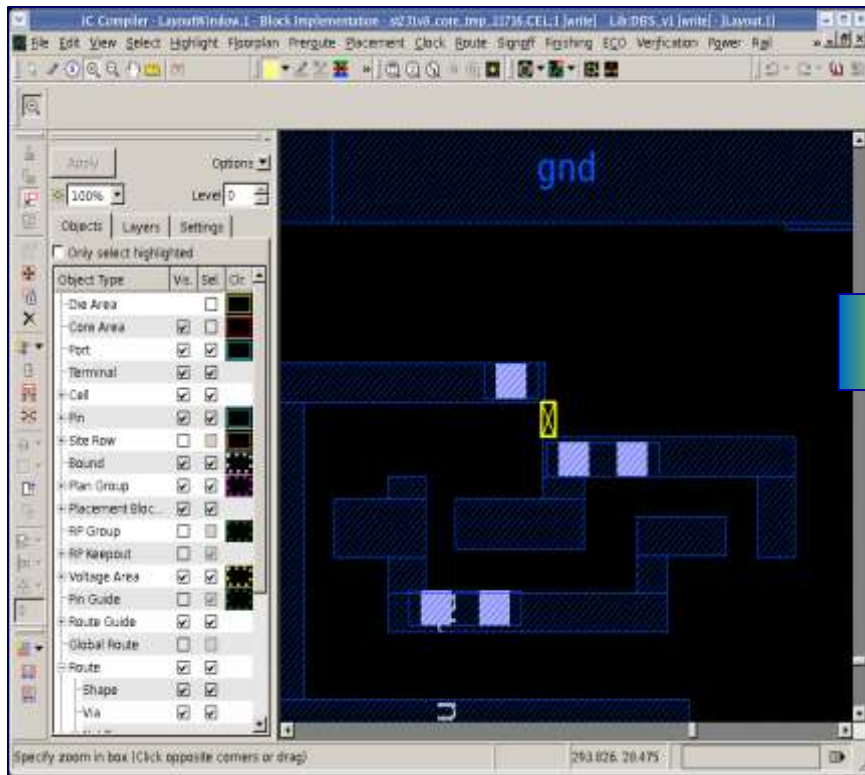


ADR: 100% DRC Repair Rate

Results: Automatic DRC Repair (ADR)

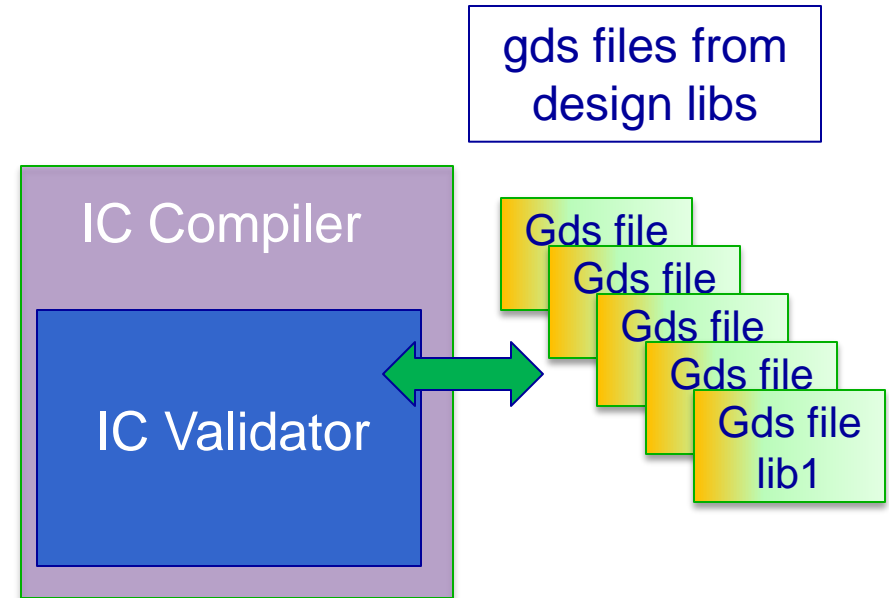


- Early 40nm 2M instance block
- End-of-line via enclosure violation (corner-case rule)
- Automatically repaired 340 violations in 35 min (ZRoute time)



ADR: DRC Clean in 35 Minutes

- Earlier Physical Verification on all layers:
 - Directly load library GDS files into ICV
 - Use actual GDS layers before IP MW layout Views are available
- Added to IC Compiler wish-list
 - Direct load of library gds files to avoid need for MW layout library views
 - Avoid coding of front end layers in technology file



Successfully tested on std cells designs

- **Benefits**
 - Improve predictability by ensuring design is DRC error free while constructing
 - Up to 3 weeks improved TAT by limiting the need of signoff re-spins
 - ADR: >90% automatic repair rate of corner-case DRC errors in minutes
- **Next steps**
 - 32nm qualification in ICCKit
 - On-demand GDSPMerge feature full qualification
 - Testing and qualification of more In-Design capabilities (pre-routing)

ST Deploying In-Design Physical Verification
in IC Compiler for 65, 45 and 32nm Designs