

# **TOSHIBA**

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## **Concurrent Hierarchical Design with IC Compiler Real Life Application on Mobile Multi-Media Processor**

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@45<sup>th</sup> Design Automation Conference**

# Agenda

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- **IC Compiler Deployment at Toshiba**
  - **Design Environment**
  - **Orion Design Kit**
- **Designing by Concurrent Hierarchical Methodology**
  - **Overview of Design Target**
  - **Challenges of Implementation**
  - **Concurrent Hierarchical Design Prototyping**
- **Summary and Expectations to Synopsys**

# IC Compiler Deployment at Toshiba

Customer

Over 30 Tapeouts In  
2007

ASSP

TC340C

Design methodology Develop.

Architecture

FAB

Circuit Tech.

Ohita, ...

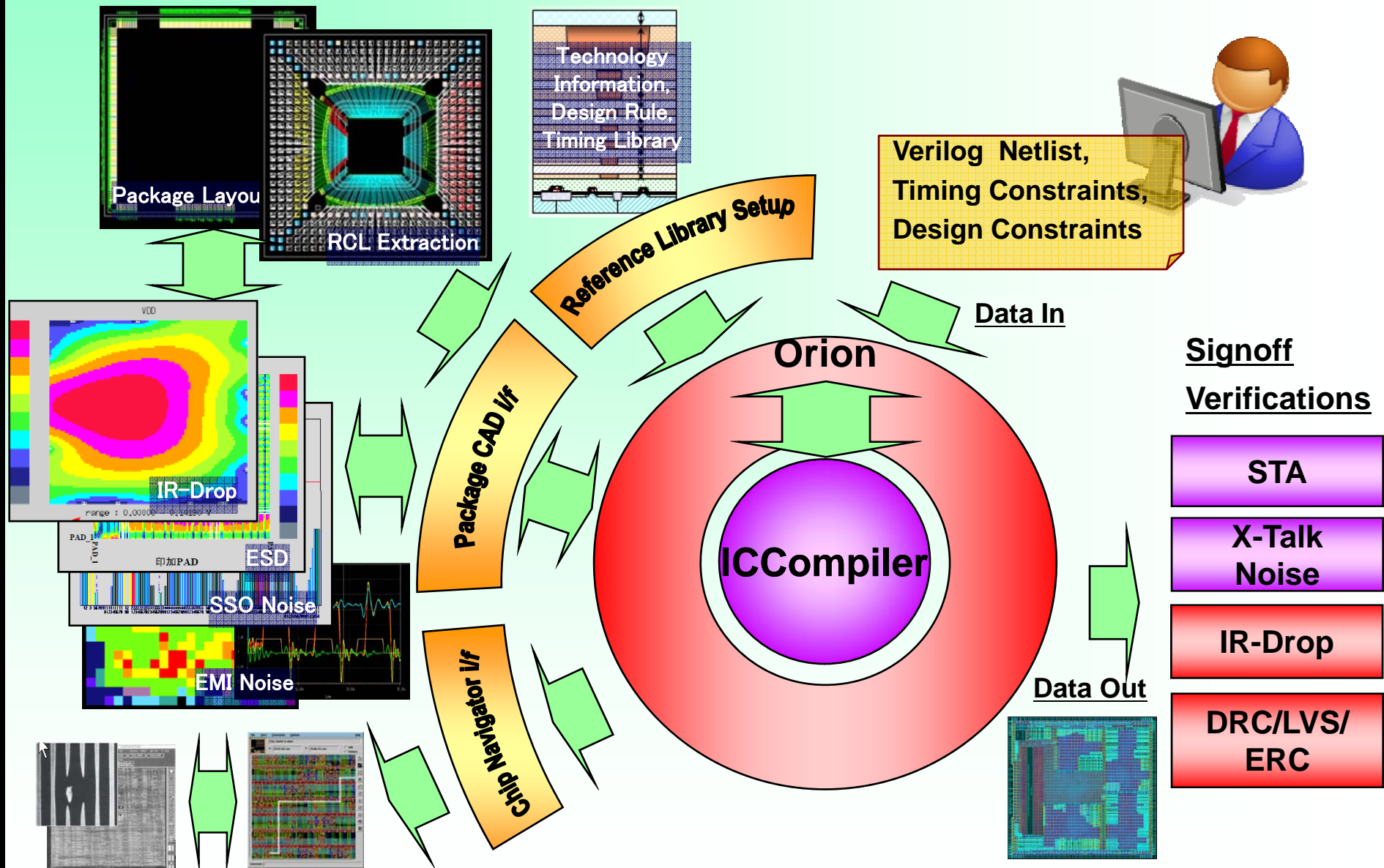
Design Kit

*Most Number of Tapeouts in 2007*

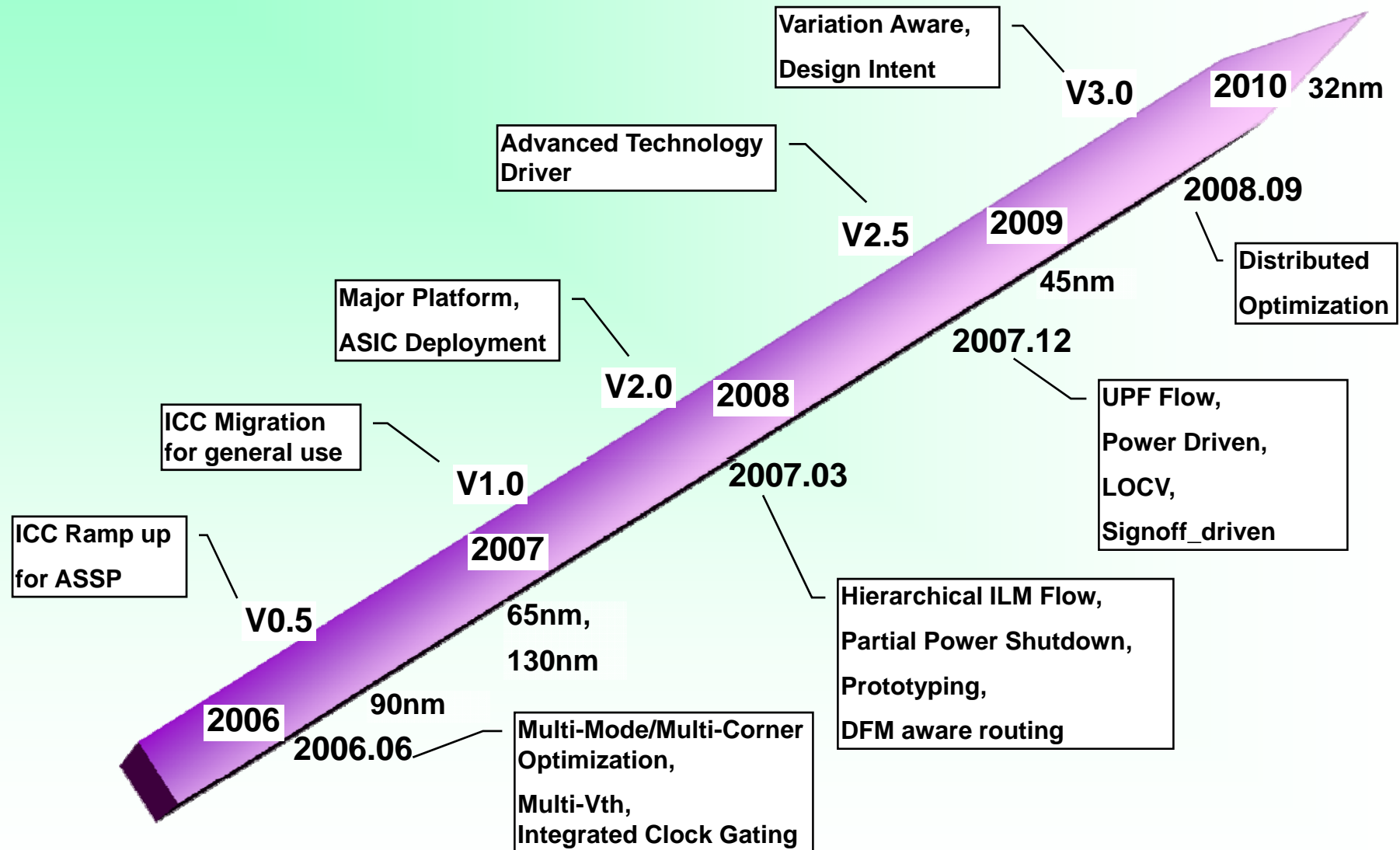
Synopsys R&D/CAE, Nihon Synopsys KK

STARC

# Design Environment in Toshiba



# Orion Design Kit Roadmap



# Overview of Design Target

## ■ Multi-media Engine for Mobile Phone

- ✓ High performance 3D graphics
- ✓ Audio/Video processing
- ✓ LCD controller

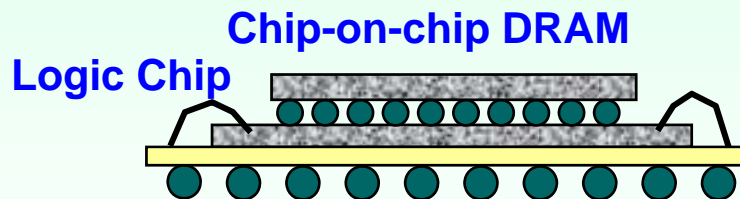
## ■ Chip-on-chip DRAM (SiP)

- ✓ Variable memory size by changing DRAM size.

## ■ 6M Gates of random logic

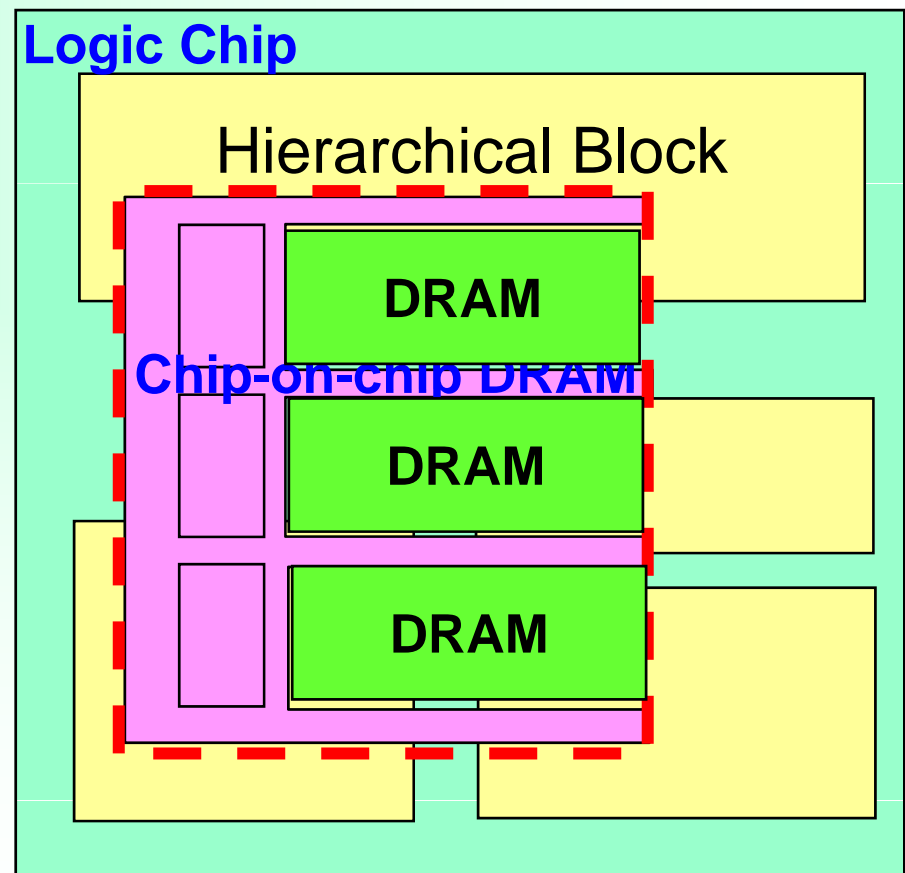
## ■ 90nm technology

## ■ 180MHz



### Chip-on-chip DRAM

- Stacked inside a package
- Connected by solder bump array.



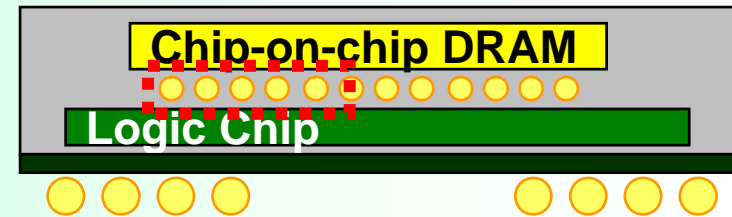
# Challenges of Implementation (1/2)

## ■ Modeling of DRAM

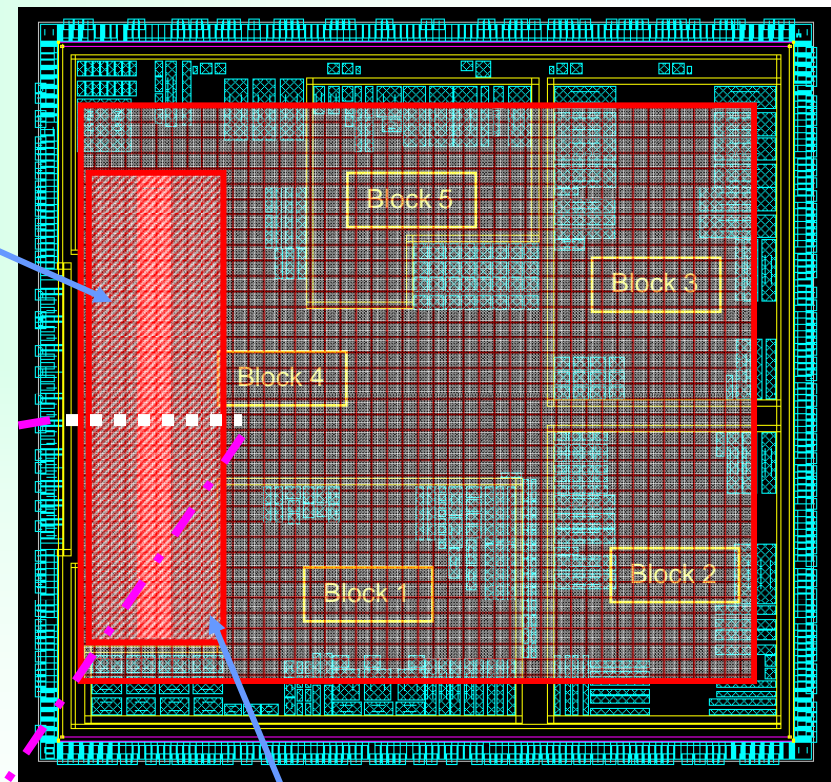
- Representing as a macro cell correspond to i/f I/O block.
- Characterizing timing as ETM model by PrimeTime.

## ■ Layout Constraint

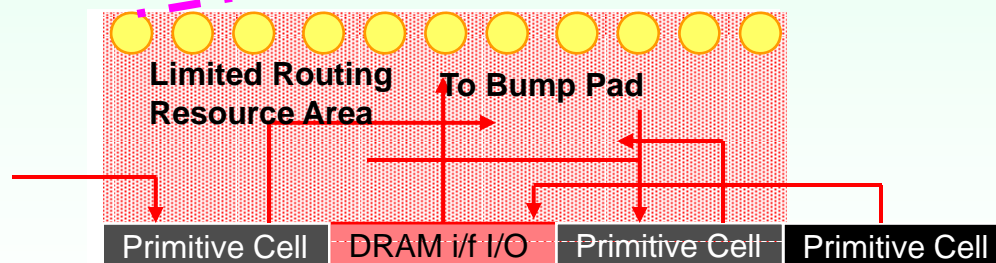
- Limited routing resource under bump PAD area.



i/f I/O

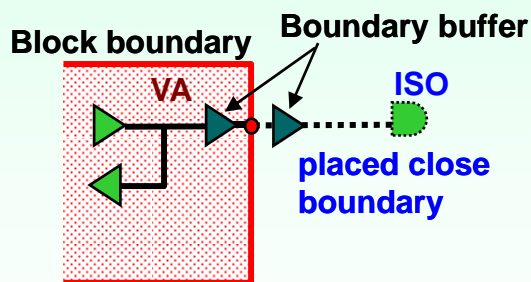
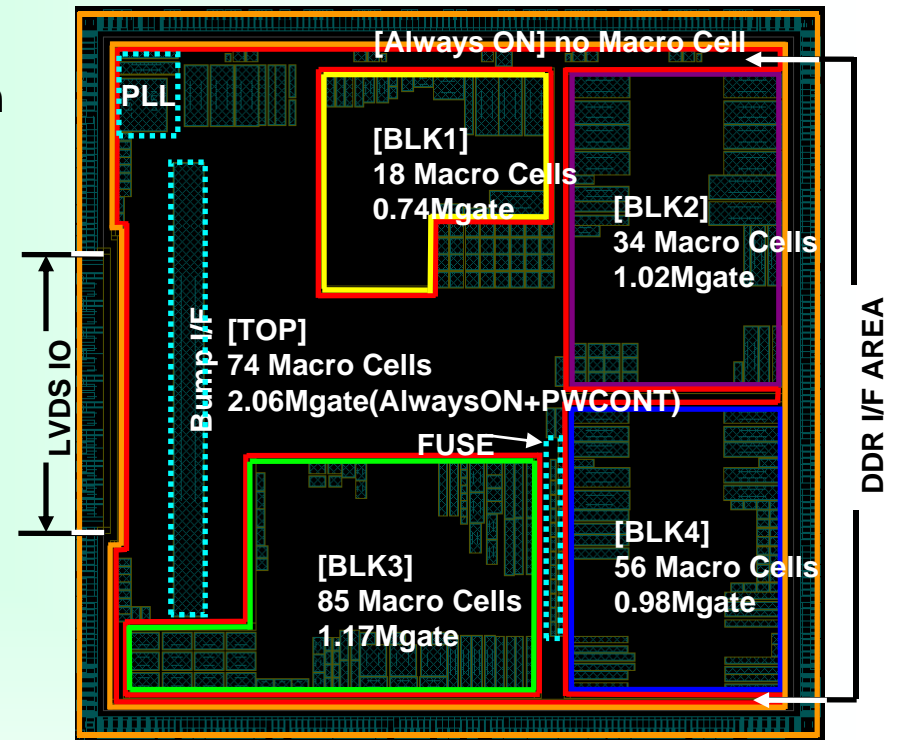


Bump PAD



# Challenges of Implementation (2/2)

- Multiple power domains for shutdown
  - ✓ 4 Power domains are in a power domain
  - ✓ Nested power domain
- Automatic ISO cells insertion
- Hierarchical design methodology
  - ✓ 4 ILMs on Top
  - ✓ L-shaped Blocks
- Multiple-Mode
  - ✓ Concurrent MC/MM Optimization

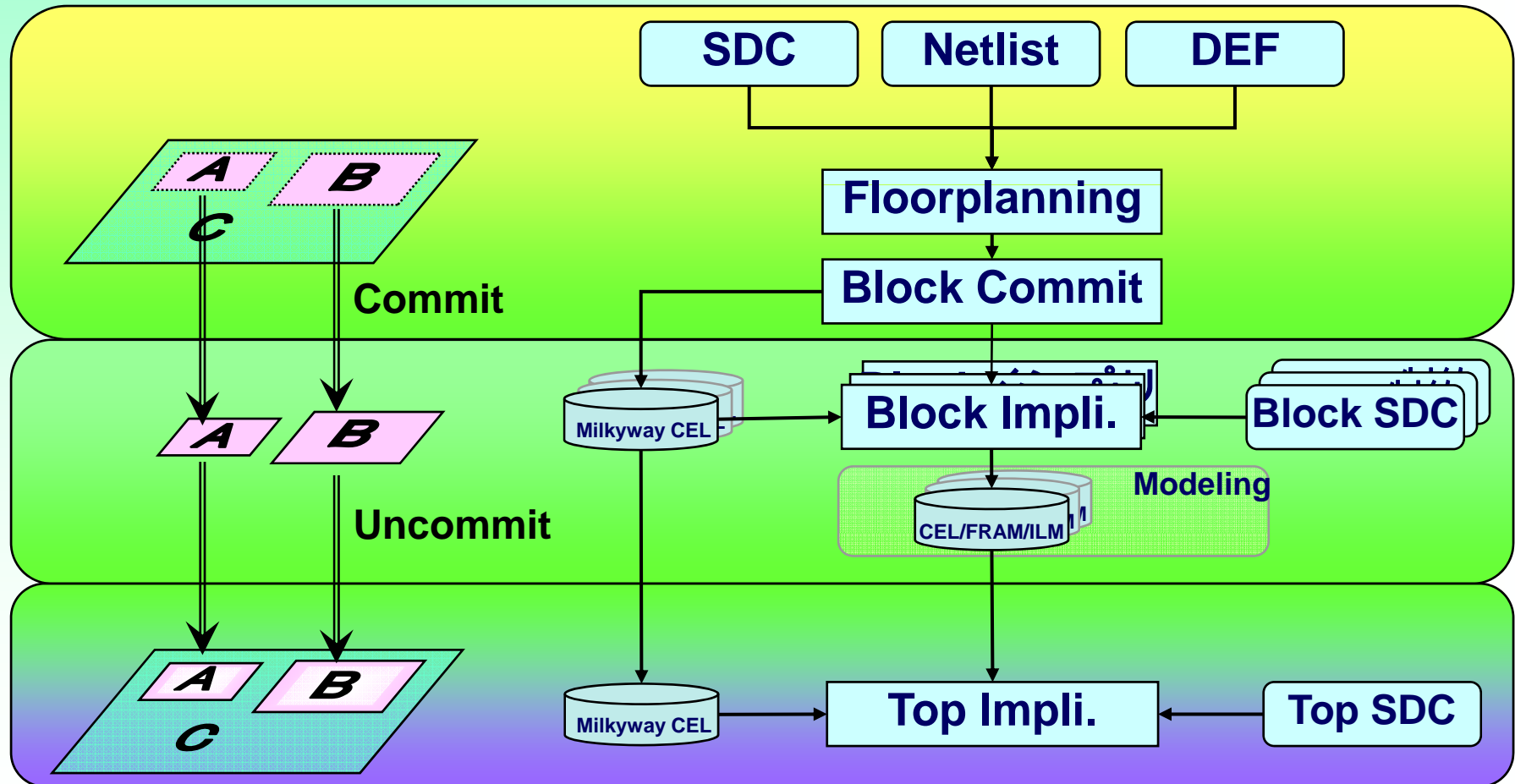


To Separate Block and Top

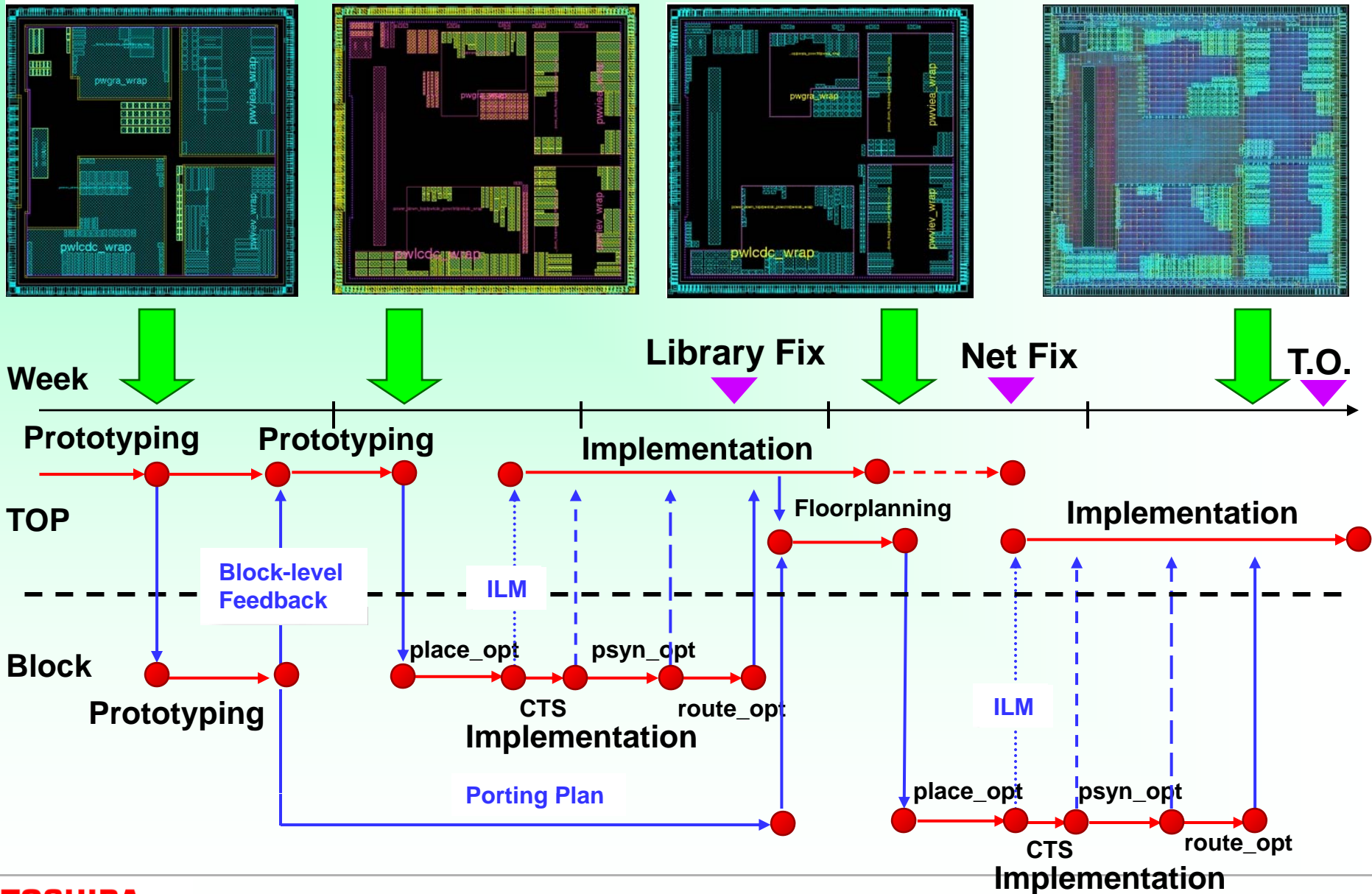
	Always ON	TOP	BLK3	BLK2	BLK4	BLK1	DRAM
Mode1	ON	ON	ON	ON	ON	ON	ON
Mode2	ON	ON	ON	OFF	OFF	OFF	ON
Mode3	ON	ON	OFF	ON	OFF	OFF	ON
Mode4	ON	OFF	OFF	OFF	OFF	OFF	OFF

# Hierarchical-ILM Flow in IC Compiler

- Each power domain corresponds to hierarchical block.
- Blocks are characterized physical ILM and fabricated on Top.

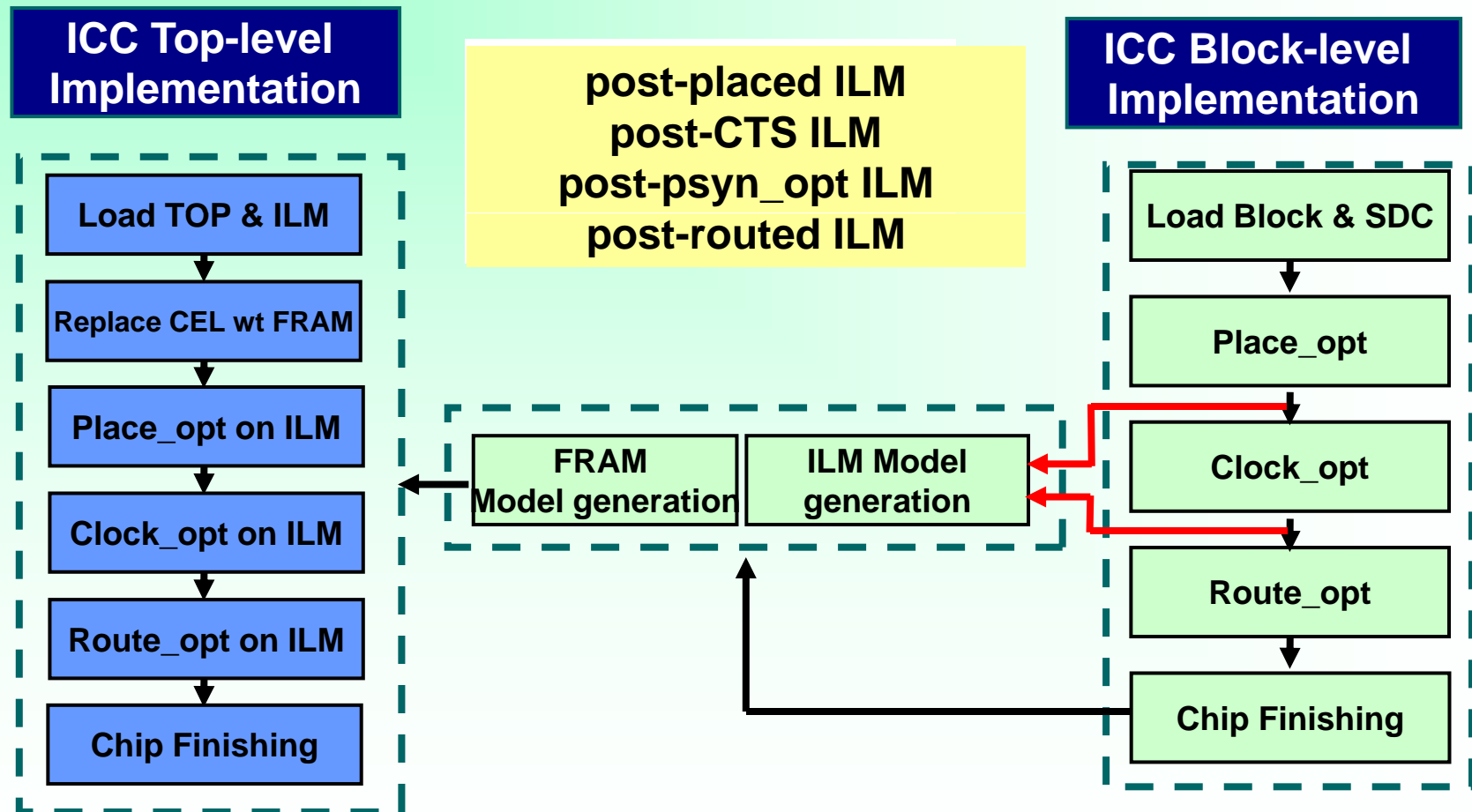


# Concurrent Hierarchical Design Prototyping



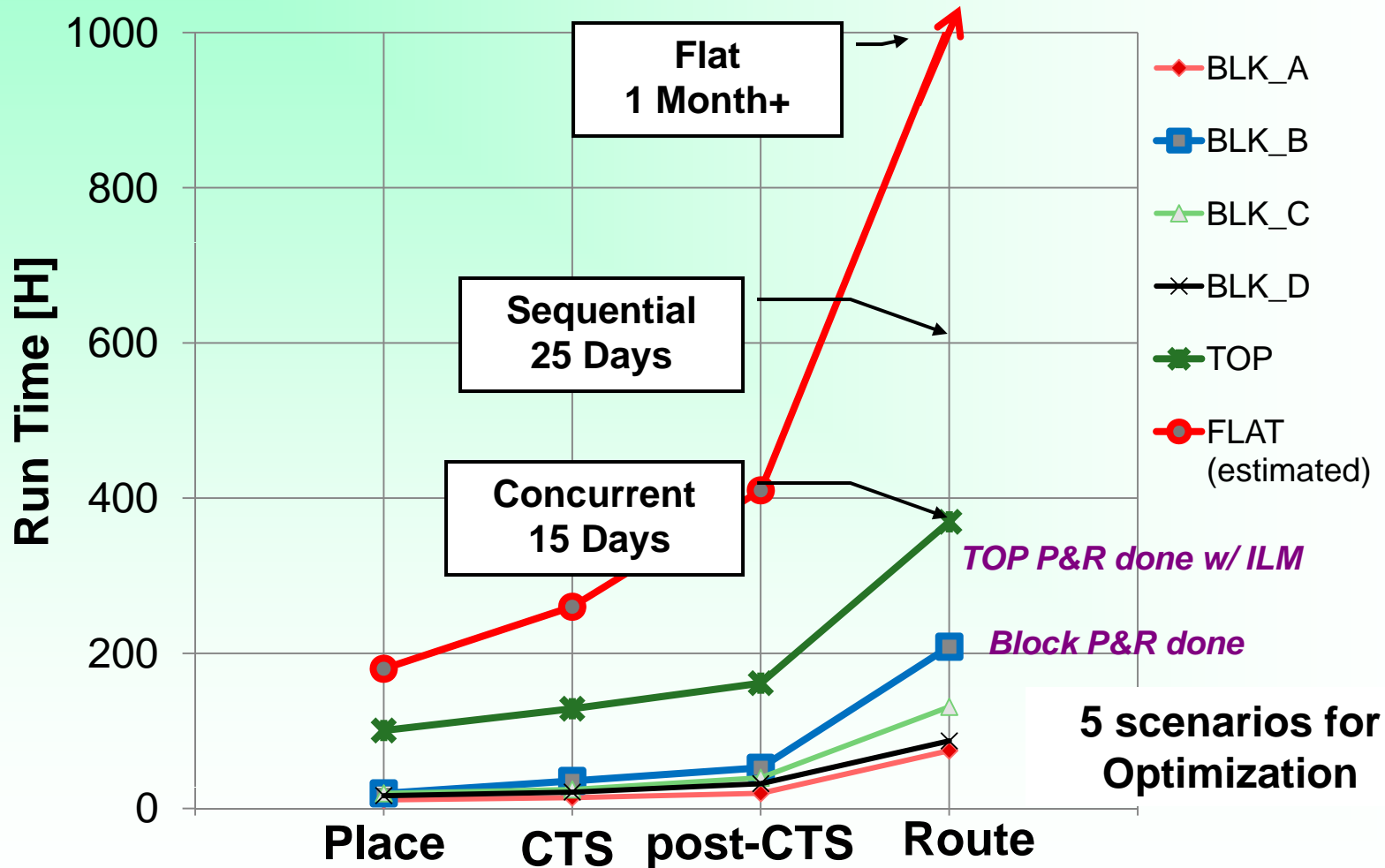
# Concurrent Design of Top and Blocks

- Physical and timing modeling capability realizes concurrent feasibility exploration.



# Design TAT Improvement

- Concurrent hierarchical design methodology reduced total design TAT by 40%.



# Summary and Expectation to Synopsys

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- IC Compiler has been widely deployed at Toshiba since 2007
  - ✓ We had over 30 tapeouts in 2007.
- Toshiba's Orion design kit supports a full IC Compiler design methodology, including a hierarchical, and power shutdown.
- We significantly reduced design TAT on Mobile Multi-Media application by using concurrent hierarchical design methodology.
- We are continuing successful collaboration with Synopsys including several 45nm design projects now.
- We would like to see further TAT improvement and even tighter correlation among IC Compiler, STAR-RCXT, and PrimeTime-SI.

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