

Automatic Block Size Reduction

With IC Compiler
MinChip Technology



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Agenda

- ▣ About STMicroelectronics
- ▣ Implementation Challenge and Current Solution
- ▣ MinChip - Automated Die Size Reduction
- ▣ MinChip Results
- ▣ Summary and Next Steps



About STMicroelectronics

STMicroelectronics is one of the world's largest semiconductor companies with net revenues of US\$10.0 billion in 2007.



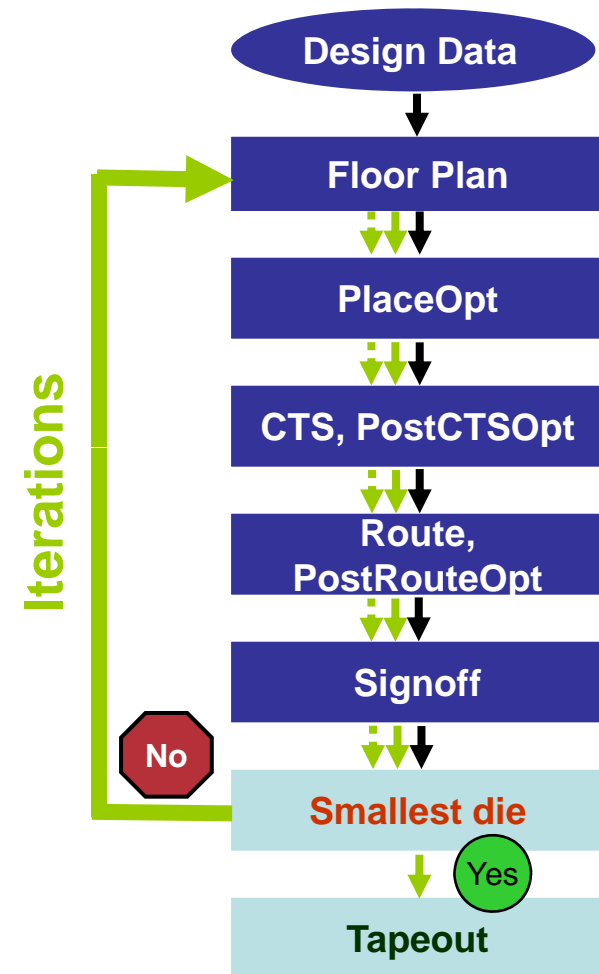
Technology R&D – TestChip Certification Design Flows

- ▣ TR&D - TCD Team Works on Library, flow compliance, advance Silicon qualification vehicles, IP implementations and Methodologies.
- ▣ Two kinds of Implementations
 - ▣ for new architectures having no prior history
 - ▣ Re-spin of existing IP's for optimization



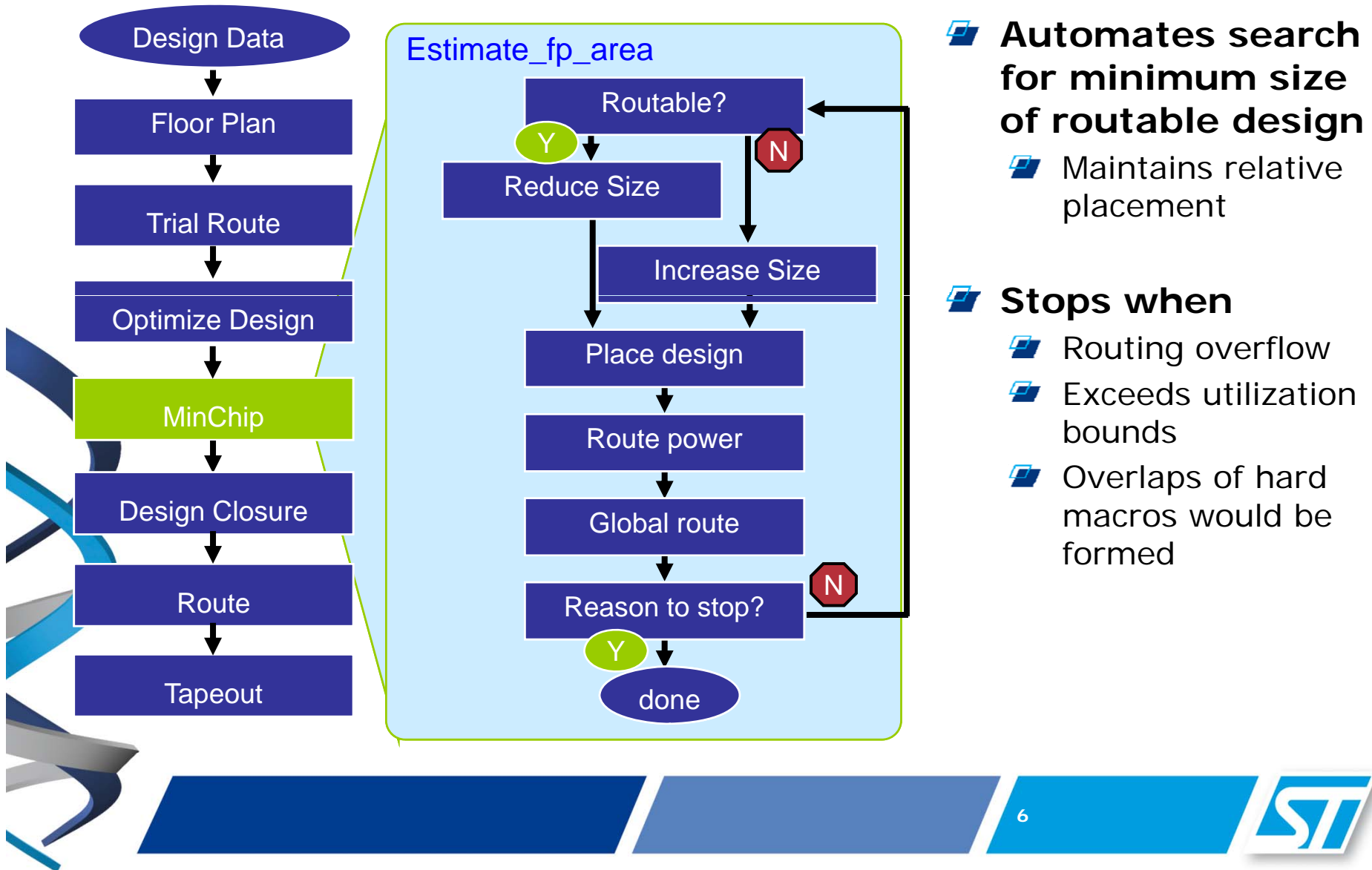
Implementation Challenge and Current Solution

- One of the challenges
 - “**minimum**” die size in “**minimum**” amount of time
- Problems with current solution
 - Manual, iterative
 - Unpredictable time to results
 - Depends on designer’s expertise



MinChip Automated Die Size Reduction

Minimum Die Size With Predictable TaT



MinChip Results (1/2)



Digital Consumer Application

- 65nm, 250 MHz
- 350K Cells, 100 Macros

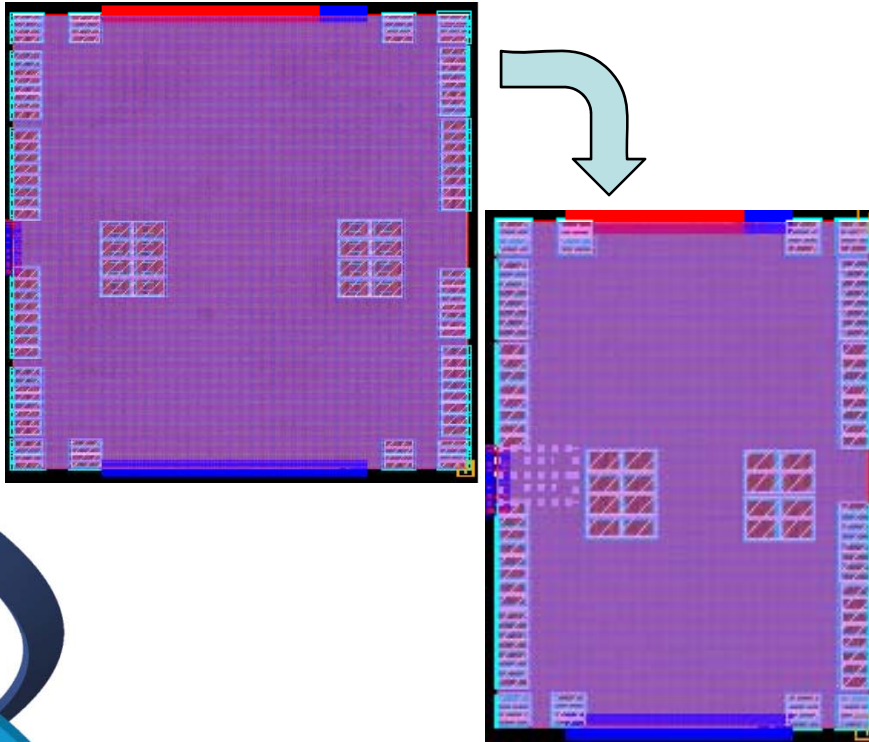
New Implementation

- Expected 2-3 days TaT

**23% Shrink
In 4 Hours**

Metrics	Initial	MinChip
Area	6.9mm ²	5.3mm ²
Utilization	~60%	~80%

MinChip Results (2/2)



Digital Consumer Application

- 2nd release of Netlist
- 520K Cells, 112 Macros

MinChip Implementation




- Allowed aspect ratio to change

**27% Shrink
In 6 Hours**




Metrics	Initial	MinChip
Area	6.9mm ²	5mm ²
Utilization	~72%	~88%

Summary and Future Steps

Summary

-  MinChip removes guesswork – delivers minimum area in minimum time
-  Removes need for manual intervention, costly iterations, unpredictable TaT
-  Good starting point for further refinement of floorplan

Future Enhancements

-  Hierarchical MinChip
-  Integration of MinChip in Prototyping flow
-  Better user feedback when MinChip cannot shrink any more (e.g. save the previous view)

Next Steps

-  Usage of MinChip for all new designs on Synopsys platform