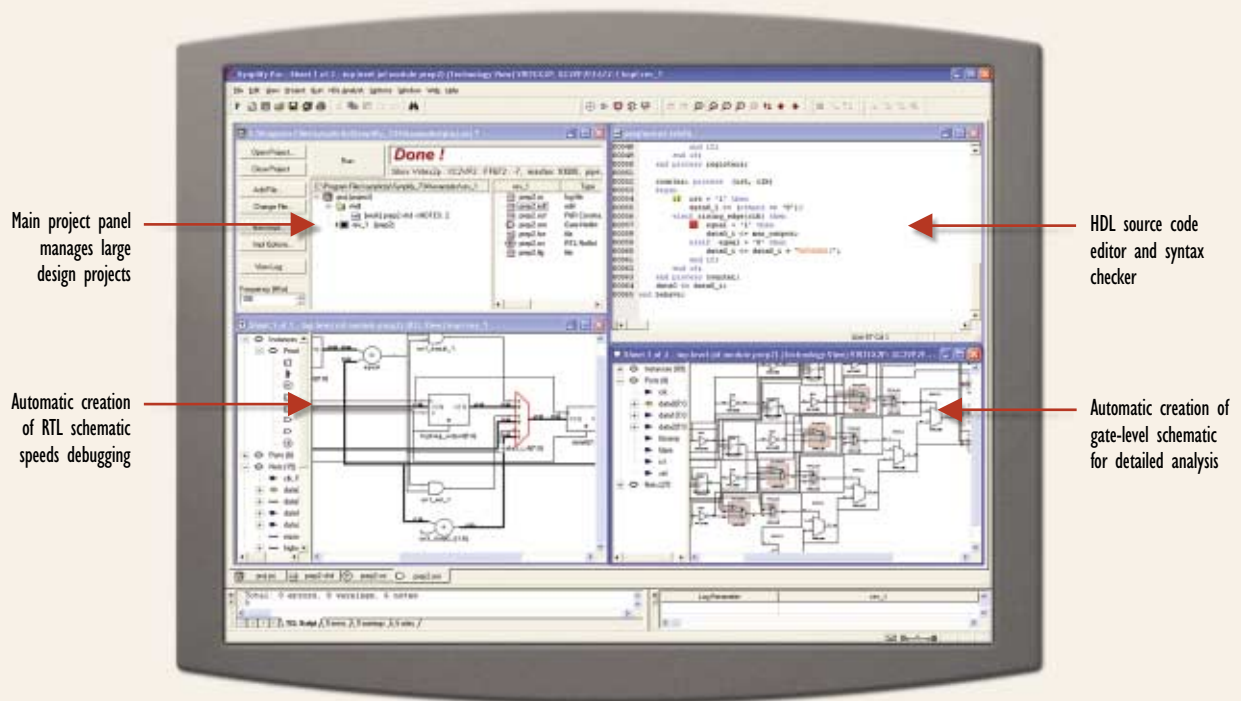


HDL Analyst®

A Powerful Graphical HDL Code Analysis Environment
for Verilog and VHDL Designers



Main project panel
manages large
design projects

Automatic creation
of RTL schematic
speeds debugging

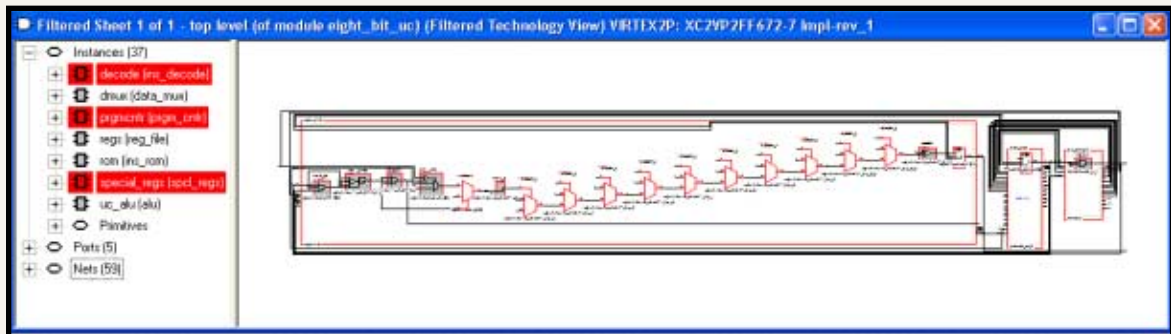
HDL source code
editor and syntax
checker

Automatic creation of
gate-level schematic
for detailed analysis

The HDL Analyst environment instantly generates an RTL block diagram from HDL code

While HDLs improve system performance and designer's productivity, specific coding styles may create undesired or inefficient logic (e.g., an asynchronous load when a synchronous load is required or implied latches). Only the designer will know whether these circuits are required. This is where the HDL Analyst environment comes in. By letting you instantly see, in graphical form, both a high-level block diagram and a technology-specific, gate-level schematic, you'll know exactly where further optimization is possible and link it directly back to your HDL source to make the changes where they belong — in the HDL source code.

With three different views of your design available, you can choose the best view for the task at hand and cross-probe between all three. HDL Analyst tool's easy to read RTL schematic displays high-level functions like Finite State Machines (FSM) multipliers, adders, and memories. This allows the designer to analyze high-level functionality without all the details, making it easier to find potential problems. Critical paths within the design may be highlighted with timing information annotated on the schematic. The HDL Analyst analysis and debugging environment's unique "filter schematic" command creates a custom schematic showing only the critical path (or other selected logic) in a single, easy-to-read schematic viewer.



Filtered schematic showing critical path of design

Benefits both new and experienced designers

The HDL Analyst tool is essential for high-density FPGA and CPLD designs. For designers new to Verilog or VHDL, it provides easy-to-read block diagrams and schematics with direct links to the HDL code from which they were created. For experienced designers, the HDL Analyst environment displays post-mapped, gate-level schematics for detailed analysis and refinement. It is easy for you to find and analyze critical paths and cross-probe back to the HDL source code, thereby simplifying and dramatically shortening the debug cycle while improving the quality of the HDL code.

Configurations

HDL Analyst is an option to the Synplify® product and a standard feature in the Synplify pro® product.



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