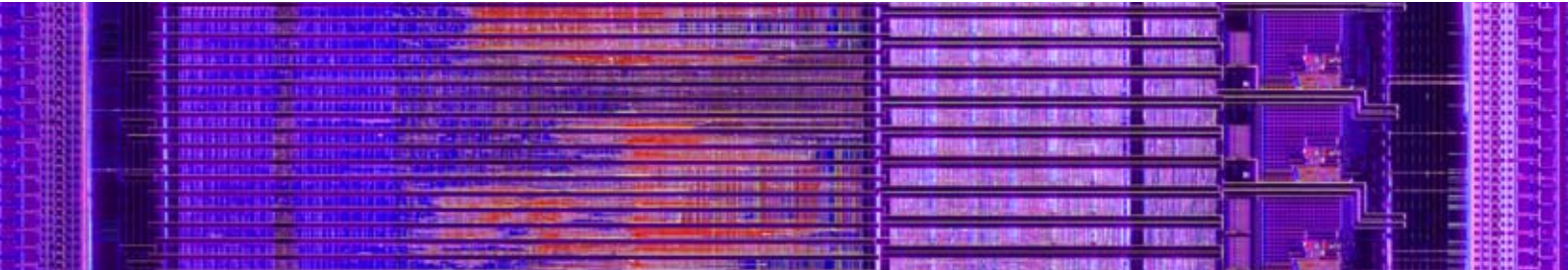


# Tapeout Assistance

Dedicated expertise to resolve tapeout bottlenecks



The path to a successful tapeout is often lined with challenges that only become critical late in the design cycle. Some of these bottlenecks are predictable, others are not. In virtually all cases, delays in these final stages of the project are highly stressful and equally visible, as the project team pushes hard towards a successful tapeout.

Synopsys Tapeout Assistance services help design teams in this critical stage of their project cycles. Physical design consultants provide dedicated support to help mitigate technical risks and address design and tools issues that are hindering tapeout. The Synopsys on-site staff is backed by a worldwide network of consulting, CAE and R&D resources.

Synopsys consultants understand the issues that most commonly impede progress in the physical design phase – from constraints management to power distribution and clocking to DRC/LVS integration issues – and possess the expertise and experience to develop practical action plans with your design team. While the primary objective is completing your current design project, our Tapeout Assistance services often lead to flow and methodology enhancements as well as knowledge transfer that improve your team's readiness for the next tapeout.

### At-a-Glance

- Specialists help to quickly resolve design and tool bottlenecks through tapeout
- Implement new methodologies as needed
- Dedicated physical design assistance when you need it most

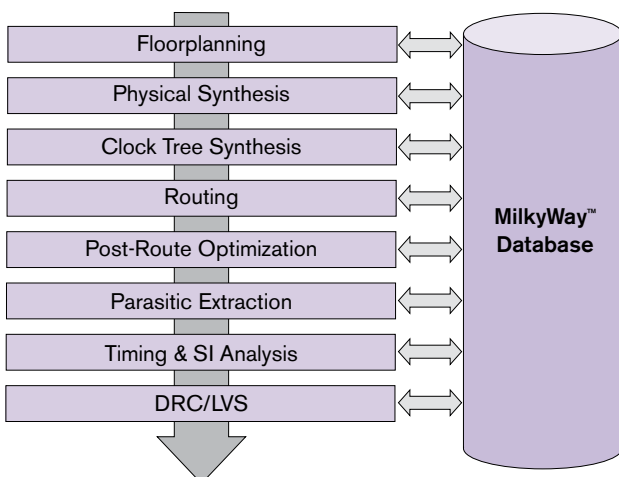


Figure 1. Specialists assist your project team in the most critical phases of physical design to facilitate tapeout.

### Customer Case Study

To mitigate their tapeout risks and achieve critical schedule milestones, a global leader in wireless chipsets turned to Synopsys for assistance with a complex multi-channel design incorporating 40 clock domains. Synopsys consultants joined the customer's design team to ensure cell utilization was optimized and the highly complex clocking architecture was correctly implemented. Synopsys' onsite support in the final weeks of tapeout focused on synthesis, clock-tree balancing and latency control to ensure timing closure was achieved and performance targets were met. Timing closure was achieved across both synchronous and asynchronous paths. The CTS methodology and scripts developed in the course of the project were adopted and applied to several subsequent designs.

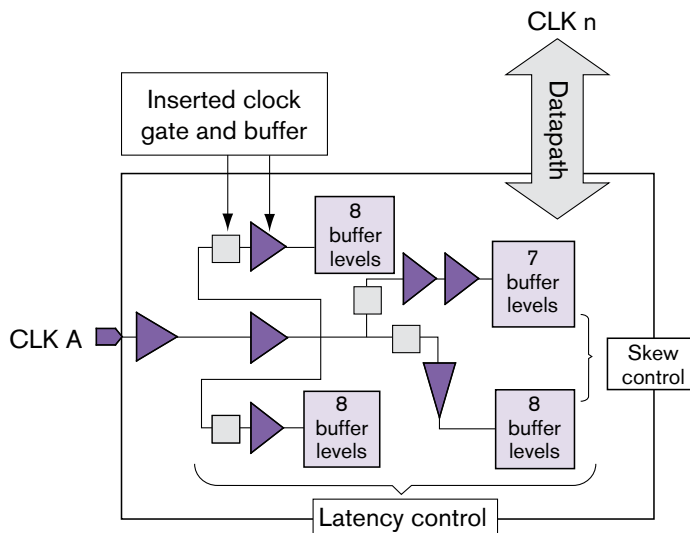


Figure 2. Clock buffers and clock gates were inserted and resized to meet skew and latency goals as well as reduce power. This enabled the design team to achieve timing closure across all synchronous and asynchronous clock domains.

Synopsys consultants deliver tool and implementation assistance in important areas that often cause delays in the latter stages of a design project, including:

- Constraints management at block and chip level
  - Floorplan macro placement optimization
  - Power optimization
    - Clock gating
    - Multi- $V_{TH}$  optimization and placement
    - Multi- $V_{DD}$ , MTCMOS
  - Clock tree placement and balancing
  - DFT implementation including 3rd-party IP integration
  - ATPG with more complete fault models
  - Timing closure with post-route SI optimization analysis and repair
- Configuration tech file modifications for routing
  - Scan compression
  - Multi-corner, multi-mode (MCM) optimization and analysis
  - Rail analysis to address IR drop and electromigration
  - Chip finishing, including metal fill, spare-cell and Dcap insertion
  - LVS and DRC on sub-blocks and top-level
  - Recommend and implement flow and methodology enhancements, including SI-aware, power-area and yield-aware place and route

Design Description	Process	Gate Count	Clock Freq	Primary Area of Assistance
Wireless phone chipset	90nm	13M	200MHz	STA/SI analysis
DSP-based broadband	65nm	11M	1GHz	Timing closure
Video graphics controller	180nm	4M	162MHz	Constraints, STA, Clock routing
Mobile computing	90nm	500K	600MHz	Scan insertion, STA
HDTV graphics	130nm	5M	250MHz	DFT, STA/SI
DSP-based consumer chip	130nm	1.5M	240MHz	Timing closure, scan insertion
Networking chip	90nm	11M	250MHz	P&R
PCI-Express switch	130nm	6M	375MHz	Floorplan, CTS, placement
40G optical switch	130nm	1M	700MHz	Top level routing, timing closure
Graphics controller	90nm	3.5M	600MHz	STA/SI analysis, P&R
Computing application	90nm	3M	667MHz	P&R
CPU core	130nm	880K	230MHz	P&R
Baseband processor	130nm	1M	125MHz	Timing closure

Table 1. Sample of recent Synopsys-assisted customer tapeouts.

Synopsys assists customers in achieving more than a hundred successful tapeouts every year. These designs span a broad spectrum of application areas, chip sizes and complexity, and process nodes. This extensive resume enables our consultants to draw upon valuable experience of the issues and solutions associated with getting a chip to tapeout, helping you to avoid costly delays.

**For more information about Synopsys' complete portfolio of consulting and design services, visit [www.synopsys.com/sps](http://www.synopsys.com/sps) or contact your local Synopsys sales representative.**

**For more information about Galaxy™ tools and tool flows, visit [www.synopsys.com/products/solutions/galaxy\\_platform.html](http://www.synopsys.com/products/solutions/galaxy_platform.html).**

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