An Analytical Study on the Role of Thermal TSVs in a 3DIC Chip Stack

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Abstract— **This paper analyzes the effectiveness of the use of thermal TSVs in lowering the overall average temperature of a 3D IC vertical stack as well as the impact and significance of thermal TSV count on the vertical and lateral thermal gradients in the stack for a given set of initial boundary conditions. A set of simulations were carried out using a 3DIC compact thermal model simulator on a multi-tier multi-die 3DIC design to access these effects of thermal TSVs.**

Keywords - 3DIC, TSV (through silicon vias), thermal simulation

I. INTRODUCTION

Via-first / Via-early TSV based 3D IC is gaining momentum as an optimal way of realizing the vision of "More than Moore" as it offers the desired benefits of higher performance (increased bandwidth) and lower dynamic power - due to shorter interconnect and weaker IO buffers- as well as realizing compact heterogeneous integration of analog, digital, MEMS, and RF applications where each is designed in its optimal technology node.

TSV fabrication includes thinning of the wafer substrate from a nominal 500um to a thickness of sub-60 um. That, plus the added proximity of interacting heat sources due to vertical stacking of dies results in increased power densities that could be detrimental to the performance as well as the reliability of the 3D IC realized system.

Various studies indicate that current heat convection capability of a system does not scale with stacking. Thus operating temperatures and thermal gradients are most likely higher in 3D ICs than in their single die configurations. Thus the need for accurate thermal analysis and for thermally assisted 3D IC design has lately accelerated [1-6, 8-9].

For 3D IC thermal simulation to be accurate it is imperative to consider the whole system including the package and the stack of dies at once rather than iteratively simulating one die at a time as it eliminates the need of artificial initial thermal boundary conditions for each die and the need for a large number of iterations. It also results in a smaller run time and more credible results.

The introduction of Thermal TSVs is one way to assist in reducing a 3D IC stack's maximum temperature and thermal intra-die and across the stack gradients [7-10]. It has been reported that by carefully planning thermal vias in a 3D IC the maximum as well as the minimum temperatures were simultaneously significantly reduced [7,8,10]. Another proposition for managing the thermal profile of a 3D IC stack is engaging in thermally driven placement – not an easy task given individual chips' placement constraints and the need of simultaneous knowledge of thermal profiles of the chips to be stacked.

Considering the fact that thermal TSVs consume valuable real estate on a die in area and in routing congestion cost sufficient qualitative and quantitative understanding of its role is mandatory. Our goal from this work was to quantify the role of thermal TSVs in 3DIC design and the scope of benefits their presence have on reducing hotspots and steep thermal gradients. Towards that end we constructed a comprehensive test case for simulation composed of a stack that included multi-tiers, pumps, across die thermal TSVs, and package. We also used a data-calibrated thermal simulator

In the next section (II) we will have a brief theoretical exploration of the role of thermal TSVs. In section III we will present our compact thermal simulation flow for 3D IC. In section IV we present the experimental setup of our simulations of thermal TSV effects as well as the simulation results. We summarize and conclude in section V.

II. ROLE OF THERMAL TSVS IN 3D IC

In order to better understand TSVs' role in the heat transfer process in 3D IC it is helpful to establish the analogy between heat transfer and electrical circuits. In fact several numerical thermal simulators use this analogy to perform their thermal analysis [3,4,11]. A heat source is analogous to a current source. Thermal resistance is analogous to electric resistance. Temperature gradient is analogous to electric potential (voltage) in circuits. Therefore the heat transfer process in a 3D IC stack can be simplified as follows:

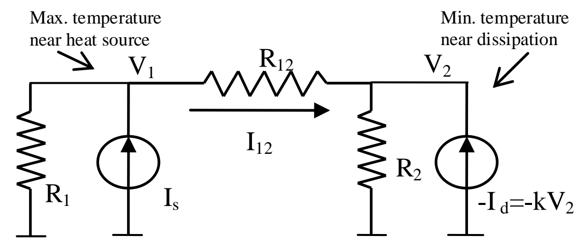

Figure 1. Circuit analogy of a 3D IC stack heat transfer.

The current source I_s in the circuit represents the total heat generated from the heat sources. It constitutes the total power consumption of a 3D IC design. The current source I_d drains current from the circuit representing heat dissipation. Heat dissipation is happening only at the stack interfaces to its environment and is described by HTC (heat transfer coefficient) of the stack surface. By definition, $HTC=\Delta Q/(A*\Delta T*\Delta t)$. Hence the dissipated heat quantity ΔQ is

proportional to HTC and to the heat transfer surface. Heat sink design can effectively improve heat dissipation mainly because it increases the effective heat transfer area. The dissipated heat ΔQ is also proportional to the temperature gradient between the dissipation surface and the ambient temperature. Therefore, this current source I_d is described as a voltage controlled current source in the circuit (Figure 1), $I_d = kV_2$. Also, note that in the same figure circuit ground represents the ambient temperature. Usually the maximum temperature in a 3D IC stack is located near the heat sources represented by V_1 in the circuit (Figure 1). The minimum temperature is located near the dissipation surface connected to the heat sink. It is represented by V_2 in the circuit (Figure 1). Hence we obtain the following equation for heat transfer:

$$\begin{cases} \dfrac{V_1 - V_2}{R_{12}} + \dfrac{V_1}{R_1} = I_s \\ \dfrac{V_1 - V_2}{R_{12}} - \dfrac{V_2}{R_2} = I_d = kV_2 \end{cases}$$

After a series of derivations, the above 2 equations are equivalent to:

$$\begin{cases} \left(\dfrac{1}{R_1} + \dfrac{1}{R_{12} + a}\right)V_1 = I_s \\ \left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + k + \dfrac{R_{12}}{aR_1}\right)V_2 = I_s \end{cases}, \quad \text{where} \quad a = \frac{1}{k + 1/R_2}.$$

When inserting TSVs the effective thermal resistivity R_{12} between the hot spots and cold spots decreases. R_1 and R_2 are the relative thermal resistivity from the heat sources and the dissipation surface (to ambient) respectively. They donot change significantly when TSVs are added. Therefore a decrease in R_{12} leads to a decrease in V_1 and to an increase in V_2. In other words adding TSVs will always decrease the maximum temperature and increase the minimum temperature in a 3D IC stack. Therefore it is not an entirely true statement that adding TSVs decreases temperature across the whole stack. On the contrary it results in temperature increases in many places especially ones close to cold spots.

It is also interesting to note from the above equation that when a heat dissipation solution is very effective, in other words, when the parameter k is very large, it is dominant in the sum $(1/R_1 + 1/R_2 + k + R_{12}/aR_1)$. Hence a decrease in R_{12} results in a small increase in V_2 (the minimum temperature) not equal in magnitude to the decrease in V_1 (the maximum temperature).

In order to reduce temperature in a 3D IC stack everywhere the heat dissipation solution (heat sink included) itself has to be improved. This will increase the value of the parameter k. Thus V_1 and V_2 both decrease.

III. A Compact Thermal Simulation Flow for 3D IC

In this section, we will describe a compact thermal simulation flow for 3D IC utilized in our experiments. It considers the package and multi-dies in the stack simultaneously rather than use an iterative method.

The complete flow is illustrated in Figure 2. Given that individual dies in a 3D IC stack could have been implemented in different technology nodes and different design styles it is to be expected that they would each have a distinct design database. Therefore the first step in our thermal simulation flow is to generate a thermal database for each tier in the 3D IC stack. Here a tier can be a die, a bump layer (the layer between dies -usually having an array of metal bumps), or a heat sink. For a die tier conductivity matrices are extracted layer by layer from the physical layout of the design. TSVs are also extracted and included in the conductivity matrix. The power generation of each thermal grid can be also calculated by using power simulation results. The created thermal database for a die tier has both conductivity and power data. This is not the case for a bump tier or a heat sink tier because they are passive tiers. The only factor dictating the thermal database of such tiers is their material and geometric properties. Different size and distribution of metal bumps or heat sink fins can result in distinct conductivity values of thermal grids. In our simulation flow we use a separate extractor to convert the geometric information of bump tier and heat sink tier into thermal databases.

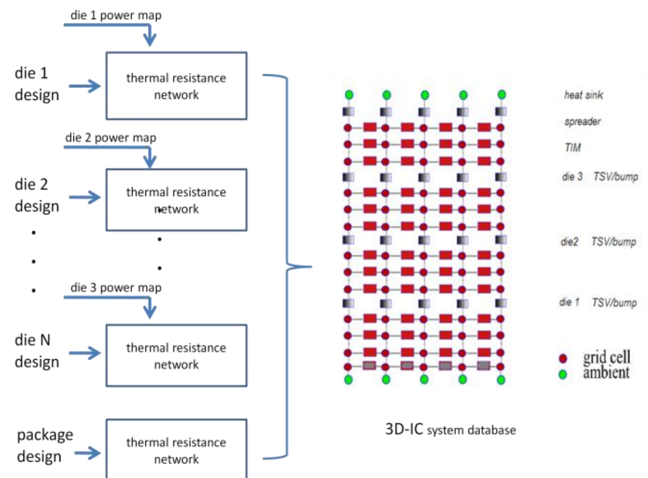

Figure 2. A compact thermal simulation flow for 3DIC

The process of creating a thermal database continues until all the tiers of the 3D IC stack are considered. Then the thermal databases are merged into a single database by stacking the conductivity matrices and power matrices of individual tiers on top of each other. The resulting thermal database of the stack is then solved by a customer-calibrated static thermal simulator.

IV. Experimetal Setup and Results

First we examine the effect of die stacking on temperature. We assume a linear relation between power density and temperature. Then we experiment with different patterns of TSV insertion in order to access the thermal TSV impact on thermal behavior compared to other properties of a 3D IC tier such as the density of TSVs, size of TSVs, and heat transfer coefficient (HTC) of the system. Our results reveal a significantly different role for thermal TSVs than what is usually reported in the literature (however, our work was done for a post routed layout which might explain some of the discrepancies) [7,8,10]. In the following paragraph we give basic information about the test circuit we use in our

experiment. Then we show the effects of die stacking on temperature, followed by the results on thermal TSV insertion.

A. Test circuits information

We use three 6mm×6mm designs as our building blocks of our 3D IC stack. The basic information about these three designs is listed in Table 1. As shown in the table design "L" is a low power ASIC design, design "M" is a memory die and design "C" is a mixture of logic and memory which has a similar structure to that of a CPU. The last column DT is "delta" which is the thermal gradient of the 3D IC system. Starting from layout extraction and power simulation of individual dies we compute the static temperature of each these design. The ambient temperatures for top, bottom and sides of the 3D IC dies are all set to be 27 ℃. From table 1 it is easy to observe that low power logic design and memory design do not show very interesting temperature gradients; however, in a CPU-like architecture the temperature gradient can be as high as 50 ℃.

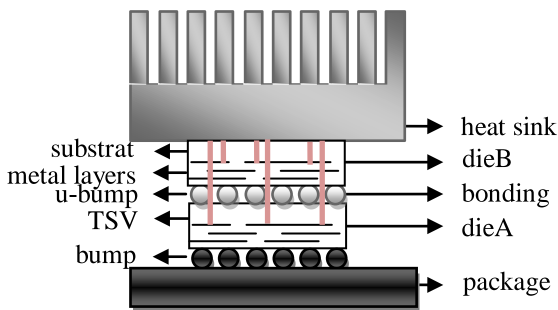

Figure 3. Die stacking in 3DIC. All dies are flipped and the heat sink is attached to the substrate of the top die. Dies are bonded by u-bump layer.

B. Thermal effects of die stacking

In the stacking experiments we define the geometries of bump layers and of the heat sink. The geometries are then converted into internal thermal databases and merged with thermal databases of the dies. The stacking of the 3D IC is illustrated in Figure 3. In our experiments we construct two-die 3D IC stacks using different combinations of three test circuits. Both dies are flipped so that the silicon substrate of the top die is connected to the heat sink.

Name	Type	Power(W)	MinT(℃)	MaxT(℃)	DT(℃)
L	Logic	2.35	52.96	56.74	3.78
M	Memory	1.17	39.98	41.87	1.89
C	Logic+mem	6.13	82.57	135.03	52.46

Table 1. Basic information about test circuits.

As can be seen from Table 2, the minimum temperature of the 3D IC stack increases due to higher power density resulting from stacking. We test three different setups. In "L/L" we have two identical designs "L" on top of each other. In "M/C" we stack memory die "M" on top of CPU die "C", with memory die attached to the heat sink. The last case is "C/M" which is a CPU on top of a memory die; the memory die attaches to the heat sink. In Table 2, for each stacking configuration we list the minimum, maximum temperatures and temperature gradients for individual dies and for the whole system. The column "dieA" indicates the die at the bottom of the stack adjacent to the package pins. The column "dieB" is the die on top adjacent to heat sink.

name	System (℃)			dieA (℃)			dieB (℃)		
	Max	Min	DT	Max	Min	DT	Max	Min	DT
L/L	88.4	80.0	8.5	88.4	82.5	5.9	84.0	80.0	4.0
M/C	158.9	103.7	55.2	158.9	110.5	48.4	129.5	103.7	25.8
C/M	143.3	100.3	43.0	122.9	106.2	16.7	143.3	100.4	42.9

Table 2. Die stacking increases temperature due to higher power density, but with hotter dies close to heat sink, the temperature level can be shifted down.

One observation from case "L/L" is that even with identical power density distribution the die adjacent to the heat sink has better thermal condition than that farther from it. In case of two dies with significantly different power density (as in cases "M/C" and "C/M") placing the die with a larger power density closer to the heat sink always help to reduce the peak stack temperature.

C. Thermal effects of TSVs

In the following experiments we inserted thermal TSVs into the 3D IC stacks constructed as shown in Table 2. TSVs are from metal layer 1 of dieA all the way through the substrate of dieB as illustrated in Figure 3. The major contribution of TSVs to the thermal profile is that they create multiple high thermal conductivity paths from lower layer to layers closer to the heat sink. TSVs do not impact the heat convection of the system as was discussed in section II.

We will first address the most significant observation about the impact of thermal TSV insertion on the thermal profile of the 3D IC stack. Then we discuss the effects of thermal TSVs as a function of their sizes and numbers. We also evaluated the effects of thermal TSV insertion for various heat transfer coefficient values and for different ambient temperatures of the system.

1) TSVs reduce temperature gradient but not minimum temperature

The most important observation we made from our experiments is that inserting thermal TSVs can help reduce the maximum temperature of hotspots in the 3D IC stacks. However it does not reduce the minimum temperature. In other words the role of thermal TSV is merely "soothing" the temperature profile of 3DIC than shifting down the working temperature level as a whole as indicated in the existing literature. Our results are consistent with the theoretical analysis in section II.

Figure 4 shows the simulated maximum temperature and minimum temperature of 3D design "C/M" as a function of TSV area. As shown in Figure 4 as we increase the percentage of TSV area with respect to die area (by inserting more TSVs), we observe that the maximum temperature decreases while the minimum temperature increases. Furthermore the ability of TSVs to reduce maximum temperature is not unlimited. It is loosely bounded on the downside by the minimum temperature of the design before inserting TSVs – a logical expectation. For example, in the extreme case of close to a 100% of the die area occupied by TSVs – an impractical situation - the design has a temperature range of 110°C to

117°C, well above the 100°C lower bound – not to mention the fact that in reality the TSV to die area ratio is much lower. For example 9 of 10x10 TSV arrays composed of 10um diameter TSVs has a TSV array area to die area ratio of 0.25% (6mmx 6mm die) .

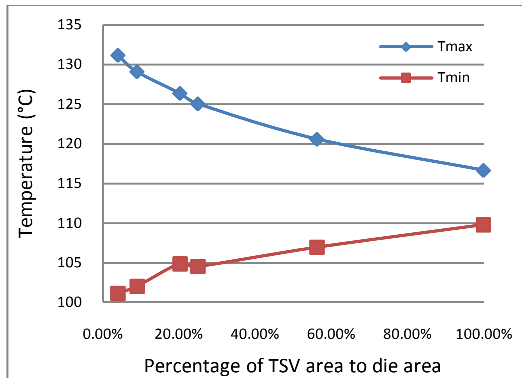

Figure 4. With more TSV inserted, max temperature decreases while min temperature increases, the net effects is to reduce the temperature gradient.

We also examine the effects of thermal TSVs for both low and high thermal gradient cases. In the case of a design starting with low thermal gradient TSV insertion has very limited effect on thermal distribution, a not so surprising result since with a low thermal gradient design the minimum temperature sets the lower bound and is close to the maximum temperature (low gradient) hence not much room for further reducing the maximum temperature. This has been reflected in Figure 5 by the bottom 2 curves in red color.

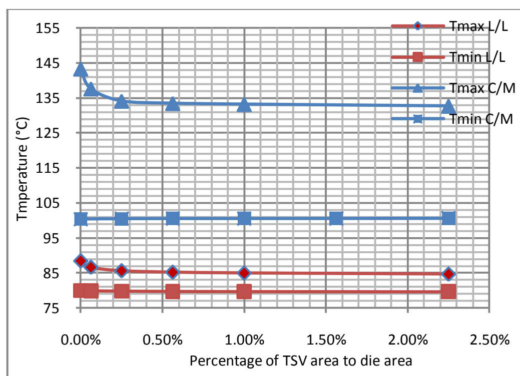

Figure 5. Temperature trend with TSV insertion for design “L/L” and “C/M”

On the other hand the top two curves in figure 5 shows that for a design with a high initial thermal gradient design a small number of TSVs inserted near hotspots can significantly reduce the maximum temperature and consequently the thermal gradient. For design “C/M”, the temperature gradient is 42.9°C without TSV insertion. This can be reduced to 33.7°C (a 9.2°C reduction which is about 5.6% of the maximum temperature) with 9 of a 10×10 TSV array of 10um diameter each (see table 3). Such an array of TSVs consumes merely 0.25% of the total die area of 6mm x 6mm. With a larger TSV array the rate of reduction becomes saturated quickly. Therefore, having TSVs in high thermal gradient designs is always superior to designs with no thermal TSVs in terms of maximum temperature and thermal gradient. But trading off more die area for TSV becomes less effective very quickly.

2) Larger TSVs are better than more TSVs

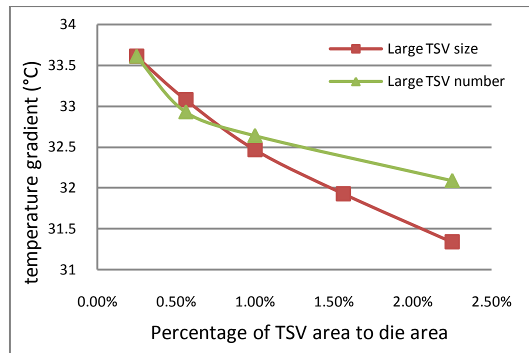

Figure 6. With larger TSVs, it is more efficient to reduce the temperature gradient for design “C/M”.

With the same percentage of TSV area to die area the ability of reducing the thermal gradient varies with different choices of TSV array. We experimented with two different sets of configurations. In the first set we fix the number of TSVs to be 10×10 while increasing the diameter of TSVs; in the second set we fix the diameter of TSVs while increasing the size of TSV array. The results are as shown in Figure 6. From these results we can conclude that for the same TSV to die area using larger TSVs is more effective than using more TSVs in reducing thermal gradients. The reason behind this is shown in Figure 7. In the process of manufacturing TSVs there is a forbidden zone for each TSV. The size of the zone does not increase proportionally to the size of TSV. In other words, larger TSVs can have higher local TSV density compared to smaller TSVs. Even though the two cases in Figure 6 have exactly the same total TSV area the larger TSV case can have higher TSV density around hotspots. This helps further reduce the temperature gradient near those hotspots. This however assumes the flexibility in TSV size which might not be practical. We included it for study completeness.

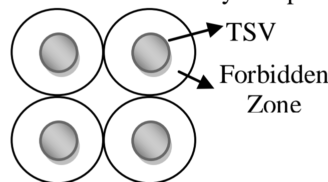

Figure 7. Forbidden zones between TSVs. With larger TSV, the zone does not expand proportionally.

3) TSVs' effect on inter-die gradient is larger than intra-die gradient

Table 3 lists the simulation results for maximum and minimal temperature changes for different dies of a 3DIC stack with different TSV insertion schemes. We used the “C/M” CPU on top of memory chip case. Due to the much higher power density the CPU chip on the top is the hotter chip. Inserting thermal TSVs will clearly show the effect of reducing the whole system temperature gradient (the inter-die gradient). However for each individual die this effect is not as

Area ratio	Bottom Die (memory)			Top Die (CPU)		
	Max	Min	DT	Max	Min	DT
0%	122.9	106.2	16.7	143.3	100.4	42.9
0.06%	124.4	106.2	18.3	137.7	100.5	37.2
0.25%	126.5	106.0	20.5	134.2	100.5	33.7
0.56%	126.8	105.7	21.1	133.5	100.6	32.9
1.00%	126.7	105.5	21.2	133.2	100.6	32.6

Table 3. Impact of TSV on thermal gradients of different die in the 3DIC system.

obvious especially for cool dies. However for hot dies the effect of thermal TSVs on intra-die thermal gradients is significant compared to that of the cool die. In fact the temperature gradient of the memory die increased – a counter intuitive result. It is because some of the heat is transferred from the top hotter die to this cooler die. Therefore the TSVs' effect on intra-die temperature gradient reduction is not always as obvious and as significant as it is on the temperature gradient of the whole 3D IC stack.

4) TSV thermal effects for different HTC and ambient temperature

Independent of TSV insertion changing the heat transfer coefficient and ambient temperature can shift the temperature level of the system as a whole. But changing these environmental conditions does not affect the heat-leveling effect of TSVs much. The following experiments demonstrate this observation.

The results for change in ambient temperature are shown in Table 4. From this table we can see that change of ambient temperature shifts both maximum and minimum temperature by the same amount. However the reduction of thermal gradient by inserting TSVs remains the same regardless the change of ambient temperature.

Area ratio	Ambient = 50°C			Ambient = 27°C		
	Max	Min	DT	Max	Min	DT
0%	166.3	123.4	42.9	143.3	100.4	42.9
0.06%	160.7	123.5	37.2	137.7	100.5	37.2
0.25%	157.2	123.5	33.7	134.2	100.5	33.7
0.56%	156.5	123.6	32.9	133.5	100.6	32.9
1.00%	156.2	123.6	32.6	133.2	100.6	32.6

Table 4. Impact of TSV on thermal gradient does not change with different ambient temperature.

In Table 5 we show the results of thermal gradient changes for two different HTC values under the same TSV insertion patterns. In both cases the thermal gradient always decreases with the addition of more TSVs. The thermal gradient reduction rates in these two cases are similar, does not show a clear monotonic relation with the value of HTC. But the magnitude of temperature gradient reduction in both cases is similar. These experimental results confirm that the effect of TSVs on evening out the heat in the 3DIC stack is not influenced by the boundary conditions. Improving boundary conditions can help reduce the whole stack temperature dramatically does not contribute towards strengthening the role of TSVs in thermal gradient reduction. Reducing stack

Area ratio	HTC = 5000 W/M^2*K			HTC = 2500 W/M^2*K		
	Max	Min	DT	Max	Min	DT
0%	100.5	60.37	40.13	143.3	100.4	42.9
0.06%	95.31	60.44	34.87	137.7	100.5	37.2
0.25%	92	60.47	31.53	134.2	100.5	33.7
0.56%	90.47	60.47	30	133.5	100.6	32.9
1.00%	90.19	60.47	29.72	133.2	100.6	32.6

Table 5. Impact of TSV under different heat transfer coefficient HTC values.

temperature and temperature gradient are two de-coupled tasks. They can be achieved by improving boundary conditions and TSV insertions respectively.

V. Conclusions

In summary we conclude that the thermal TSVs role is limited to improving heat conduction but not heat dissipation. They evens out inter-die gradients more than intra-die ones. Adding thermal TSVs will bring down the peak temperature of the stack to a certain finite extent but slightly increase the minimum temperature. The benefits from thermal TSVs saturates quickly along an increase in either TSV size or density. Thermal TSVs role in reducing the temperature gradient is not strongly affected by changing boundary conditions. Its role is relatively independent of boundary conditions that can significantly impact the whole 3DIC system temperature level.

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