

Music to Your Ears: Tune In to Liberty 2009.06

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AGENDA

- **Power Down Function for state elements**
- Synchronous pin Type for latch cells

Power Down Function for state elements

- Background & Introduction
 - Currently `power_down_function` (PDF) can only be specified on output pins
 - Internal states corruption in seq. cells also needs to be modeled
 - To overcome such modeling limitations Liberty can now model the PDF inside the `ff/latch/statetable` groups

Power Down Function for state elements

- Liberty Syntax of PDF in a ff or latch element:

```
cell (name) {  
  
...  
    ff/latch (variable1, variable2) {  
        clocked_on : "Boolean expression" ;  
        clocked_on_also : "Boolean expression" ;  
        next_state : "Boolean expression" ;  
        preset : "Boolean expression" ;  
        clear : "Boolean expression" ;  
        clear_preset_var1 : L | H | N | T | X ;  
        clear_preset_var2 : L | H | N | T | X ;  
        power_down_function : "Boolean expression" ;  
    }  
  
...  
}
```

Power Down Function for state elements

- Liberty Syntax of PDF in a statetable group:

```
cell (name) {  
...  
  statetable( "input node names", "internal node names"  
    ) {  
    table : " input node values : current internal values  
      : next internal values,\n...  
          input node values : current internal values  
      : next internal values";  
    power_down_function : "Boolean expression" ;  
  }  
...  
}
```

Power Down Function for state elements

```
library ("low_power_cells")
{
  cell ("retention_dff") {
    pg_pin(VDD) {
      voltage_name : VDD;
      pg_type :
      primary_power;
    }
    pg_pin(VSS) {
      voltage_name : VSS;
      pg_type :
      primary_ground;
    }
    pin ("D") {
      direction : "input";
    }
    pin ("CP") {
      direction : "input";
    }
  }
}
```

```
ff(IQ,IQN) {
  next_state : "D" ;
  clocked_on : "CP" ;
  power_down_function : "!VDD +
VSS" ;
}
  pin ("Q") {
    function : " IQ ";
    direction : "output";
    power_down_function : "!VDD
+ VSS";
  }
  ...
}
...
}
```

AGENDA

- Power Down Function for state elements
- **Synchronous pin Type for latch cells**

Synchronous pin Type for latch cells

- Background & Introduction
 - Limitation
 - There is no attribute to distinguish latch synchronous set/reset/enable pins from the data pins
 - So it is required that these special non data pins should be correctly modeled
 - To overcome such modeling limitations Liberty can now model `data_in_type` inside the pin groups

Synchronous pin Type for latch cells

- A new attribute "data_in_type" will be defined in the .lib file. It will be specified on the pins of the latch cell.

```
pin(name) {  
  
    ...  
    data_in_type :enum( preset,clear,load,data) ;  
  
    ...  
}
```

Synchronous pin Type for latch cells

```
library(sync_latch_pin) {  
  voltage_map( VDD, 0.8);  
  voltage_map(VSS, 0.0);  
  ...  
  cell(latch_with_sync_set) {  
  
    pg_pin(VDD) { ... }  
    pg_pin(VSS) { ... }  
  
    latch(IQ,IQN) {  
      data_in : "D + S";  
      enable : "CK";  
    }  
    pin(D) {  
      direction : input;  
      capacitance : 1.0;  
      data_in_type : data;  
      timing() {  
        ...  
      }  
    }  
  }  
}
```

```
pin(S) {  
  direction : input;  
  capacitance : 1.0;  
  data_in_type : preset;  
  timing() {  
    ...  
  }  
}  
pin(Y) {  
  direction : output;  
  function : "IQ";  
  power_down_function : "!VDD + VSS";  
  timing() {  
    ...  
  }  
}
```

For More Liberty Information

- <http://opensource.liberty.org/>
- Current Version
 - Liberty Documentation version 2009.06
 - Liberty Parser Version 2.6

