

Welcome to the 21st EDA Interoperability Forum

sponsored by



November 6, 2008

Welcome to the 21st EDA Interoperability Forum

Rich Goldman
Vice President
Corporate Marketing &
Strategic Alliances

What you've come to expect...

- Interesting keynote presentation
 - *“EDA is an Ecosystem: Interoperability and the Future of EDA”*
 - Mike Santarini – Former EDA editor with EE Times and EDN Magazine; now publisher of Xcell Journal and Sr. Manager of Editorial services at Xilinx
- Relevant information
 - Interoperability for Custom Design
 - Practical Usage of VMM Verification Methodology
 - Liberty for All Design Flows
 - TLM 2.0 for System Level Design
- Plus prizes!

Stay informed. Get involved. Participate in the Process.



- Accellera www.accellera.org
- EDA Consortium www.edac.org
- EEMBC www.eembc.com
- IEEE www.ieee.org
- IPL Alliance www.IPLnow.com
- The Multicore Association www.multicore-association.org
- Open SystemC Initiative www.SystemC.org
- Si2 www.si2.org
- SOI Industry Consortium www.soiconsortium.org
- SPIRIT Consortium www.spiritconsortium.org



And more!...



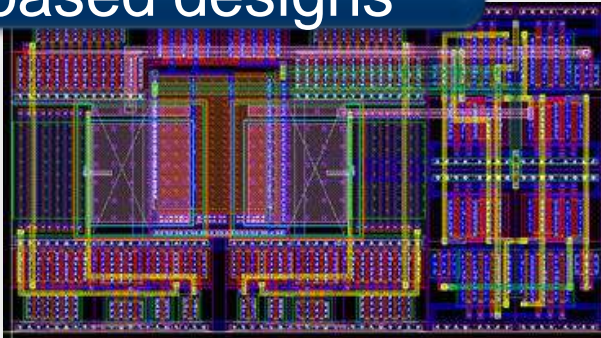
Join IPL Alliance

- IPL Charter:
 - Create and promote standards for Interoperable Process Design Kits (PDKs) on the OpenAccess database
- IPL Benefits:
 - Enables a single PDK to support any OpenAccess tool
 - Reduces PDK development and support costs
 - Creates choices in building your analog design flow
- IPL Latest News:
 - Synopsys has contributed a draft standard for Interoperable Property and Parameter Definitions to the IPL Alliance

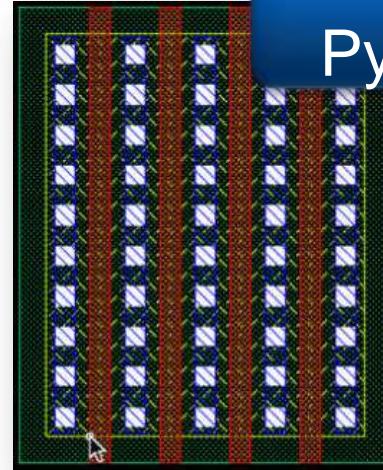
Visit www.IPLnow.com for a video demo and free downloads

Custom Designer - Open & Portable

OpenAccess
based designs



Pcells based on
Python and TCL



TCL based script
language

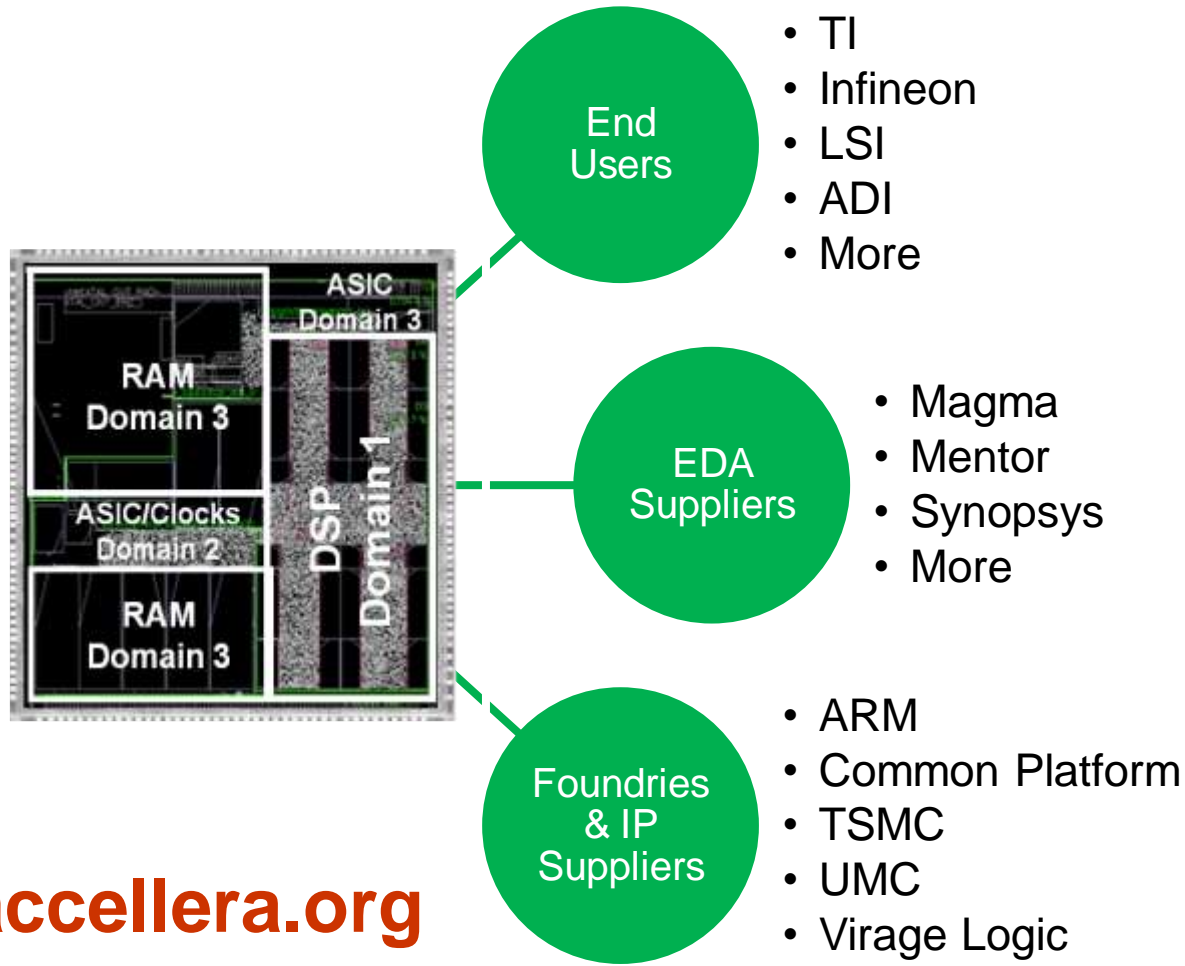
```
set libName generic90RF
set cellName n_4t
set oaLib [oa::LibFind $libName]
oa::getAccess $oaLib write 1
set oaCell [oa::CellFind $oaLib $cellName]
set accessMode "w"
set dmData [oa::DMDataOpen $oaCell $accessMode]

db::setNetlistInfo fieldHeight -cell $dmData -section form \
-value 15 \
-type integer
```

Presentation earlier this morning



UPF 1.0 – A Success in the Market



www.accellera.org



IEEE UPF / IEEE P1801 Progress



EE Times

EE Times: Design News

IEEE to vote on new low-power design standard

IEEE P1801 standardizes and enhances Accellera Unified Power Format

[Gabe Moretti](#)

(10/31/2008 11:22 AM EDT)

URL: <http://www.eetimes.com/showArticle.jhtml?articleID=211800552>

Venice, Florida — The IEEE has announced that development within the working group dedicated to IEEE P1801, "Standard for Design and Verification of Low Power Integrated Circuits," has been completed, and the standard has gone to sponsor ballot. The standard is also known as Unified Power Format (UPF) 2.0. UPF, first developed by Accellera, is currently supported by multiple vendors and is in use worldwide. This is the first time that UPF has undergone an IEEE standardization effort.

- Upward compatible with UPF 1.0
- Voting opened on Oct. 28th and is expected to close on Nov. 27th

 **IEEE** **P1800 SystemVerilog**

- IEEE P1800 SystemVerilog draft 7a is being prepared for balloting late 2008
- For more information, visit

www.eda.org/sv-ieee1800

- Find products, solutions, technical papers & more at Accellera's

www.systemverilog.org



Open SystemC Initiative

- SystemC 2.2 open source library released April 2007
- Transaction Level Modeling (TLM) 2.0 *Presentation right after this*
 - Public review of draft finished March 2008
 - Ratification on June 9, 2008
 - SystemC TLM-2.0 API Kits available
- Upcoming Regional User Group meetings
 - www.systemc.org/community/user_groups
 - North America: February, 2008 Santa Clara at DVCon

www.SystemC.org
standards.ieee.org/getieee/1666

Visit VMM Central

- Comprehensive online resource for VMM
- VMM Version: 1.0.1; Release Date: June 9, 2008
- Download the complete open source implementation which includes:
 - VMM Standard Library
 - VMM Register Abstraction Layer application
 - VMM Reusable Environment Composition application
 - VMM Memory Allocation Manager application
 - VMM Hardware Abstraction Layer application
 - VMM Data Stream Scoreboard application
 - VMM Macro Library
 - VMM Planner language specification
 - VMM Utilities, including RALGEN and VMMGEN
 - VMM Documentation
 - VMM Examples



www.vmm-central.org

VMM Presentation at 1:45

Download Current Versions

- Liberty 2007.12

www.OpensourceLiberty.org

- Liberty Parser 2.5
- Liberty CCS Modeling Technology (Timing, Noise & Power)
- Liberty 2008.09 *Available in December; Presentation at 2:45*

- Other Open Source Formats:

www.synopsys.com/partners/tapin

- SAIF 2.0 *for switching activity*
- SDC 1.7 *for design constraints*
- vSDC 2005.12 *for formal verification*

Download Current Versions

- Milkyway Access Program (MAP-in):
 - Milkyway Database Environment & C-API Z-2007.12
New!
 - Milkyway Database Environment & C-API A-2008.09
Available in December

www.synopsys.com/partners/mapin

Check out “The Standards Game”

www.synopsysoc.org/thestandardsgame

- A blog by Karen Bartleson

The screenshot shows the Synopsys Open Community.org website. At the top, the logo for Synopsys Open Community.org is displayed, with the tagline "An online forum for electronic design professionals". Below the logo, the page title "The Standards Game" is visible. The main content area features a blog post by Karen Bartleson, dated October 30th, 2008, titled "A less visible, yet important, ballot is underway: P1801". The post discusses the IEEE P1801 standard, also known as the Unified Power Format (UPF), and its importance in low power IC design. The right sidebar contains an "About" section with a photo of Karen Bartleson and a "Recent Posts" section listing other articles.

SynopsysOC

The Standards Game

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1. Life in the Standards Lane
2. Skirmishes, Battles and All-Out Wars
3. Duh.
4. Be There or Be Square
5. Travel Tales
6. The 10 Commandments
7. just me

Uncategorized

Blogroll

1. JB's Circuit
2. Harry the ASIC Guy
3. RonAmok!
4. Cool Verification

A less visible, yet important, ballot is underway: P1801

Posted by [karenb](#) on October 30th, 2008

I don't know about you, but I'll be glad when the 2008 U.S. elections are over. I mailed in my ballot this week and am now immune from those working hard to sway my vote. I am honored and grateful to live in America, and I hope for a healthy, reunified country with global consciousness in 2009.


In The Standards Game, there is another important ballot underway: IEEE P1801, formally known as the "Standard for Design and Verification of Low Power Integrated Circuits". You may know this standard as UPF, the **Unified Power Format**, which was approved as an **Accellera standard** in February, 2007. I've written about this standard in previous posts, describing its technical advantages and openness, plus the desire for a **single industry standard**.

The reason for UPF's long official name in the IEEE is to distinguish it from other standards with the word "power" in their title. As I might have mentioned, I'm a member of a couple of committees in the IEEE that approve standards in a wide range of electrical and electronic engineering fields. I fondly remember one of my fellow committee members telling me that "low power" to him meant anything below 25,000 volts. We certainly wouldn't want a nuclear power plant generating the kind of low power that we think of in the semiconductor industry.

Low power IC design continues to be an imperative to support modern electronic product requirements. The UPF/IEEE P1801 standard provides an open foundation for low power design solutions. Leading suppliers of these solutions have built and are building tools and flows around UPF.

UPF 1.0 from Accellera has been in real-world use, which has given users and EDA tool developers insights into ways to polish and enhance it within the IEEE P1801 Working Group. Oversight, ambiguity, verbosity, and backward compatibility have

About



I can hardly believe it. I've been in the EDA business since 1980 when I joined TI's Design Automation Department after graduating from Cal Poly with my BSEE. Since 1995, much of my attention has been focused on EDA standards. I reached a moment of truth this year when I admitted, albeit reluctantly, that I could be called a standards-lifer. So, I decided it's time to share my perspectives on what's going on in the standards arena. Welcome to my blog - I can't wait to hear from you!

- Karen Bartleson

Recent Posts

A less visible, yet important, ballot is underway: P1801

OVM and VMM back in the news

Big news! OpenAccess enables new analog design solutions

You're invited: 21st EDA Interoperability Forum, Nov. 6, 2008

8th Annual Tenzing Norgay Interoperability Achievement Award

- Presented to a company that
 - Surpasses common levels of interoperability
 - Contributes to overall industry advancement
 - Provides a new view of the future
 - Ensures customer success



*Tenzing Norgay
on Mt. Everest*



Previous Award Winners

- **2001: CoWare**
- **2002: Mentor Graphics**
- **2003: Silicon Metrics**
- **2004: Novas Software**
- **2005: ARM**
- **2006: Electronic Tools Company**
- **2007: The UPF Founding Team**

Nokia, Texas Instruments, Magma, Mentor Graphics



And the 2008 winners are...



The **IPL** Interoperable PDK Libraries **NOW.COM** Key Contributors



9th Tenzing Norgay Award

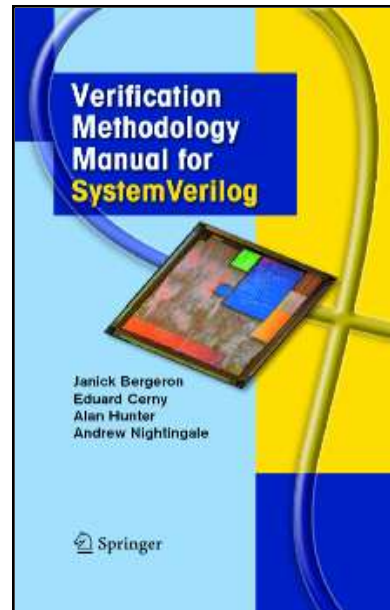
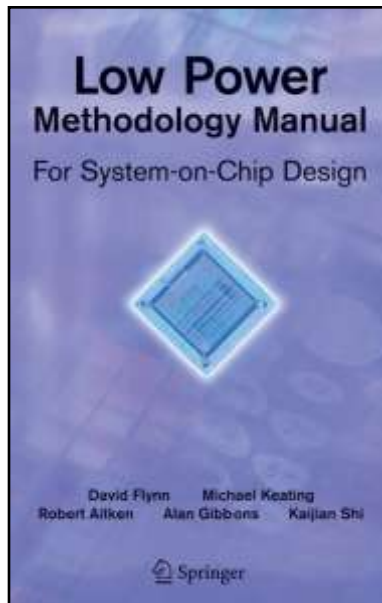
- Will be presented at the DAC 2009 Interoperability Breakfast
 - Wednesday, July 29, 2009
- Nominations are active for 3 years



Call for nominations now until April 17th
www.synopsys.com/tapin/tnorgay

Presentations & Prizes...

- Presentations will be available for download from the web Thursday 11/13: www.synopsys.com/devforum/nov2008/presentations
- Early birds get the worms
 - \$15 Starbucks gift cards to first 10 attendees
- Get your raffle ticket and complete your feedback forms to be eligible to enter drawings* for more prizes:
 - *Low Power Methodology Manual* by ARM and Synopsys
 - *Verification Methodology Manual for SystemVerilog* by ARM and Synopsys
 - Apple iPod® shuffles



*Must be present to win

22nd EDA Interoperability Forum

- Fall 2009
- In Silicon Valley
- Invite your colleagues
- Want to speak? Let us know.

See you then!

Today's Agenda

- Interoperability for Custom Design

- How to integrate EDA tools with Synopsys' Custom Designer via its open environment
- Design Data Management for Synopsys' Custom Designer
- IPL Alliance's standards for interoperable PDKs

This morning

- Lunch

- General Session

12:15PM – 4:00PM

- Welcome & Standards Update
- SystemC TLM-2.0 – Kicking platforms into full gear!
- Keynote Presentation
EDA is an Ecosystem: Interoperability and the Future of EDA
Mike Santarini, Xilinx
- Practical Usage of VMM Applications in verification process
- Generating VMM Compliant Environments
- Liberty for All Design Flows

Enjoy your 21st EDA Interoperability Forum

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