

# **Kicking Virtual Platforms into Full Gear**

## **How SystemC TLM-2.0 Interoperability will lead to Mainstream Adoption of Virtual Platforms**

Synopsys Interoperability  
Developer's Forum  
November 6<sup>th</sup> 2008  
Santa Clara, California

# Agenda

- **The Wave is coming**
- The age of proprietary solutions
- The age of standardization
- The impact on the virtual platform market
- Summary and Closure

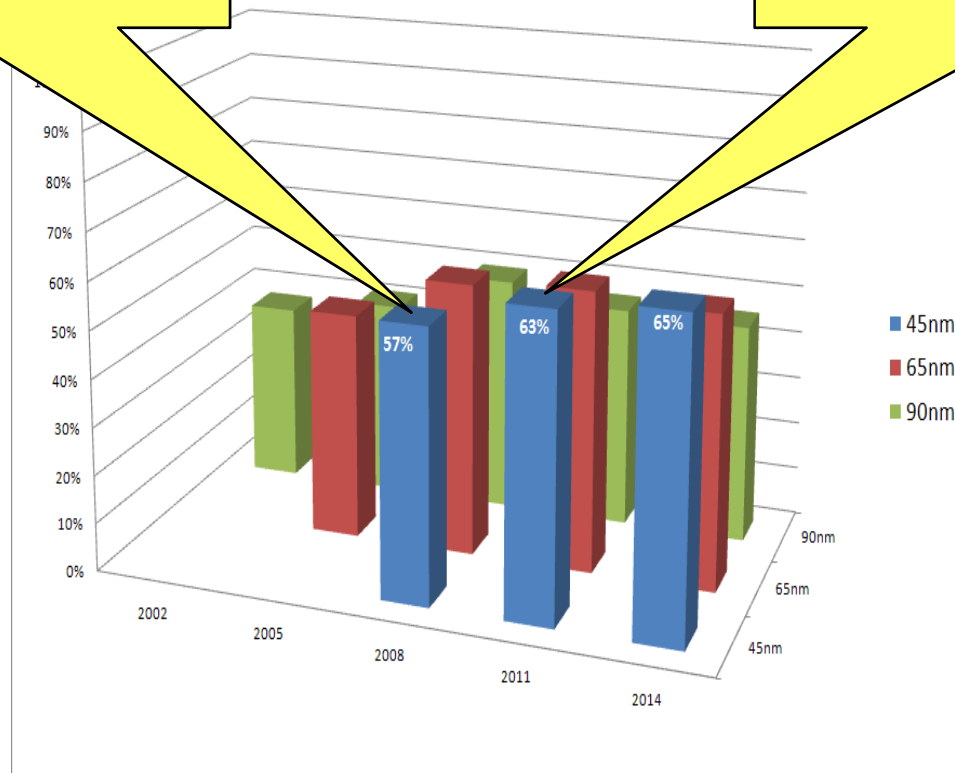
# Market Dynamics

Software is already a huge issue today and will further worsen!

65nm today: Software development cost > 57%!

Percentage of Software Cost in IC Product Development

45nm in 2011: Hardware development cost < 40%



Source: IBS

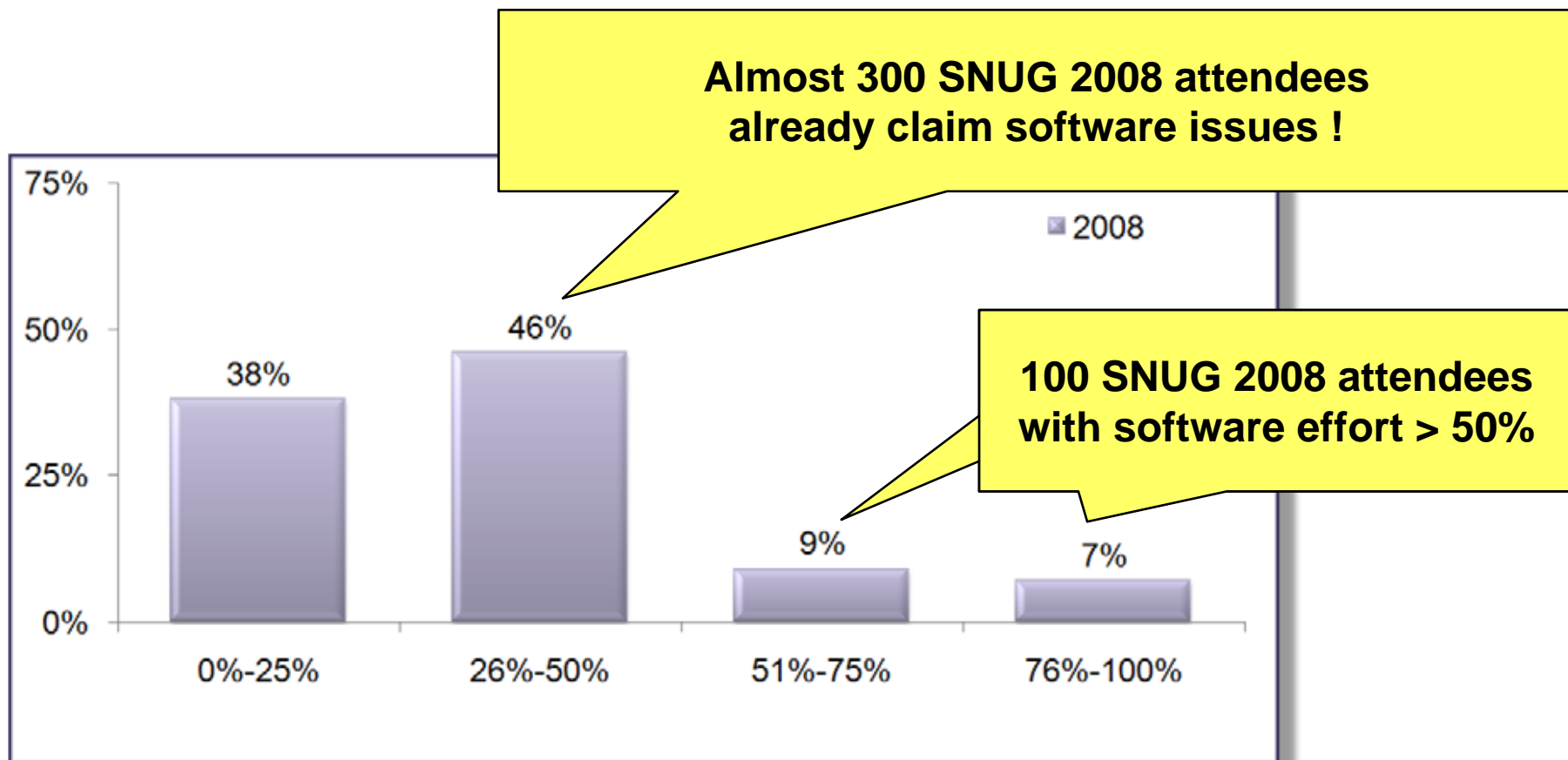
**“It’s The Software, Stupid!”**

Dataquest, DAC 2006

**Productivity,  
Validation,  
Time to Market,  
Multicore**

# Market Dynamics

Synopsys SNUG Data confirm the software trend!



What percentage of your total project effort is spent on software development (vs. hardware development) during design?

2008 N = 404; Margin of error = +/- 5%

Source: Synopsys San Jose SNUG Survey

# It's huge, alright!

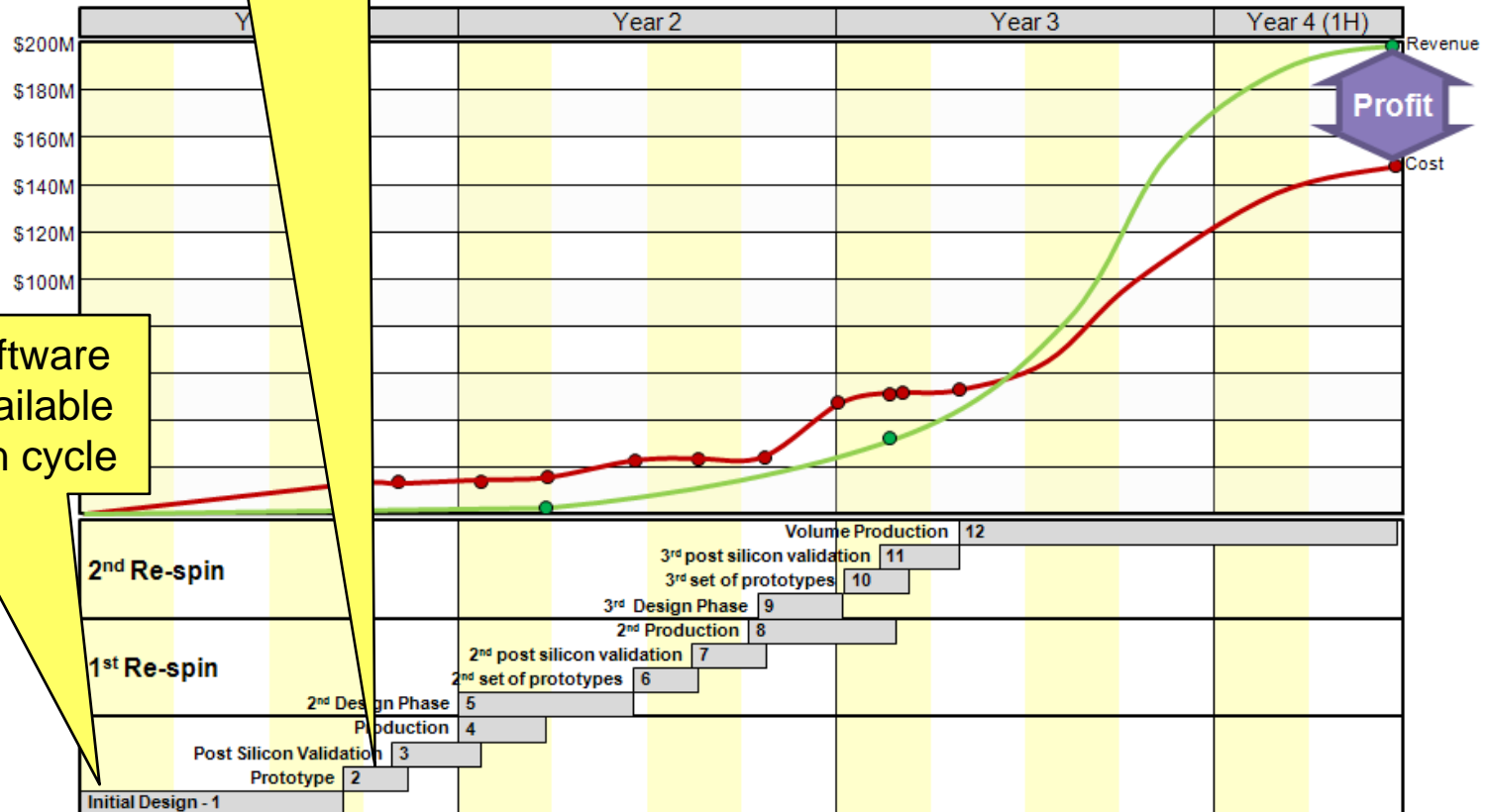


# So where to hide?

## A Chip Design Project P&L Without Virtual Platforms

Tests for post-silicon validation are developed late as well

Prototype for software development available late in the design cycle

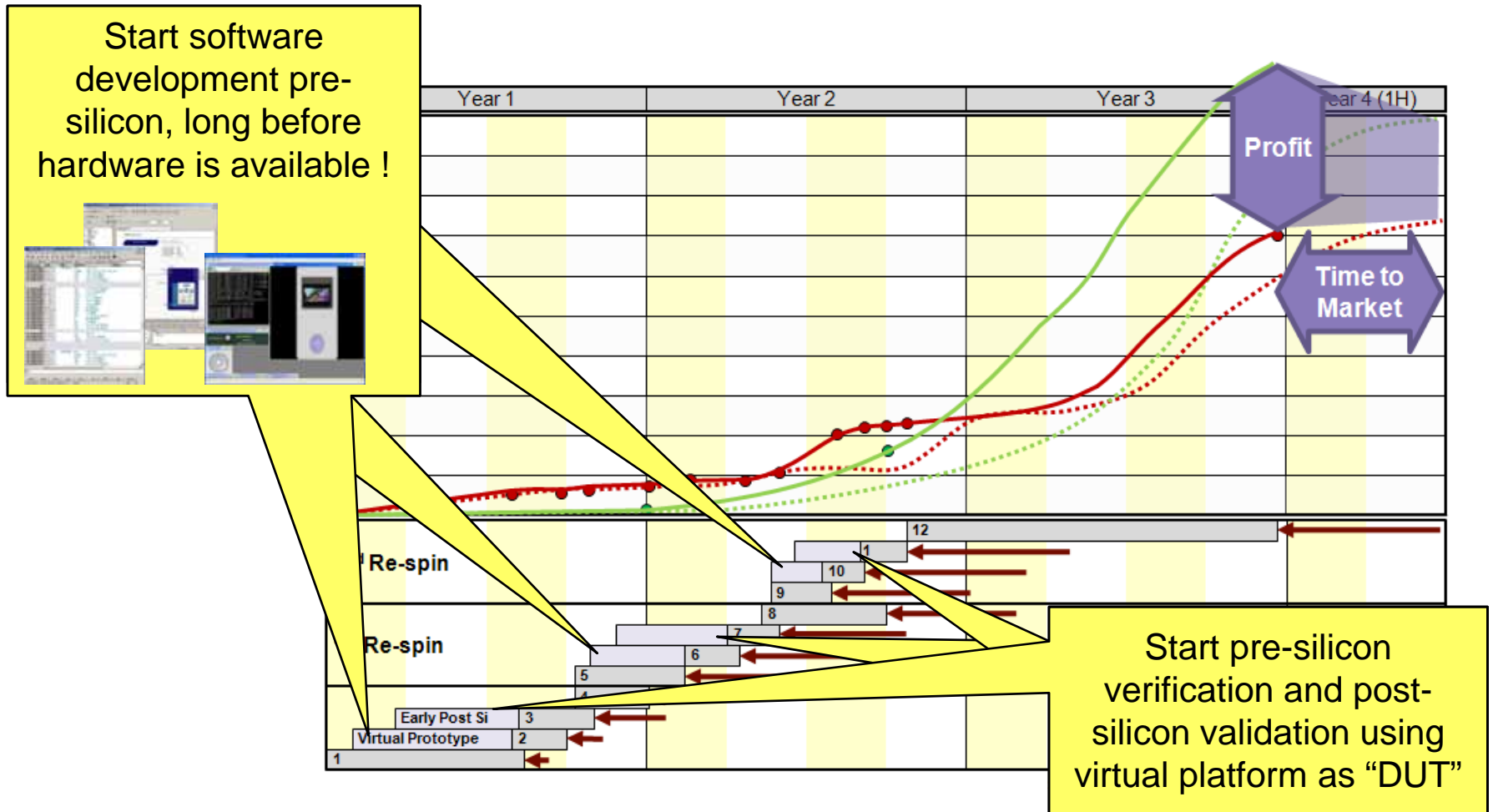


Source: Derived from IBS Data, 130nm, Wireless Application



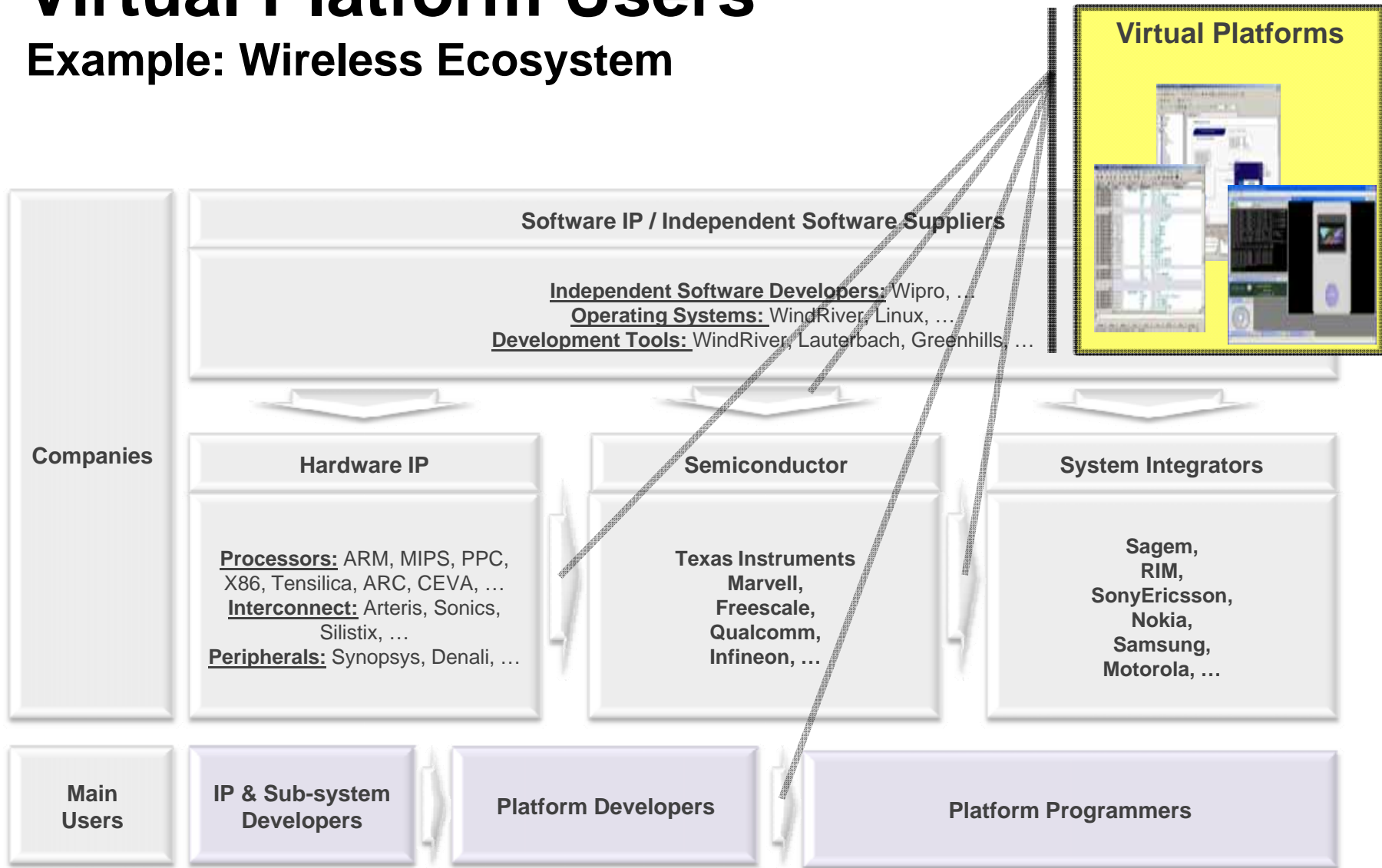
# Virtual platform business impact

## Get to market early and increase profit



# Virtual Platform Users

## Example: Wireless Ecosystem

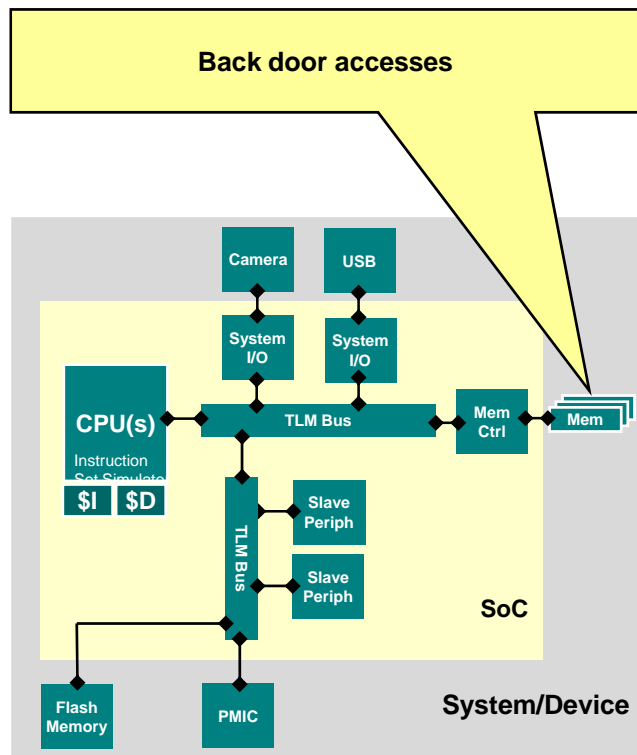


# Agenda

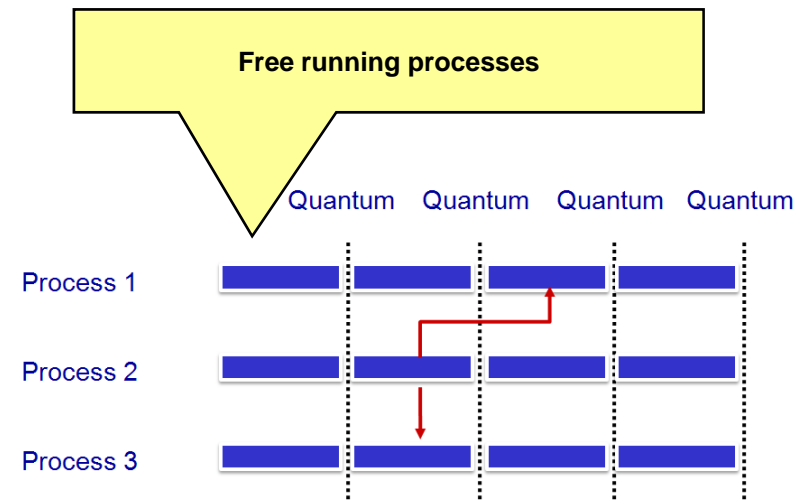
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# What makes virtual platforms fast?

## Direct memory accesses



## Quantum based simulation



# Once upon a time ...

## September 27<sup>th</sup> 1999

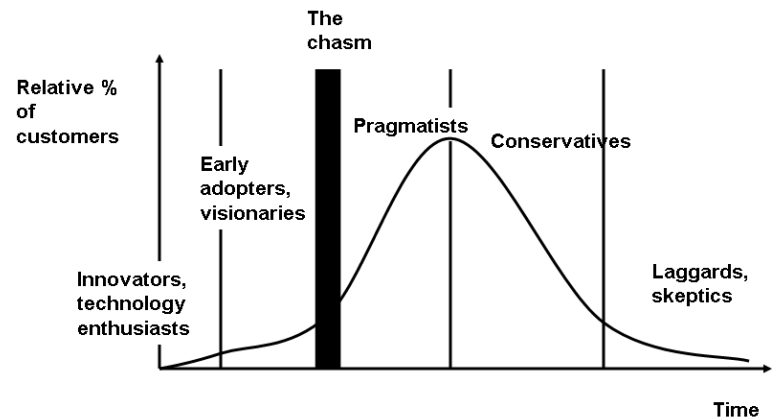
- “Major Industry Players Collaborate On Open C++ Modeling Platform To Solve Key System-On-A-Chip Problems”
- 45 charter member companies
  - Systems
  - Semiconductor
  - IP
  - embedded software
  - EDA
- Steering group
  - ARM, CoWare, Inc., Cygnus Solutions, Ericsson, Fujitsu, Infineon, Lucent Technologies, Sony Corporation, STMicroelectronics, Synopsys, Inc. and Texas Instruments.

## From the press release

“enable fully interoperable system-level IP exchange and co-design,” and to address “challenges for system-on-chip (SoC) [design, which] are the result of decreasing time-to-market coupled with rapidly increasing gate counts and **embedded software representing 50 to 90 percent of the functionality.**”

# Once upon a time ... Proprietary!

- 1997
  - AXYS Design Automation
    - Spin-off of the Aachen University of Technology
    - Language for instruction set architecture (LISA)
  - VaST Systems Technology Corporation
    - Sydney, Australia
    - binary code translation
- 1998
  - Virtutech
    - spin-off from the Swedish Institute of Computer Science (SICS) in Stockholm
- 1999
  - Virtio
    - Spin-off of National Semiconductor
  - Several in-house solution
    - Motorola Objected Oriented Simulation Environment (MOOSE).



All early providers of virtual platform technology developed proprietary modeling solutions

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# 2007 comes along ...

## Major Contributions

### **Synopsys Contributes Virtual Platform Technology to OSCI SystemC TLM 2.0 Standardization Effort**

### **Key Technology Donated to Further OSCI Standard's Evolution**

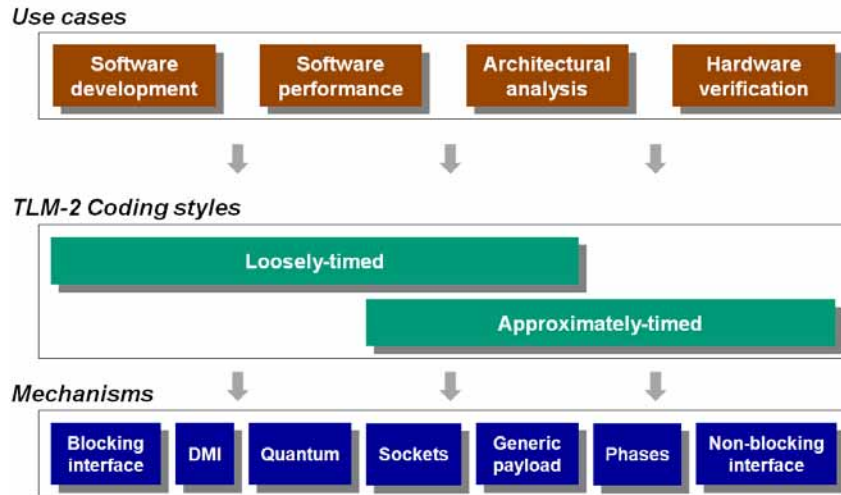
MOUNTAIN VIEW, Calif., January 24, 2007 - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor and system level design software, today announced that it has contributed key technology to the Open SystemC Initiative (OSCI), an independent not-for-profit organization dedicated to supporting and advancing SystemC as an open source standard for system-level design. The contribution addresses the need for a high-performance interface standard to enable the development of Virtual Platforms based on SystemC.

## Major Collaboration

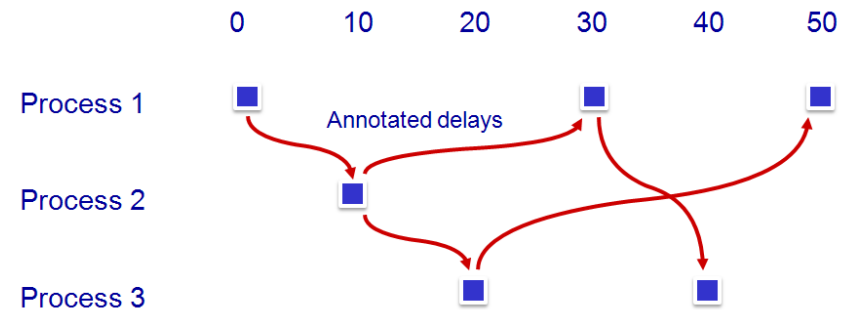
- TLM Working Group
- Feedback from user companies, ESL tool developers, and intellectual property (IP) providers including OSCI members
  - ARM
  - Cadence
  - CoWare
  - Doulou
  - ESLX
  - GreenSocs
  - Intel
  - Infineon
  - NXP
  - STMicroelectronics
  - STARC
  - Synopsys

# The Impact of SystemC TLM-2.0

## Several Use Cases



## Several Timing Models

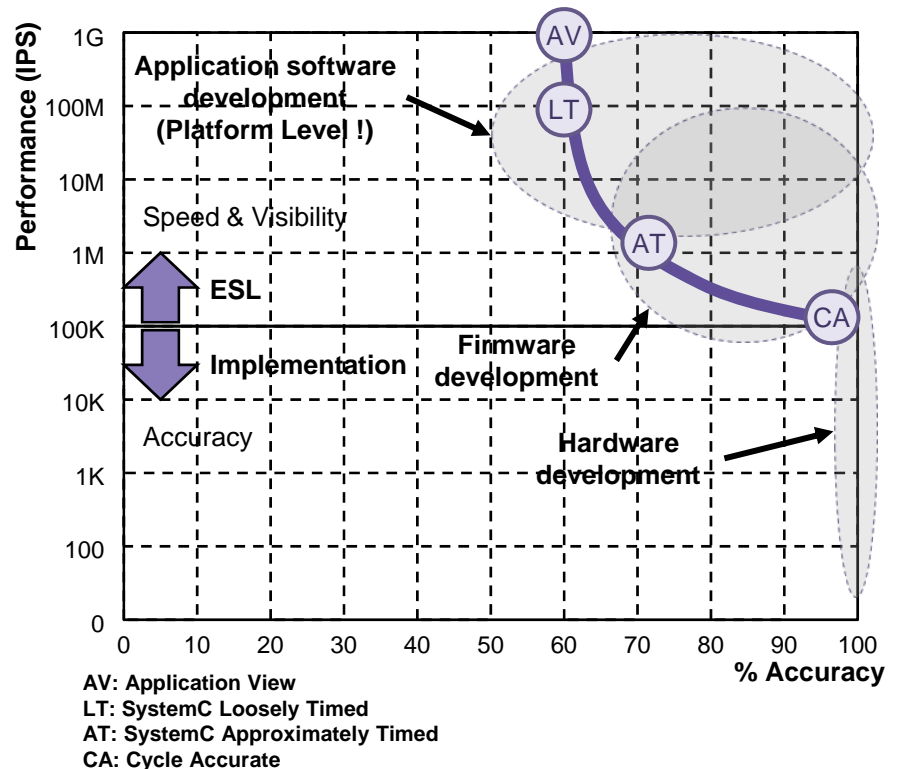


# The Impact of SystemC TLM-2.0

## Enabling Interoperability and Scalability

Previously proprietary (backdoor) APIs & new additions have now been standardized:

- (DMI) Direct Memory Interface
  - Direct backdoor access into memory
  - Allows un-inhibited ISS execution
- LT (Loosely Timed) modeling
  - Timing declaration
  - Allows speed/accuracy trade-offs
- Temporal Decoupling
  - Only synchronize when necessary
  - Allows multicore speedup



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# The Impact of SystemC TLM-2.0

A Historic Moment – like Verilog in the 90's!

Hardware Description Languages		Virtual Platforms	
1980's	1990's	1998 - 2008	Post 2008
<u>Age of Proprietary HDLs</u>	<u>HDL Standardization</u>	<u>Proprietary APIs</u>	<u>Age of Interoperability</u>
Verilog VHDL HiLo DABL LASAR Aida M (Lsim) QuickSim UDL / I N dot ISP	Verilog VHDL HiLo DABL LASAR Aida M (Lsim) QuickSim UDL / I N dot ISP	Roll your own (C, C++) SystemC TLM-1.0 Synopsys Virtio ARM AXYS APIs CoWare N2C APIs Virtutech APIs VaST APIs ...	TLM-2.0

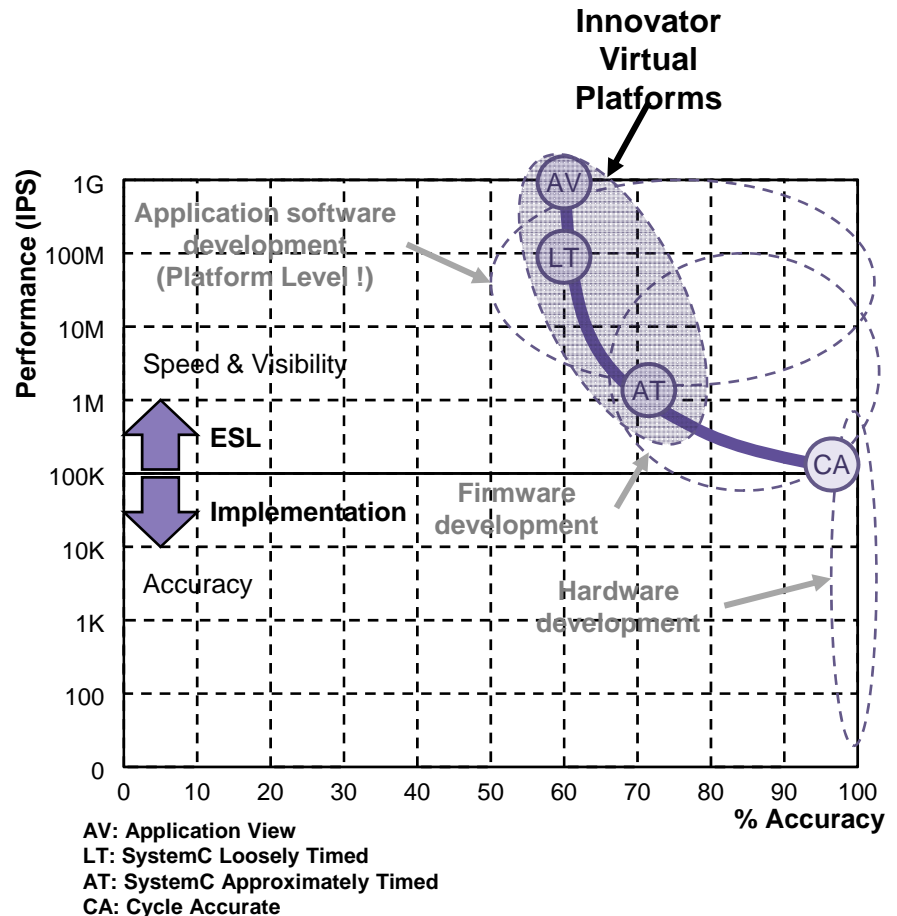
### What it means for you:

1. Model interoperability
2. Simulation commoditization
3. **It's all about the models!**

# The Impact of SystemC TLM-2.0

## Separation of Tools and Libraries

- Bifurcation in tools and interoperable libraries
- Synopsys example
  - Innovator
    - PV (LT) modeling
    - PV+T (AT) “timing annotation”
  - DesignWare® IP
    - Implementation, Verification and System-Level IP
  - Modeling Services

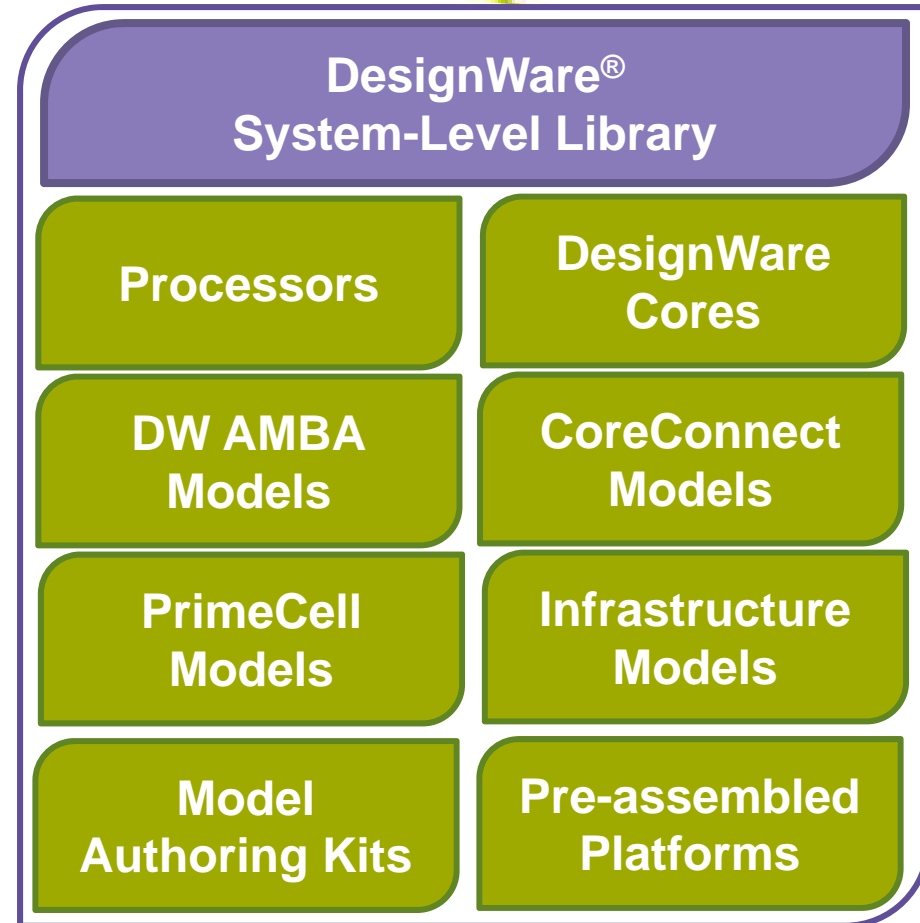


# DesignWare System-Level Library

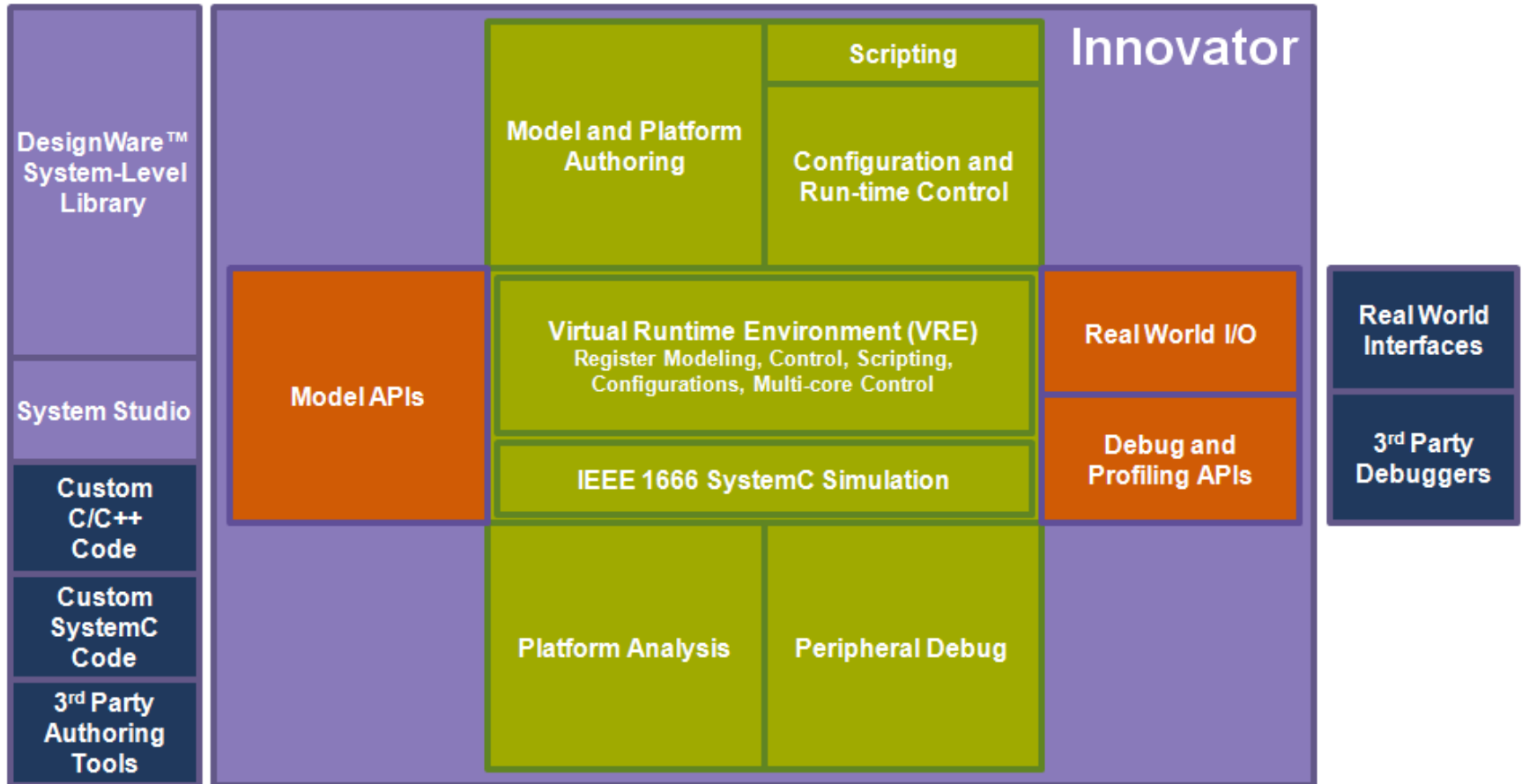
## Overview



- Accelerate virtual platform creation, through a portfolio of transaction-level models (TLMs)
  - High performance & quality
  - 100+ titles & growing ...
- Written in SystemC™
  - TLM-2.0 API support
- Tool independent: works with any IEEE-1666 compliant SystemC simulator
- Supported on Windows & Linux
- Delivered in binary format
- Model Authoring Kits

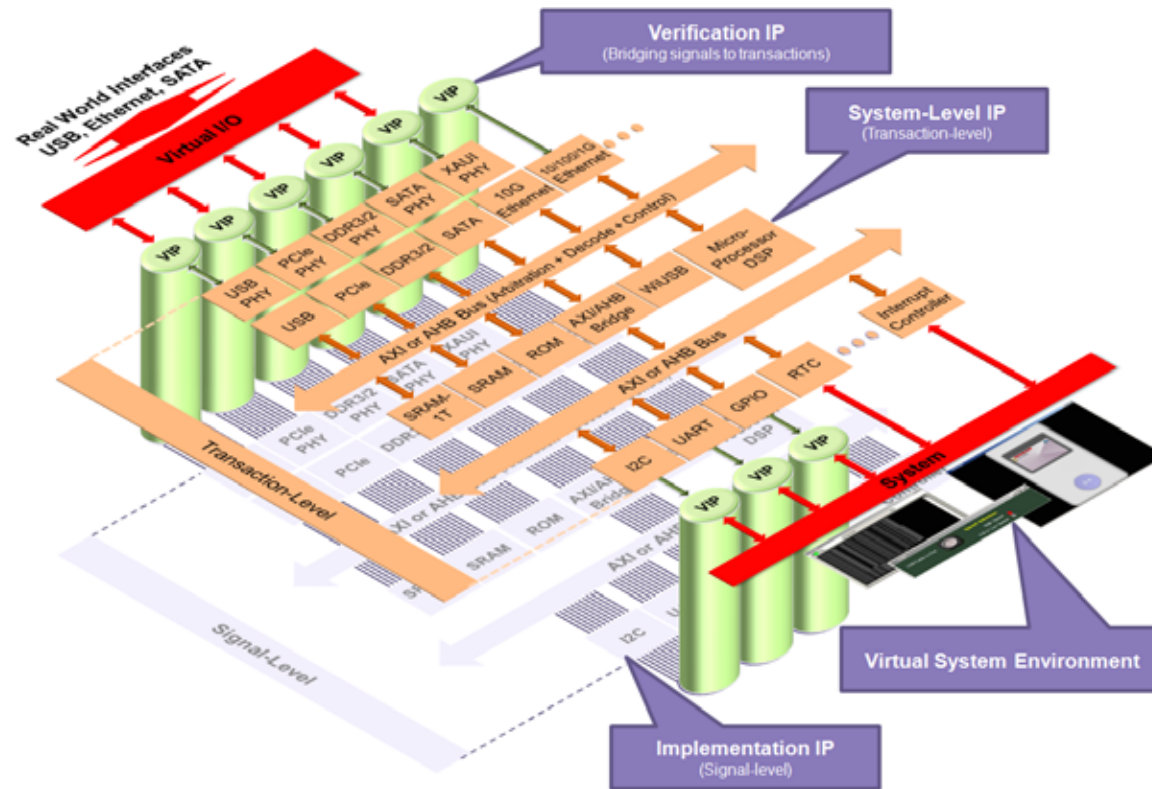


# Innovator SystemC Integrated Development Environment



# DesignWare® IP: Industry's Broadest Portfolio

## Synopsys 1<sup>st</sup> in Implementation, Verification and System-Level IP



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# DesignWare System-Level Library

## Content Overview

### Processor Models

- ARM
- MIPS
- PowerPC



### DesignWare Core Models

- USB 2.0 High Speed OTG / USB 2.0
- SATA AHCI / SATA Host
- Ethernet
- PCIe



### DesignWare AMBA Models

- AMBA AHB/APB peripherals
- UART, I2C
- Interrupt controller
- Watchdog timer
- DMA controller



### IBM CoreConnect Models

- Busses
- Memories
- Master / Slaves
- Example configurations



### ARM PrimeCell Models

- Interrupt controller
- DMA controller
- Watchdog timer
- UART
- Inter Processor controller

### Infrastructure Models

- Generic peripheral components (UART, INTC, RAM)
- Board components (SATA HDD)

### Model Authoring Kits

- USB Host
- USB EHCI
- UART

### Pre-assembled Platforms

- Multi-media Player
- ARM Integrator
- Multi-layer AMBA
- Unit-test platform



# Synopsys Product Offering

## Virtual Platforms In the Design Flow

Functional Specification – Defining the overall hardware / software system



RTL to GDSII Implementation Flow (Discovery VCS to Galaxy)

# Summary

- Got TLM-2.0? Synopsys does!
- TLM-2.0 is here! The age of TLM interoperability has begun
- Models now fully interoperable
  - DesignWare System-Level Library models run in all simulators
  - All user models can be imported into Innovator
- **What can you do?**
  - Download TLM-2.0 package at [www.SystemC.org](http://www.SystemC.org)
  - Join OSCI to participate
  - Contact Frank Schirrmeister <fschirr@synopsys.com> to discuss interoperability with Synopsys offerings



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Predictable Success