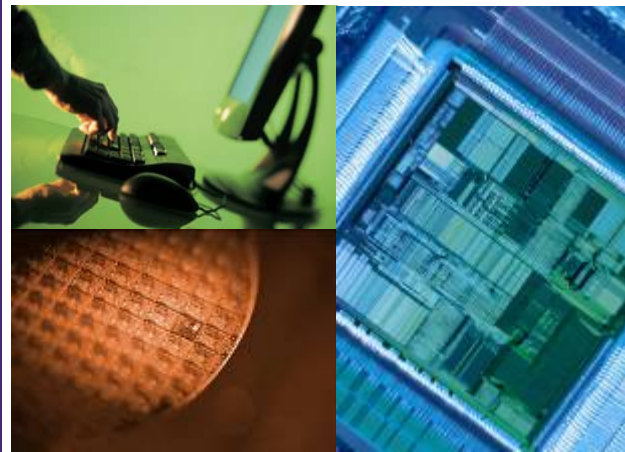


Welcome to the 20th EDA Interoperability Developers' Forum

sponsored by

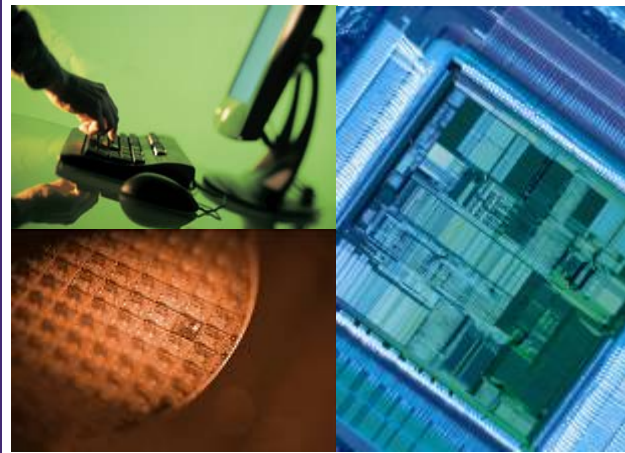


October 25, 2007



SYNOPSYS[®]
Predictable Success

Welcome to the 20th EDA Interoperability Developers' Forum



Rich Goldman
Vice President
Strategic Market Development

SYNOPSYS[®]
Predictable Success

20th – a momentous occasion

Traditional gift: China



What you've come to expect...

- Pertinent and interesting keynote presentation
 - “Low Power Design: The Third Revolution”
 - Michael Keating, Synopsys Fellow and Co-author of “Low Power Methodology Manual” (LPMM)
- Industry firsts
 - First public presentation of a new industry consortium
 - First LIVE interoperability demo using the proof of concept Interoperable PCell Library (IPL) and OpenAccess Analog Symbol Library (this morning)
 - First announcement of IPL Initiative Working Groups focused on PDKs (this announcement)
- Interesting breakout sessions
 - Low Power
 - Open Analog/Full-custom
 - VMM Methodology for SystemVerilog
- Plus prizes!

Stay informed. Get involved. Participate in the Process.

- Accellera www.accellera.org
- EDA Consortium www.edac.org
- EEMBC www.eembc.com
- IEEE www.ieee.org
- IPL Initiative www.IPLnow.com
- The Multicore Association www.multicore-association.org
- Open SystemC Initiative www.SystemC.org
- Si2 www.si2.org
- SPIRIT Consortium www.spiritconsortium.org
- And more!...



Introducing...



- Mission:
Accelerating silicon-on insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption
- Stay tuned for more information after the keynote presentation

Download Current Versions

- Synopsys Open Source Formats:

www.synopsys.com/partners/tapin

- Liberty 2007.03
 - Liberty Parser 2.4
 - 2007.03-1 adds documentation related to low power modeling *New!*
 - 2007.12 *Available in January*
- SAIF 2.0
- SDC 1.7
- vSDC 2005.12

- OpenVera: www.open-vera.com
 - 1.4.3 Testbench LRM *New!*
 - 1.4.1 Assertions LRM

Download Current Versions

- Milkyway Access Program (MAP-in):

- Milkyway Database Environment and C-API Z-2007.03 *New!*
- Milkyway Database Environment and C-API A-2007.12 *Available in March*

www.synopsys.com/partners/mapin

- Open SystemC Initiative:

- IEEE 1666™-2005 standard approved in December 2005
 - IEEE 1666-2005 LRM available at no charge
- SystemC 2.2 open source library released April 2007
- Transaction Level Modeling (TLM) 2.0
 - Public review of draft starting November 2007
 - Final approval scheduled by March 2008
- Upcoming Regional User Group meetings
 - www.systemc.org/community/user_groups
 - North America: November 7, 2007 in Massachusetts, USA
 - Europe: November 19, 2007 in Finland

www.SystemC.org *New!*
standards.ieee.org/getieee/1666



IEEE Download Current Versions

- IEEE Verilog and SystemVerilog standards merged into 1 document
 - Draft available now to active participants in P1800 technical committees
 - Feature freeze scheduled for February 2008
 - Full approval of the standard expected in early 2009
- If you are interested in participating, check out:
 - P1800 WG: <http://www.eda.org/ieee1800>
 - SV-AC (assertions): <http://www.eda.org/sv-ac>
 - SV-BC (design subset): <http://www.eda.org/sv-bc>
 - SV-CC (C-interface): <http://www.eda.org/sv-cc>
 - SV-EC (testbench): <http://www.eda.org/sv-ec>
 - SV-XC (Cross language): <http://www.eda.org/sv-xc>
- Find products, solutions, technical papers & more at Accellera's www.systemverilog.org

Verification Methodology Manual (VMM)

Proven Approach for Verification with SystemVerilog

- Jointly developed by ARM & Synopsys
- Provides coding guidelines and base classes for a layered testbench focused on reuse and randomization based coverage driven verification.
- Open to all

www.vmm-sv.org



The screenshot shows a web browser window titled "Verification Methodology Manual for SystemVerilog - Microsoft Internet Explorer". The page features a blue header with the title "Verification Methodology Manual for SystemVerilog" and navigation links for "NEWS", "ERRATA", "RESOURCES", "AUTHOR BIOS", "SystemVerilog", and "日本語". Below the header is a navigation bar with "> ARM" and "> SYNOPSIS". The main content area includes a 3D image of the manual book, the ARM and Synopsys logos, and a "What's Hot" section with a list of news items from 2007. A quote from Yoshiharu Funui, senior manager at STARC, is also present. At the bottom, there is a section titled "Verification Methodology Manual for SystemVerilog" with a brief description of the manual's purpose.

VMM Catalyst Program

- Join Synopsys' VMM Catalyst Program
 - Promotes the development and use of EDA tools, verification IP, training and services supporting the VMM verification methodology
 - Open to: EDA vendors, Verification IP companies, training and services providers
 - Qualified access to Synopsys' SystemVerilog-based tools VCS[®], Pioneer-NTB and VCS Verification Library
- Use the VMM Standard Library Source Code
 - C Class Library that implements the VMM
 - Available under separate license agreement
 - Licensee may redistribute compiled/encrypted versions of the unmodified source code

www.synopsys.com/partners/vmmcatalyst/vmmcatalyst_program.html

50+ VMM Catalyst Program Members

Tools • IP • Services • Training



Check out “The Standards Game”


www.synopsysoc.org/thestandardsgame

- A new blog by Karen Bartleson

The Standards Game - Microsoft Internet Explorer

File Edit View Favorites Tools Help

The Standards Game

Synopsys  Open Community.org
An online forum for electronic design professionals

SynopsysOC

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1. Life In The Standards Lane
2. Skirmishes, Battles And All-Out Wars
3. Duh.
4. Be There Or Be Square
5. Travel Tales
6. Decoder Ring
7. Just Me

Archives

October 2007

Is there any hope for a single low power standard?

Posted by [karenb](#) on October 18th, 2007

About a year and a half ago, the electronic design automation industry, along with its customers designing low power integrated circuits, began efforts to create a standard to describe low power design intent for implementation, analysis, and verification.

Today, there are two standards in play: UPF (Unified Power Format) and CPF (Common Power Format). UPF was developed by Accellera using donations from seven companies, while CPF was donated to Si2's Low Power Coalition by Cadence Design Systems.


Just about everyone I know wants there to be a single standard. Supporting two standards is costly to suppliers and customers alike.

Is there any hope that there will be a single standard for low power design? I, the optimist, say "Yes"!

Within the IEEE, a working group is actively moving towards ratification of IEEE standard 1801. Participants in the group are from both Accellera's UPF technical subcommittee and Si2's Low Power Coalition. The results of the Low Power Coalition's CPF/UPF comparison study have been shared with the IEEE working group to help ensure completeness of their standard-in-progress, with UPF forming the basis of their work.

I expect that when the 1801 standard is sanctioned by the IEEE, the

About



I can hardly believe it. I've been in the EDA business since 1980 when I joined TI's Design Automation Department after graduating from Cal Poly with my BSEE. Since 1995, much of my attention has been focused on EDA standards. I reached a moment of truth this year when I admitted, albeit reluctantly, that I could be called a standards-lifer. So, I decided it's time to share my perspectives on what's going on in the standards arena. Welcome to my blog - I can't wait to hear from you!
- Karen Bartleson

Recent Posts

Is there any hope for a single low power standard?

7th Annual Tenzing Norgay Interoperability Achievement Award

- Presented to a company that
 - Surpasses common levels of interoperability
 - Contributes to overall industry advancement
 - Provides a new view of the future
 - Ensures customer success



*Tenzing Norgay
on Mt. Everest*



Previous Award Winners

- **2001: CoWare**
- **2002: Mentor Graphics**
- **2003: Silicon Metrics**
- **2004: Novas Software**
- **2005: ARM**
- **2006: Electronic Tools Company**



And the winners are...



The  **UNIFIED POWER FORMAT** founding team



8th Tenzing Norgay Award

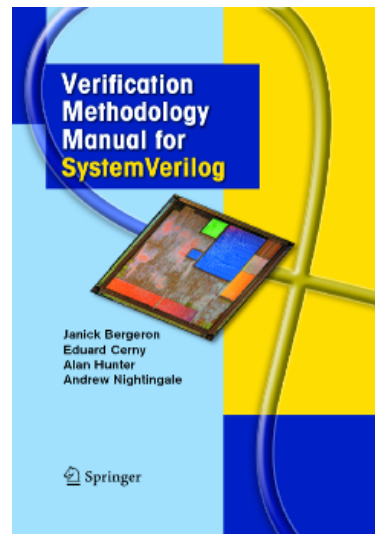
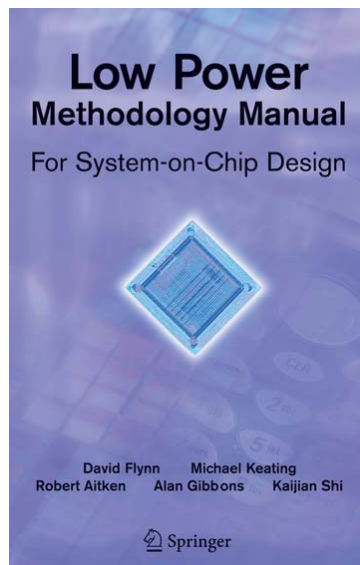
- Will be presented at the DAC 2008 Interoperability Breakfast
 - Wednesday, June 11, 2008
- Nominations are active for 3 years



Call for nominations now until April 11th
<http://www.synopsys.com/tapin/tnorgay>

Presentations & Prizes...

- Presentations will be available for download from the web starting today:
www.synopsys.com/devforum/oct2007/presentations
- Early birds get the worms
 - \$15 Starbucks gift cards to first 10 attendees
 - Synopsys AMS Thermos bottles
 - IPLNow insulated lunch bags
- Keep your raffle ticket and complete your feedback forms to be eligible to enter drawings* for more prizes:
 - *Low Power Methodology Manual* by ARM and Synopsys
 - *Verification Methodology Manual for SystemVerilog* by ARM and Synopsys
 - Apple iPod® players



*Must be present to win



Mark Your Calendar!

21st EDA Interoperability Developers' Forum

- April 2008
- In Silicon Valley
- Invite your colleagues
- Want to speak? Let us know.

See you then!

Today's Agenda

- Interoperability of Analog/Full-Custom Flows *This morning*
- Integrating with VMM Methodology for SystemVerilog *This morning*
- Lunch featuring IPL Member Showcase
- General Session *12:15PM – 2:15PM*
 - Keynote Presentation *The Low Power Revolution*
Michael Keating, Synopsys Fellow and Co-author of “LPMM
 - Introducing the SOI Industry Consortium
 - Liberty UPF/Low Power Checklist
 - Liberty Technical Advisory Board Updates
- The Power of One: UPF on the Path to IEEE Ratification *2:15PM – 4:30PM*
 - Getting Started with UPF/P1801
 - “Keeping Locals Local” by NXP Semiconductors
 - UPF Support Blitz

Enjoy your 20th EDA Interoperability Developers' Forum

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