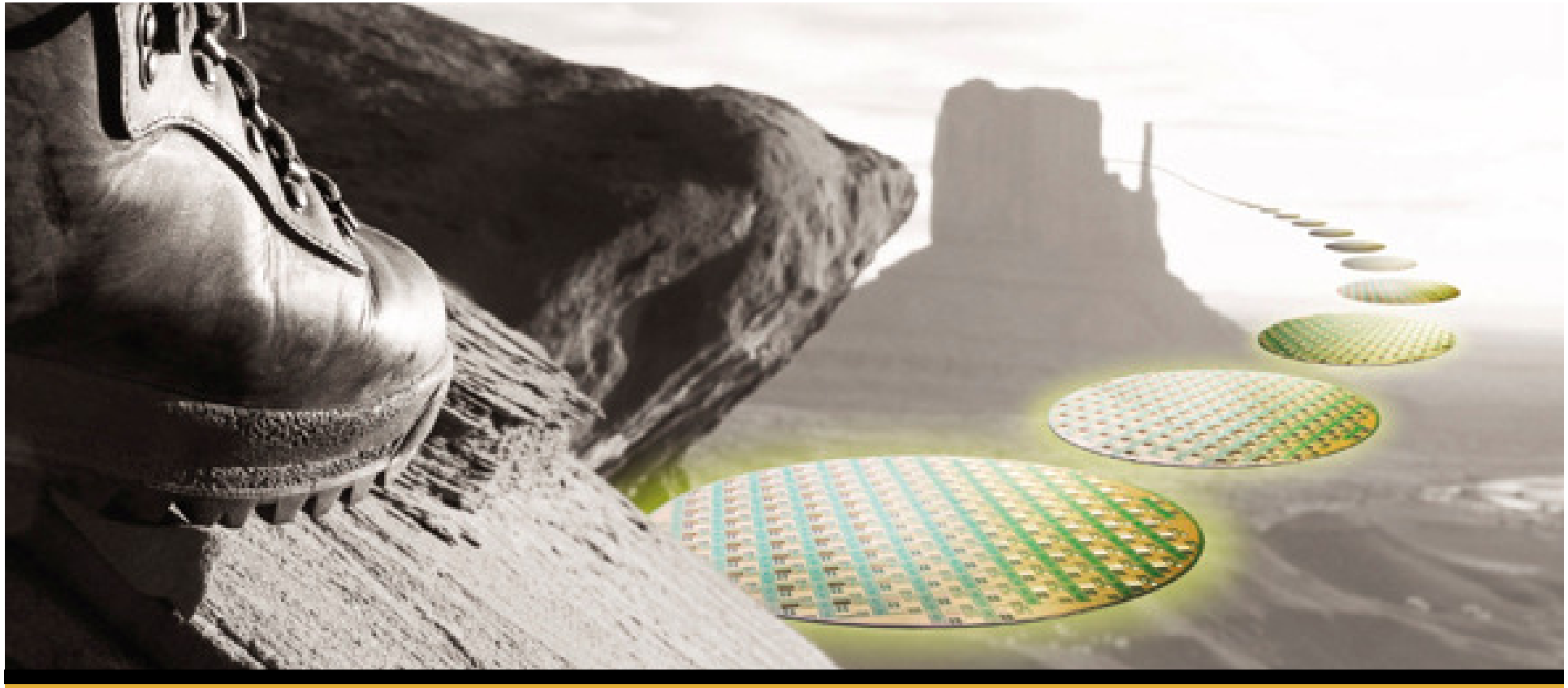

Moving Forward With Power Formats

Oscar M. Siguenza, Director Platform Infrastructure

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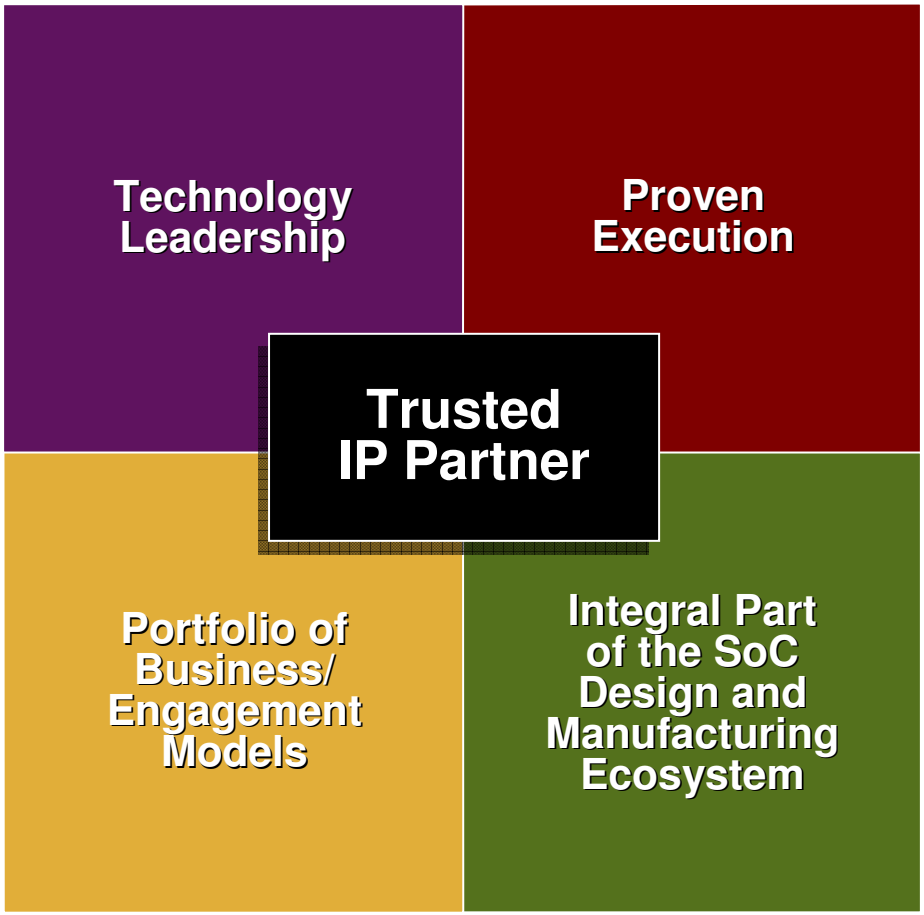
Agenda

- Why care about power formats?
- Standards: hindrance or solution?
- Where do we go from here?

Virage Logic's Trusted IP Partner Qualifications



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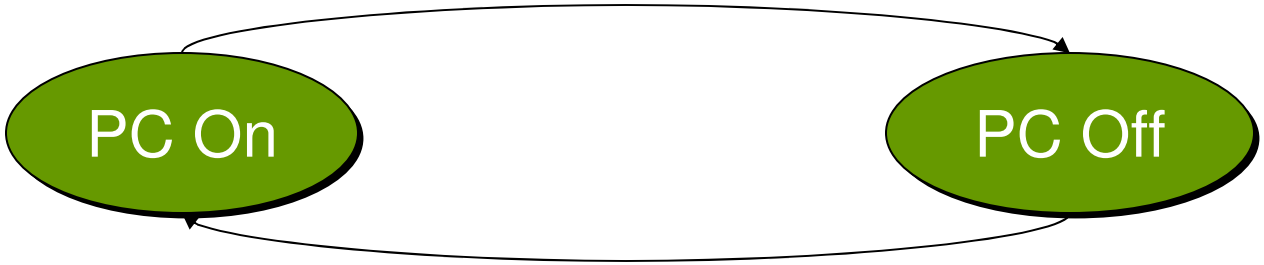
Why Care About Power Formats?

- Technology scaling is driving the need for standard low-power techniques
  - Leakage increasing as a proportion of total power
  - Current increasing as voltage scaled
  - Integration increases leading to transient activity in sections of design
- Mobile convergence devices challenging performance and power requirements
- Lack of significant battery improvements leading to need for clever design techniques to extend battery life
- Large part of the market driven by all these requirements

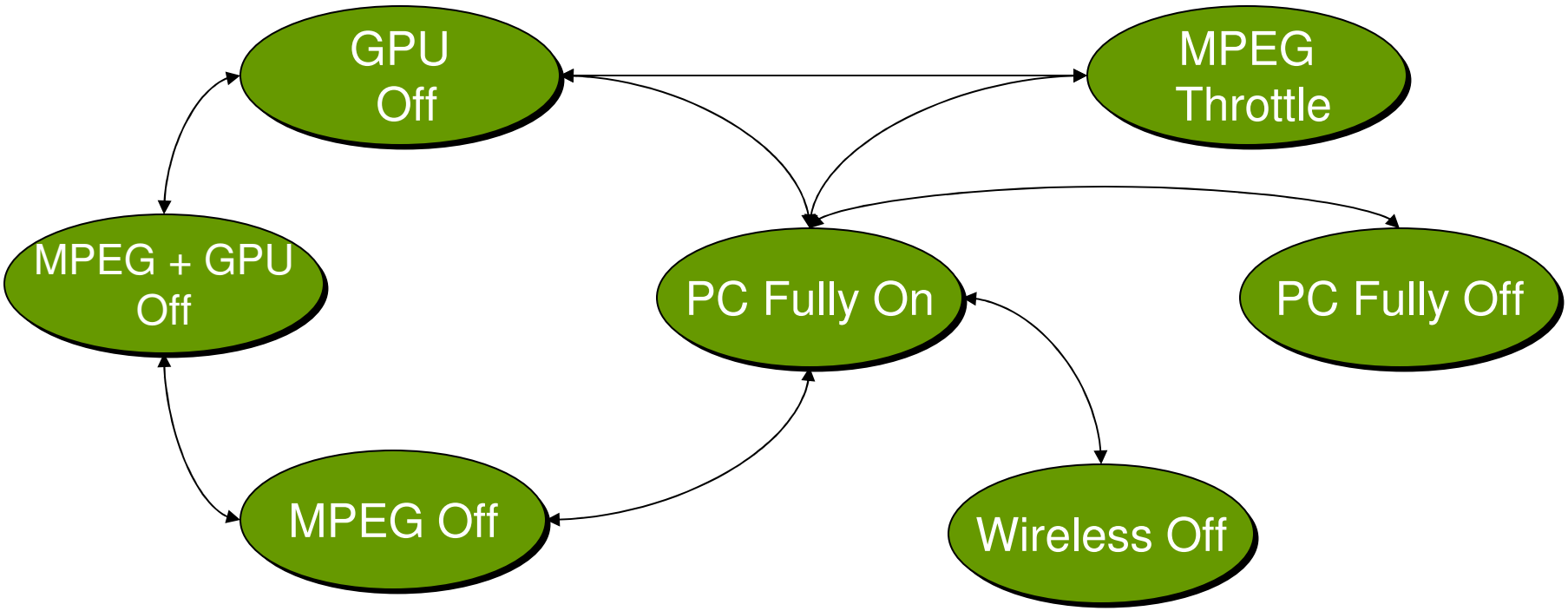
So, what could possibly go wrong?

What Happened To My Golden Source?



VDD Global
VSS Global

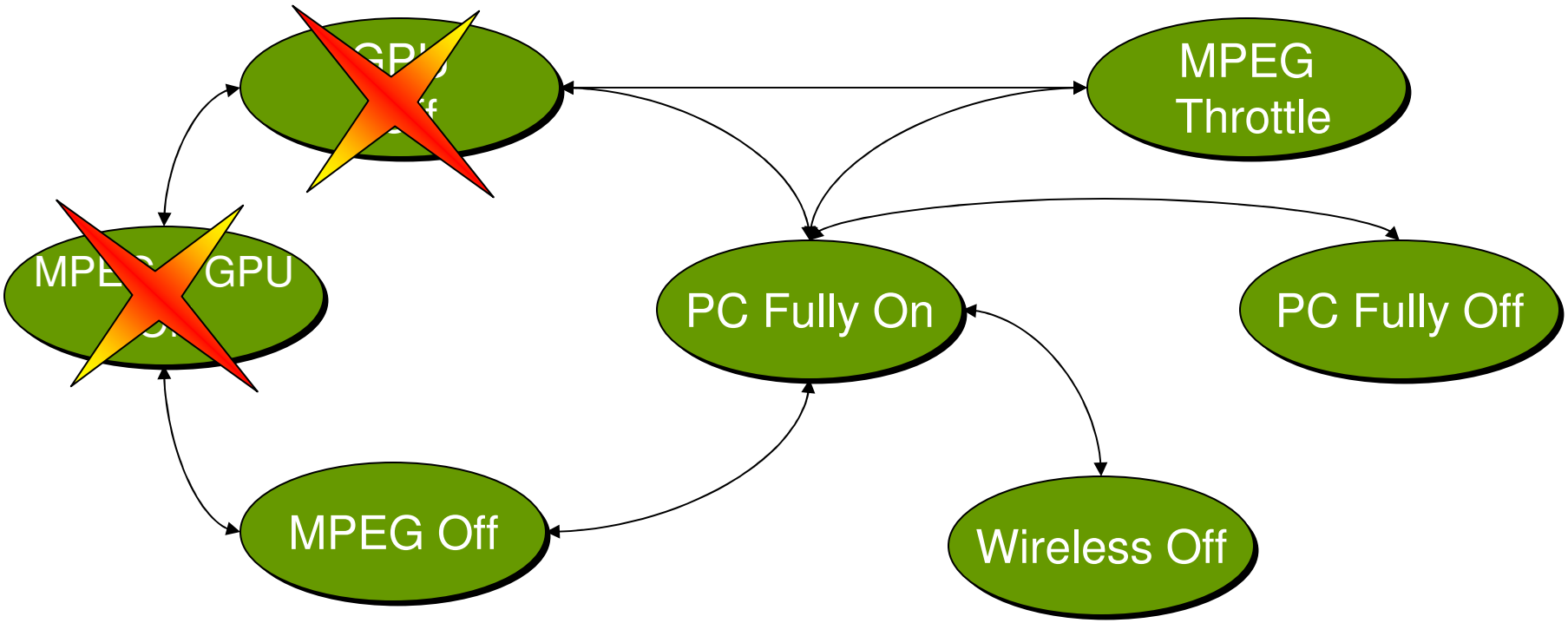
What Happened To My Golden Source?



GPU = VDD1, VSS
MPEG = VDD2, VSS, VBN
Wireless MAC/PHY = VDD3, VSS
Others = VDD, VSS

Wait!
- VDD2 Derived from VDD1
- Two States Equivalent

What Happened To My Golden Source?



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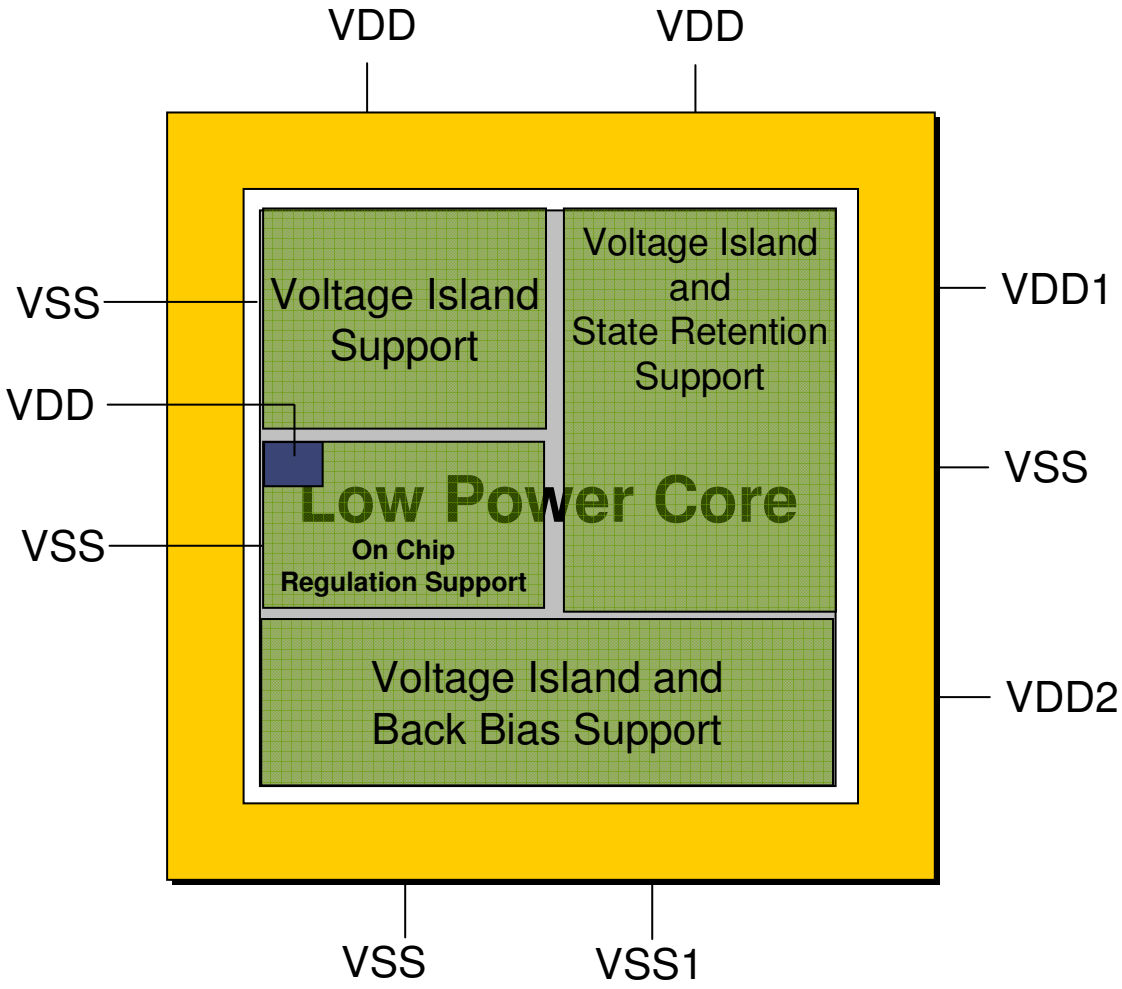
What Happened to My Power Nets?



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Standards … Hindrance or Solution?

- Standards can be both
- When are they a hindrance?
  - Open, but not really open?
    - To be effective a standard needs to be available to all players
    - Any standard that is used to shut out competition, should not be considered a good standard
  - Limited in scope
    - Any standard that does not allow for optimization options, should not be considered a good standard
    - Ensuring potential for innovation in design, is critical for a good standard
- When are standards' solutions?
  - Open, widely available and widely used
    - Allows for good peer review and robustness, as well as low-overhead cost
  - Allows for evolution when design innovation would be improved

Moving Forward …

- UPF fits the definition of a good standard
  - Widely available
  - Subject to peer review
  - Evolving in real-time
- Virage Logic is helping to evolve UPF
  - Making sure the standard is expressive enough to deal with rich low-power IP
  - Ensuring consistent semantics between different vendor tools
  - Making sure that correct electrical rule checks can be implemented for robustness of design

Forward With Power At Virage Logic

- Design has been created to showcase the following IP
  - State retention
  - Always-on cells
  - Level shifters/isolation cells
  - Power gating
  - Back bias
- UPF defines syntax for description of IP and constraining of design
  - Need additional view information to complete design flow and ensure correct semantics for power-aware flow

Forward With Power At Virage Logic

- Generating required primary views
  - Power format constraints and IP directives
  - Liberty description of IP
  - Verilog description of IP
  - LEF description of IP
  - LVS description of IP
  - GDS layout of IP
- Once common infrastructure IP and design is complete and described
  - Implementing RTL to GDS design flow
    - Layout QOR
    - Timing QOR
    - Verification QOR

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Forward With Power At Virage Logic

- Initially concentrating on physical implementation and verification
  - Required to ensure smooth IP tape out
- Currently working on creation of “derived views”
  - Milkyway
  - Volcano
- Overall goal
  - Single source of power constraint data
  - Single source of primary views
  - Wide usage and consistent QOR across different vendor tools
  - Applicability of techniques across multiple technology nodes
    - 180-nanometer (nm) to 45nm and beyond

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Conclusions

- As the industry's trusted IP partner, Virage Logic is committed to ensuring open standards for power-aware design
- Actively working with the different standard bodies to maintain consistency
- Working together with various partners to ensure consistent syntax, semantics, and QOR