

IEEE P1801 Working Group (Unified Power Format – UPF) Status

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On behalf of
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Chair, P1801 Working Group

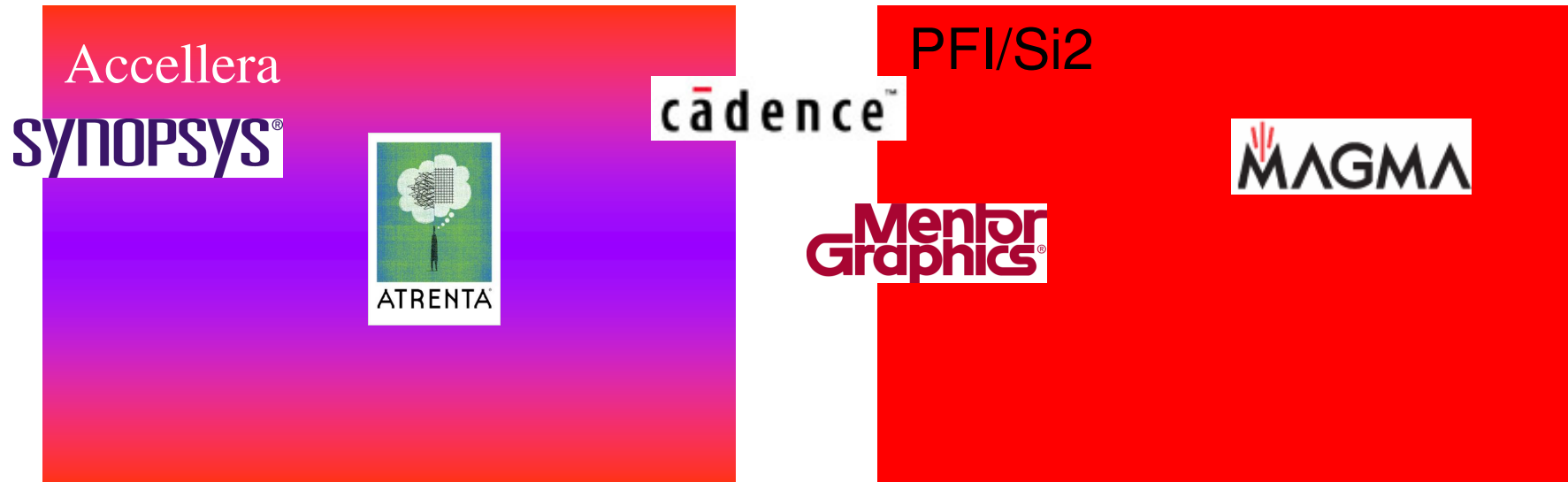
Agenda

- Origins of UPF
- Accellera UPF Standard
- IEEE P1801

Origins of UPF

- Origins for a standard format for capturing low power design intent
 - Multiple vendors developed their own solutions to a problem their customers brought to them
 - Synopsys
 - Magma
 - Mentor
 - Cadence
 - Atrenta
 - ArchPro
 - ...
 - Users realized a standard is needed for tool interoperability
 - Redundant specification; ripe for inconsistencies and bugs
 - Vendor independence

DAC 2006: Users Request an Open, Fast, Inclusive Standard



- Industry rallied to respond
- Accellera successfully organized all but one vendor to converge their formats into a single format – UPF
 - Cadence participated in all but 1 Accellera UPF meeting
 - But declined to contribute their format (CPF) to the effort
- UPF is the industry converged standard

Agenda

- Origins of UPF
- **Accellera UPF Standard**
- IEEE P1801

Accellera & IEEE Structure

- Anyone can attend Accellera and IEEE meetings
- Anyone may donate (assign copyrights) of technology for use in creating a derivative work
- No essential patents have been asserted for UPF
- Anyone may provide technical contribution
 - Non members providing technical input to UPF:
 - Nordic Semiconductor
 - ArchPro
 - ChipVision
 - NXP
 - IBM
 - Intel
 - Infineon
 - VaST
 - Virage Logic
- All members have equal voting rights; majority approval

Accellera UPF 1.0 Sets Record

- Sep 2006, Accellera UPF Technical SubCommittee (TSC) starts
- Feb 2007, Five months later, Accellera approves the UPF standard
- May 2007, IEEE WG is approved and Accellera executes copyright assignment
- Mar 2008, IEEE P1801 UPF standard goes to ballot

UPF is *the* Industry Standard

- A single format serving entire low-power solution
- Extension of logic specification for low-power design intent
- Consistent semantics for implementation and verification

UPF Participating Companies

- | | |
|--------------|------------------|
| • AMD | • Nordic Semi |
| • ARM | • Novas |
| • Atrenta | • NXP |
| • Azuro | • Qualcomm |
| • ChipVision | • Si2 |
| • FreeScale | • STARC |
| • IBM | • STM |
| • Intel | • Synchronous DA |
| • Infineon | • Synopsys |
| • LCDM Eng | • TI |
| • LSI Logic | • Toshiba |
| • Magma | • VaST |
| • Mentor | • Virage Logic |
| • Nokia | • Xilinx |

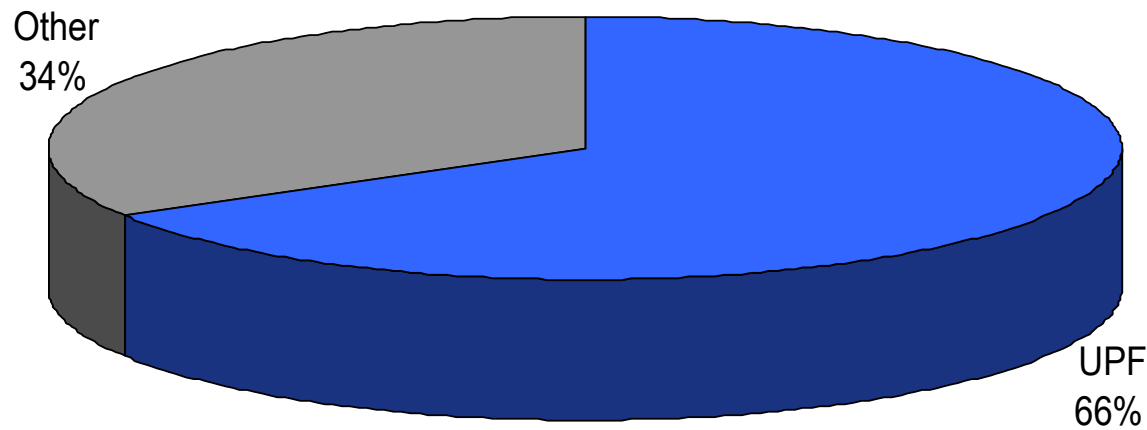
Download UPF Spec freely
<http://www.accellera.org/>



Industry Support for UPF

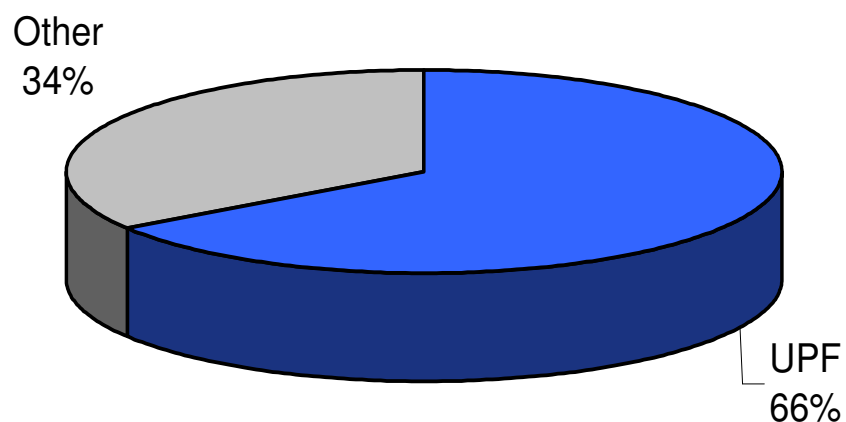
UPF EDA Support – Digital Design

COT/ASIC/FPGA Synthesis + Physical Implementation + DFT + Signoff



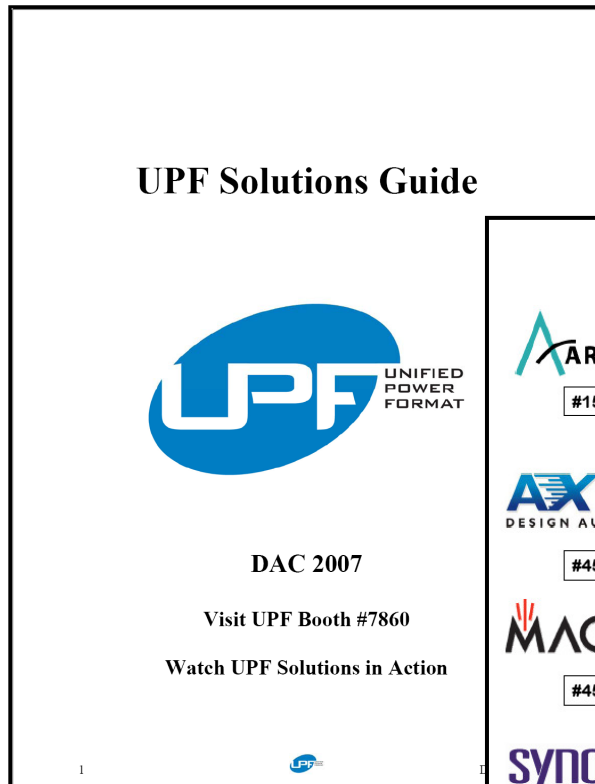
Based on Q4 05 through Q3 06 EDAC MSS data plus other publicly available market data

UPF EDA Support – Digital Simulation



Based on 2007 John Cooley DeepChip DevCon Survey “Mindshare” – 818 Respondents

Catalog of UPF Products



Company	Product	Usage
ArchPro	MaVeric	Verification
Atrenta	Spy Glass-Power	Analysis
Axiom	MPSim	Verification
Azuro	PowerCentric	Implementation
Magma	Talus Power	Implementation
Magma	Quartz Rail	Analysis
Mentor	Questa	Verification
Mentor	FormalPro	Verification
Springer	LP Methodology Manual	How-to Book
Synopsys	DesignWare IP	IP blocks
Synopsys	VCS	Verification
Synopsys	Design Compiler Ultra	Implementation
Synopsys	Power Compiler	Implementation
Synopsys	DFT Compiler/MAX	Implementation
Synopsys	Leda	Analysis
Synopsys	Formality	Verification
Synopsys	IC Compiler	Implementation
Synopsys	PrimeTime/PX,SI	Analysis
Synopsys	PrimeRail	Analysis
Synopsys	TetraMAX	Implementation
Virage	Silicon Aware IP	Low Power Libraries

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- Origins of UPF
- Accellera UPF Standard
- **IEEE P1801**

IEEE P1801 WG Approved May 2007

- Request for donations were submitted to Accellera and Cadence/LPC
 - Accellera immediately responded with assignment of copyright
 - Si2 LPC declined to assign copyright for CPF to create a derivative work
 - This ended any possibility of a single low power format
 - LPC did make available to the IEEE WG “differences” document
 - LPC users brought the document into IEEE to ensure full capabilities of UPF and hope it will ease future translations to/from the formats

Goals of IEEE P1801 Standardization

- Incorporate bug fixes & enhancements related to experience implementing UPF 1.0 support
- Enhance to better meet use models
- Enhance to raise abstraction

IEEE P1801 Participants

- Voting Attendees

- Accellera
- ARM
- Infineon
- LSI
- Magma
- Mentor Graphics
- Synopsys
- TI

- Non-Voting Attendees

- ChipVision
- Intel
- Nordic
- NXP
- Bhanu Kapoor, Self
- Joe Daniels, Self

Chair: Steve Bailey, Mentor Graphics

Vice-Chair: Gary Delp, LSI

Monitoring P1801 Activity

- Mantis database for Issue Tracking
 - All issues are logged for entire life-cycle
 - Creation, discussion, resolution, doc
 - <http://www.eda-stds.org/mantis> (need login)
- Minutes of Meeting, hypermail tracking
 - <http://www.eda-stds.org/p1801/hm>
 - http://www.accellera.org/activities/p1801_upf
- Discussion on Reflector
 - p1801@eda.org

P1801 Schedule

- Weekly telecons (Tues mornings)
- Monthly Face to Face Meetings
 - Sep: 19-21 at ARM in Cambridge
 - Oct: 17-19 at TI in Dallas
 - Nov: 12-13 at Magma in San Jose
 - Dec: 10-12 at Infineon in Munich
- Draft standard for WG review:
 - Feb 2008
- Enter IEEE ballot:
 - Mar 2008
 - Complete balloting May/June 2008

Thank You