



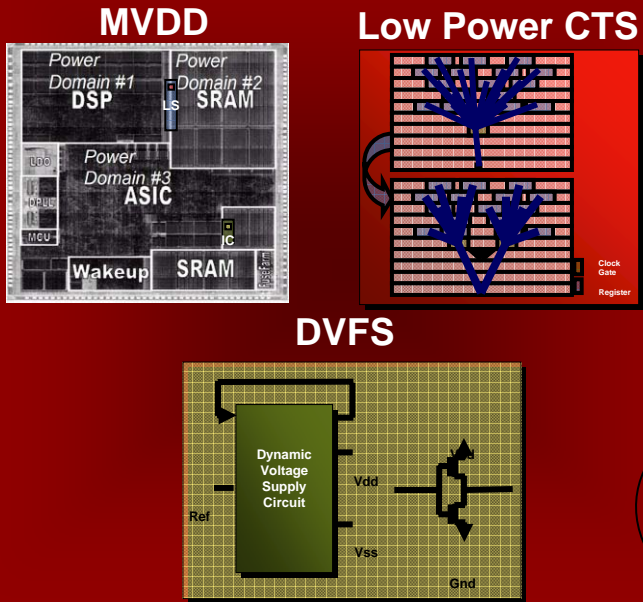
UPF Low Power Flow

October 2007

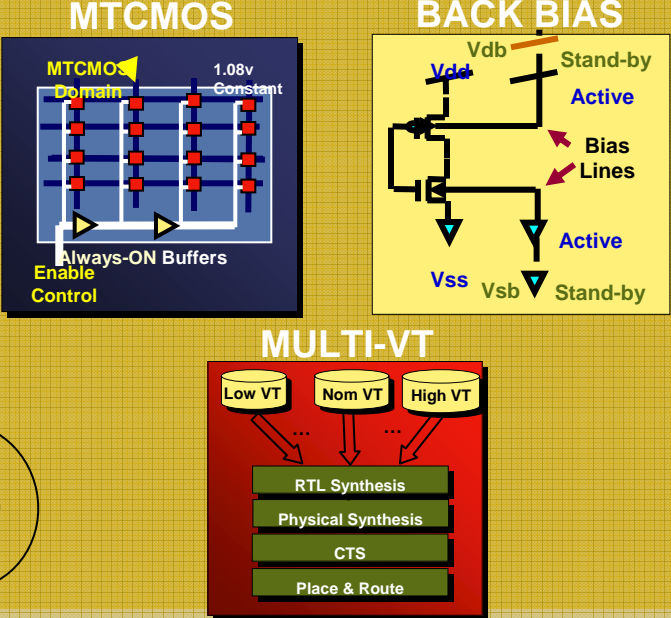
For 20th Synopsys EDA Interoperability Developers' Forum attendees only

Magma Unified Low Power System

Dynamic Power Reduction

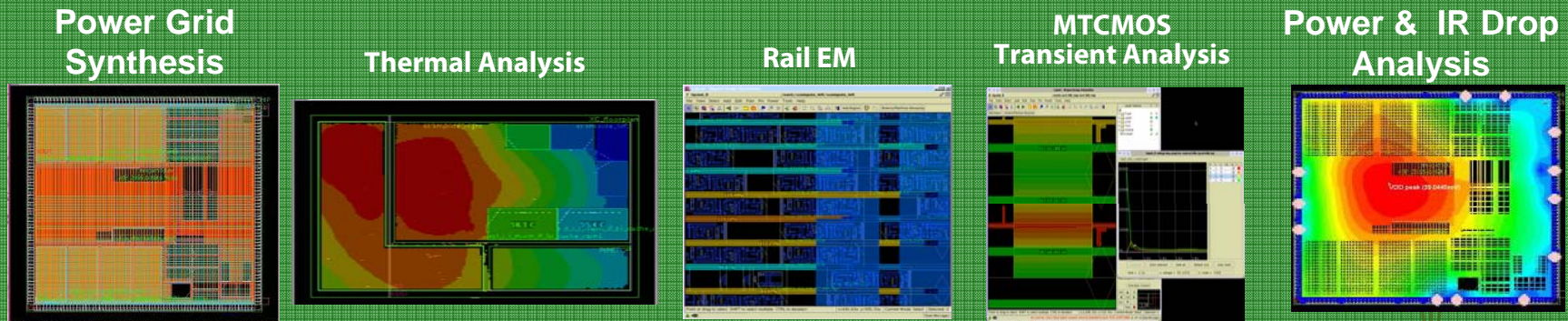


Leakage Power Reduction

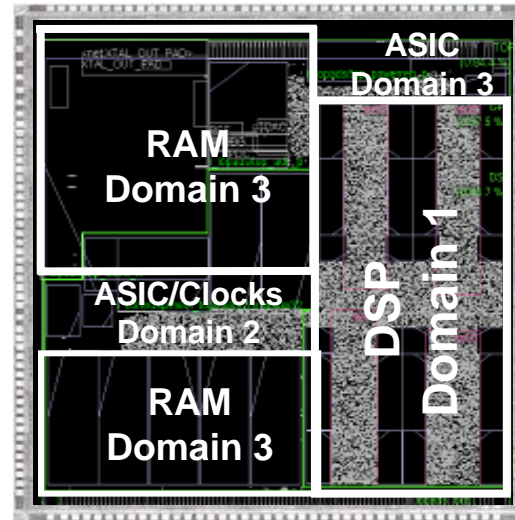
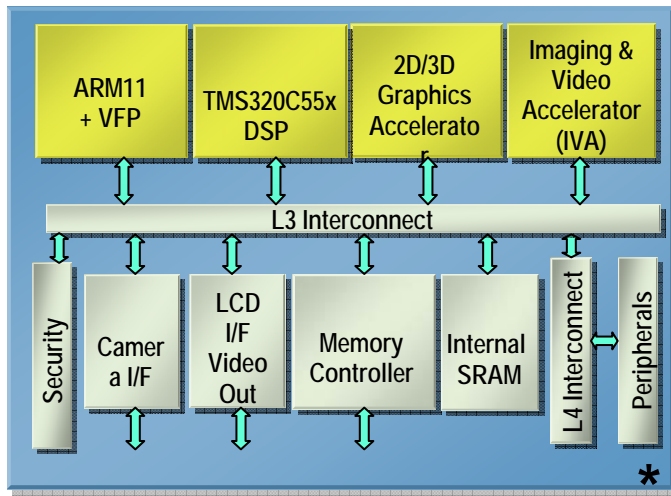


Talus
Power
Pro
&
Quartz
Rail

Power Analysis & Implementation



Advanced Low Power Techniques for Mobile Devices



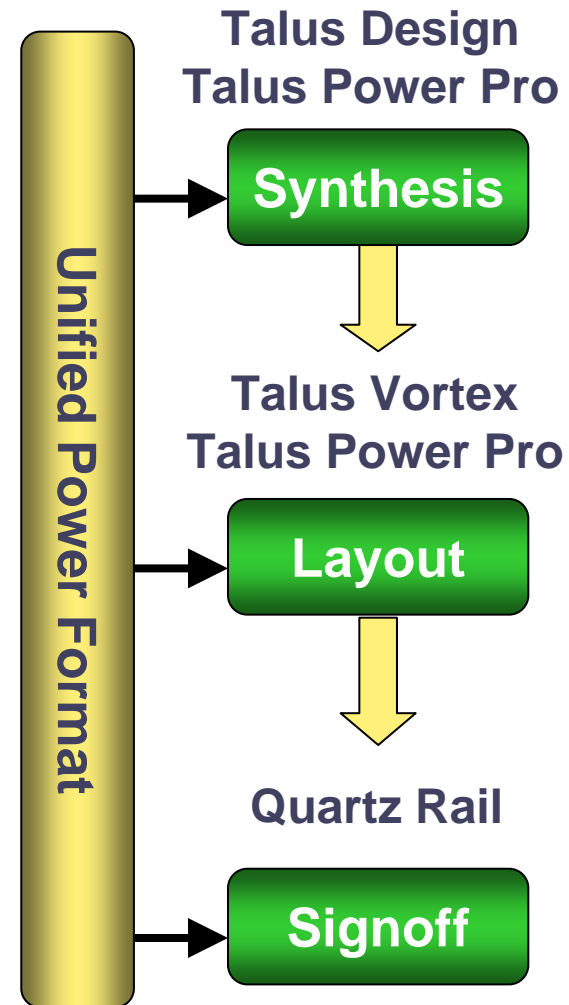
- Clock Gating
- Power aware CTS
- Retention flop synthesis

- MTCMOS
- Isolation cells
- Back-Bias (VTCMOS)

- Multi-VDD
- DVFS
- Level Shifters
- Multi-Vt

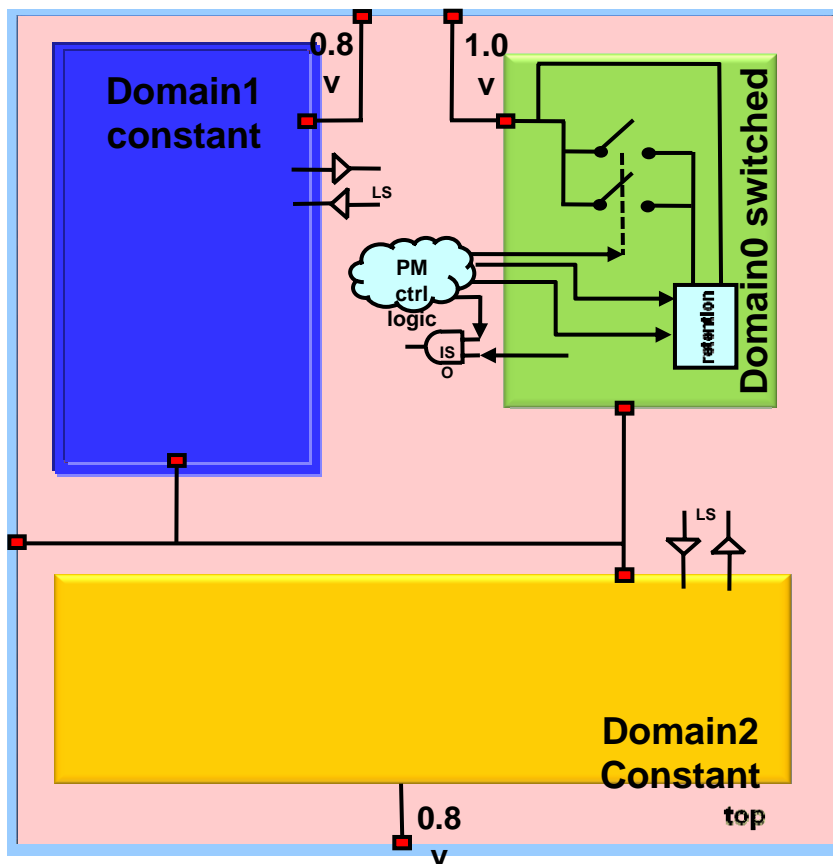
UPF Based Flow in Magma

- **Domain Definition**
 - Power domains
 - Supply rails
- **Domain Relationship**
 - Power state tables
- **Special Cells**
 - Retention
 - Isolation
 - Level shifters
 - Switches



Defining Domains and Electrical Conditions

Logical → Electrical → Physical



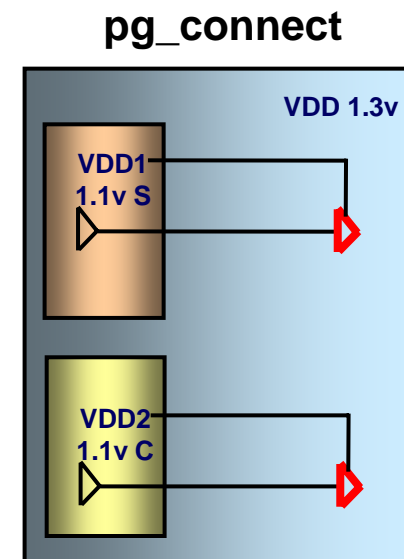
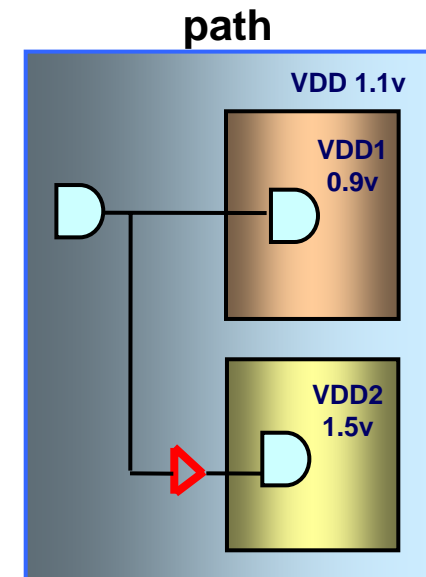
UPF Commands

```
create_power_domain
add_domain_element
connect_supply_net
create_supply_net
create_supply_port
get_supply_net
merge_power_domains
set_domain_supply_net
```

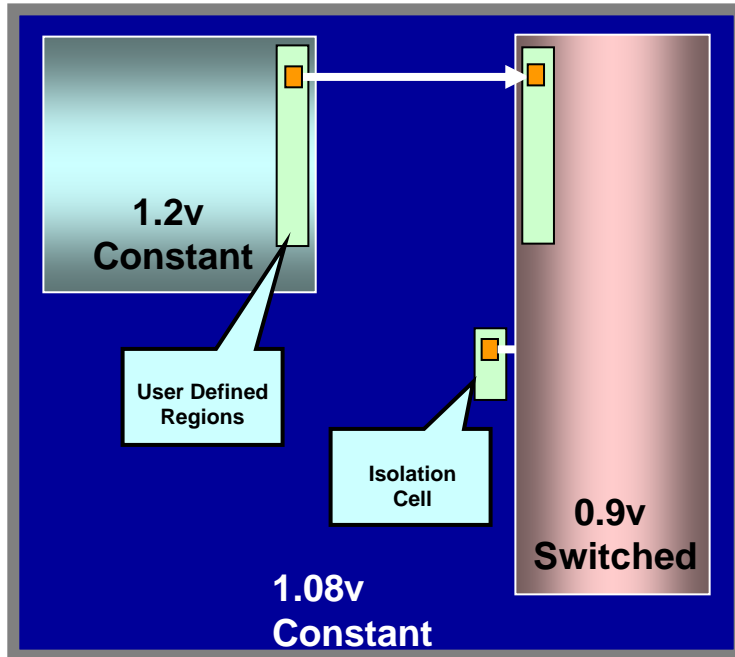
Level Shifters in MVDD flows

Level shifter considerations:

- Pick a power domain or a set of elements
- Select input ports, output ports, or both
- Tolerate a voltage difference threshold
- UP shift or down SHIFT rule
- Location (self, parent, sibling, fanout, auto)
- Insert or not insert



Level Shifter insertion using UPF



Supply Type

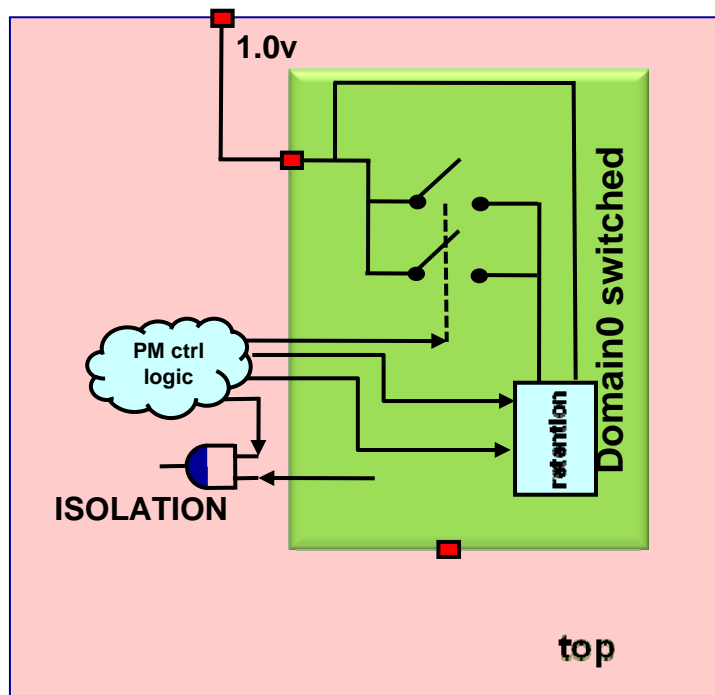
- Constant
- Variable
- Switched constant
- Switched variable

UPF Commands

```
set_level_shifter  
map_level_shifter
```

- Automatic rule based insertion
- Length dependant and IR drop dependent Insertion
- Electrical Rule Checks to identify domain relationships
- Well spacing rules honored

Isolation Cells for Shut Down Domains



UPF Commands

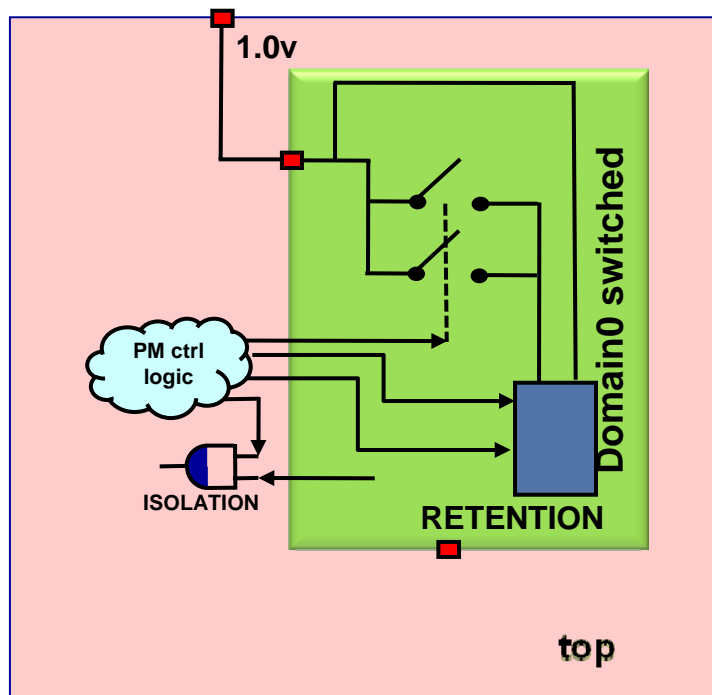
```
set_isolation  
set_isolation_control  
map_isolation_cell
```

- Automatic placement close to domain boundary
- Options for clamp "0" or "1"

Retention Flops in Shut Down Domains

UPF Commands

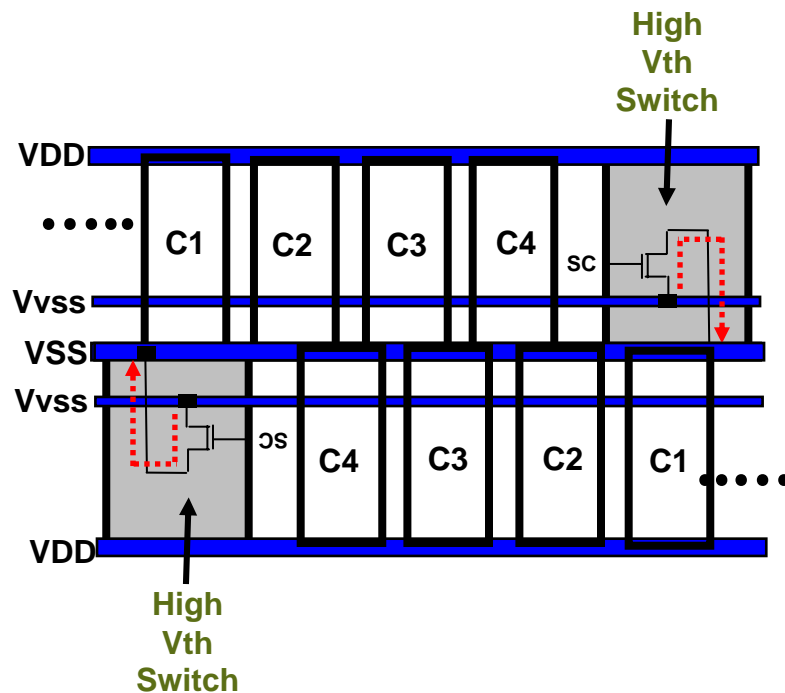
```
set_retention  
set_retention_control  
map_retention_cell
```



- **Maintains state of domains that are powered down**
- **Automatic placement and power connectivity**

Switch Cell inference using UPF

Distributed MTCMOS



UPF Commands

```
create_power_switch
set_power_switch
map_power_switch
```

- Distributed MTCMOS
- Fine Grain
- Global
- Standard cell specific
- Grid based insertion

Power State Table

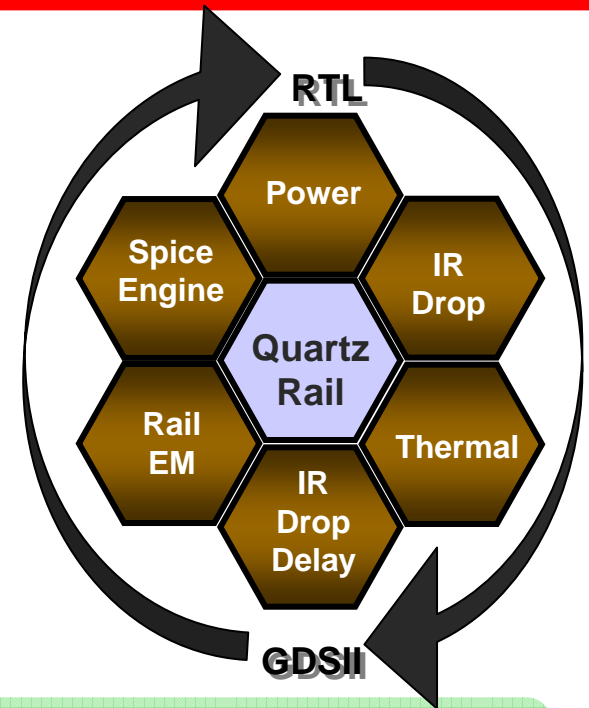
- A *power state table* defines the legal combinations of states for different domains
- **create_pst** command creates a PST, using a specific order of supply nets during operation of the design
- Each row defines a valid combination of supply states
- Power states enable optimization and verification
 - Infer or verify level shifters and isolation gates

UPF Commands

```
create_pst  
add_pst_state
```

Power Integrity Sign-Off – Quartz Rail

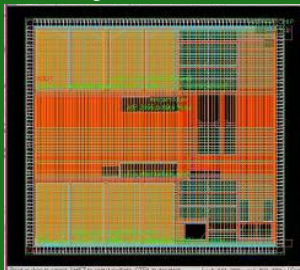
- Power/IR drop sign-off solution to ensure power network integrity
- Accuracy
 - Built-in spice engine for sign-off accuracy
 - Static & transient power & IR drop analysis
- Integration
 - Concurrent optimization and analysis for optimal QoR
 - IR drop induced delay
- Predictability
 - RTL-to-GDSII power sign-off accuracy with early predictability



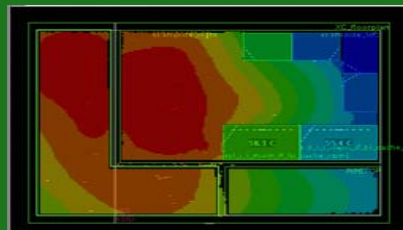
Support for SAIF

Power Analysis

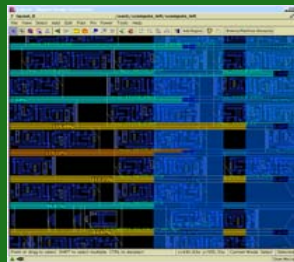
Power Grid Synthesis



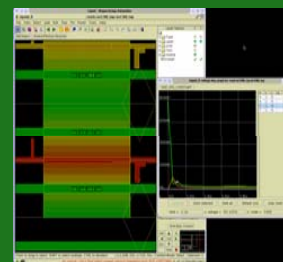
Thermal Analysis



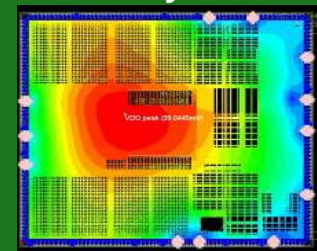
Rail EM



MTCMOS Transient Analysis



Power & IR Drop Analysis



Thank You