

Atrenta Support of Unified Power Format (UPF)

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Interoperability workshop
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The Need for a Power Standard

- **Power-aware design requires specification of power intent**
- **No existing standard for power intent specification**
 - Power intent described in Atrenta SGDC format for SpyGlass
 - Other EDA tools have proprietary formats
 - Customers have internal formats
- **Power standard is important**
 - Consistent power intent throughout the design flow
 - Interoperability between EDA tools
 - Ease of adoption and consistent results from power-aware design tools
- **Atrenta power solution**
 - Voltage and power domain verification
 - Power domain sequencing verification
 - Domain-aware power estimation
 - Power reduction and planning

Atrenta Support for UPF

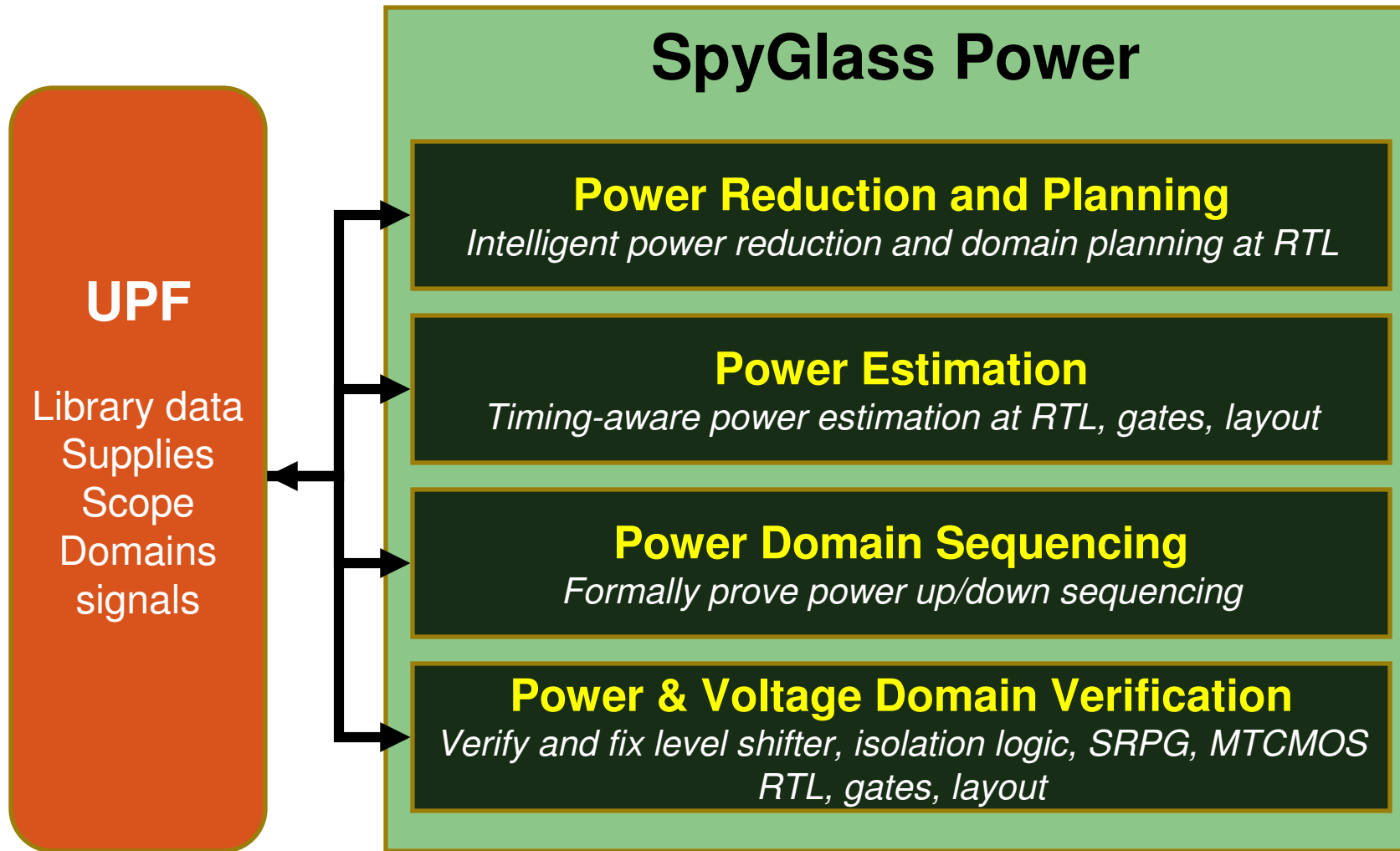
■ Atrenta is an active participant in UPF

- Strongly support efforts for unification of power formats and IEEE standardization
- Donated SpyGlass SGDC format to Accellera in 2006
- Participate in technical sub group (TSG) & IEEE p1801 working group

■ Atrenta is working closely with customers for UPF support in SpyGlass Power

- Provide a transition path from/to SpyGlass SGDC format to/from UPF
- Ensure UPF support in SpyGlass is adequate and robust for use in design projects
- Work with UPF members to resolve any tool interoperability issues

SpyGlass Power Requirements from UPF



UPF Support in SpyGlass Power

The screenshot displays the SpyGlass Desktop interface. The main window shows a Verilog module named `simple1` with inputs `a, b, VDD1, VDD2, GND` and output `x`. It includes level shifters `LS21` and `LS12`, and a block `ua`. A warning in the Message Tree indicates an incorrect power connection for `VDD1` and `VDD2`. An xterm window shows the translated UPF file, which defines power domains `VDD1` and `VDD2`, level shifters `LS12`, and supply nets.

```

module simple1 (a, b, x, VDD1, VDD2, GND);
  input a, b, VDD1, VDD2, GND;
  wire aw, bw, xo;
  output x;
  LS21 lea (.I(a), .O(aw), .VDDI(VDD2), .VDDO(VDD1), .VSS(GND));
  LS21 leb (.I(b), .O(bw), .VDDI(VDD1), .VDDO(VDD2), .VSS(GND)); // wrong
  LS12 lex (.I(xw), .O(x), .VDDI(VDD1), .VDDO(VDD2), .VSS(GND));
  blockA ua (.a(aw), .b(bw), .x(xw), .VDD(VDD1), .VDD2(VDD2), .GND(GND));
endmodule

module blockA (a, b, x, VDD, GND);
  input a, b, VDD, GND;
  output x;
  wire aw, bw, xo;
  LS12 lex (.I(xw), .O(x), .VDDI(VDD), .VDDO(VDD), .VSS(GND));
endmodule
    
```

Message Tree:

- lowpower[2] (WARNING -> 2)
 - LPPLIB04[2]:Ensure level shifters are connected to two supplies
 - Incorrect Power Connection for in-supply terminal 'VDD1'
 - Incorrect Power Connection for out-supply terminal 'VDD2'
- spyglass[1] (INFO -> 1)

xterm1 Translated SGDC UPF:

```

current_design simple1
supply -name VDD1 -alwayson 1 -value 1.0
supply -name VDD2 -alwayson 1 -value 2.0
voltage_domain -name Vtop -modname simple1 -value 2.0 \
  -supplyname VDD2
voltage_domain -name VA -instname simple1.ua -value 1.0 \
  -supplyname VDD1

levelshifter -name LS12 -from VA -to Vtop \
simple1gate.sgdc_from_upf 1,1 Top
set_design_top simple1

# Logical information
create_power_domain Vtop -elements simple1
create_power_domain VA -elements simple1.ua
set_level_shifter A_to_top -domain VA -applies_to outputs
set_level_shifter A_to_top -domain Vtop -applies_to inputs
set_level_shifter top_to_A -domain Vtop -applies_to outputs
set_level_shifter top_to_A -domain VA -applies_to inputs

# Physical information
create_supply_net VDD1
create_supply_net VDD2
set_domain_supply_net Vtop -primary power net VDD2
simple1gate.upf 1,1 Top
    
```

Terminal Output:

```

pft.tcl
usage: pft.tcl {sgdc|cpf|upf|none} infile [outfile]
pft.tcl sgdc simple1gate.upf simple1gate.sgdc_from_upf
    
```

Translation command line: simple1gate.upf 1,1 Top