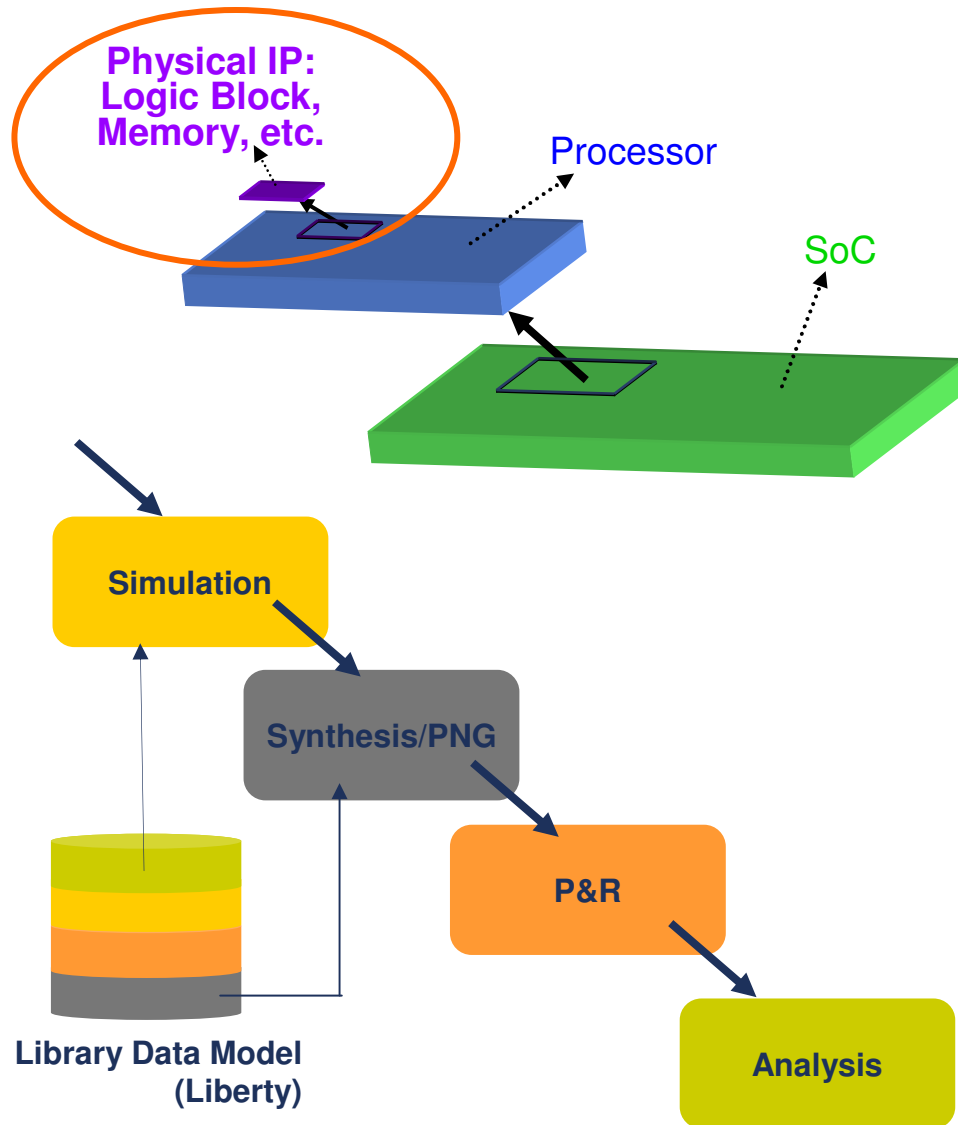




Managing Power:
ARM Physical IP &
The Power of One

Leah Schuth
ARM Physical IP
October 2007

Low Power Physical IP Integration

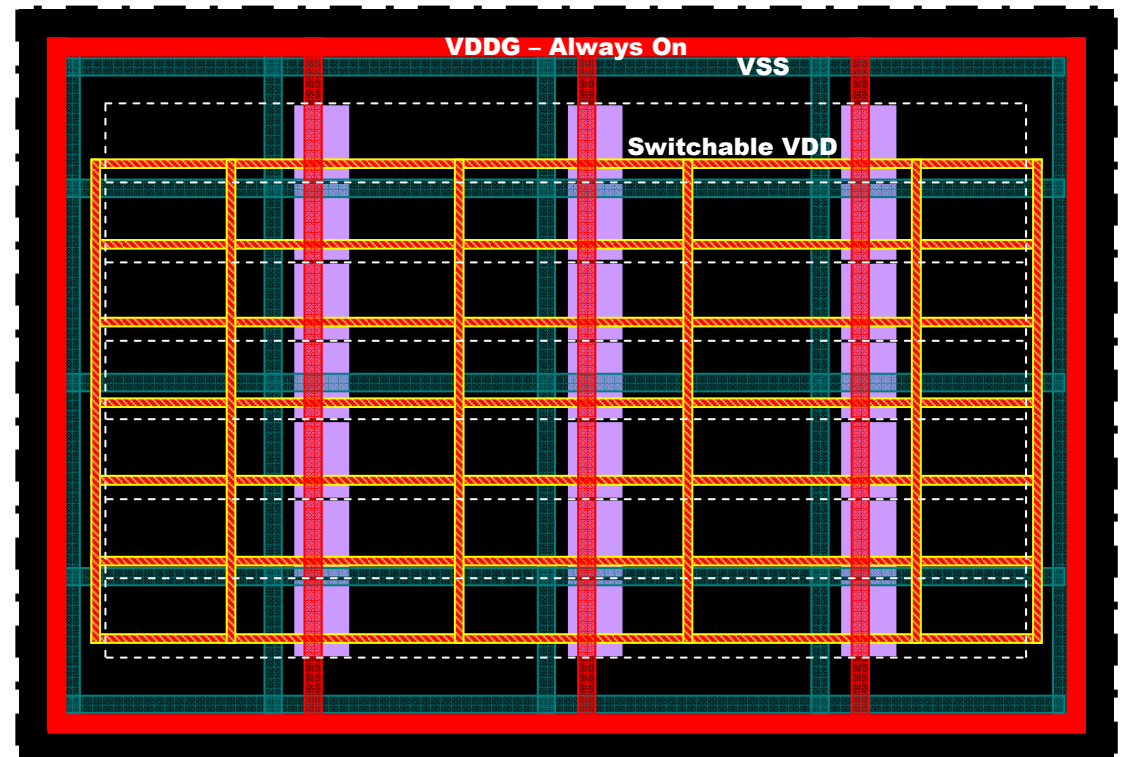


- Architectural integration
 - Components must support a variety of voltage domain and power down options
- Flow integration
 - Simulation views
 - Analysis views (i.e. CCS)
- Design point integration
 - Multiple PVT characterizations

Physical IP Architecture

Expanded cell
set at 45nm

- Power Management Kit (PMK)
 - Level shifters
 - Isolation cells
 - Power gates
 - Retention flops
 - Always-on buffers
 - Back bias cells
- Memory
 - More later
- *Liberty PG Pin*
UPF ready



Low Power Attributes for Liberty - PMK

```
cell (RETENTION_FLOP) {  
  
    area : 1.0;  
    ...  
    pg_pin(VDDG) {  
        voltage_name : VDDG;  
        pg_type : backup_power;  
    }  
    ...  
    pin(RETN) {  
        direction : input;  
        capacitance : 1.0;  
        nextstate_type : data ;  
        related_power_pin :VDDG;  
        related_ground_pin:VSSG;  
    }  
  
    pin(Q) {  
        related_power_pin : VDD ;  
        related_ground_pin : VSS;  
        direction : output;  
    }  
}
```

```
cell (ENABLE_LEVEL_SHIFTER) {  
  
    is_level_shifter : true;  
    pg_pin(P1) {  
        voltage_name : VDD1;  
        pg_type : primary_power;  
        std_cell_main_rail : true;  
    }  
    pg_pin(P2) {  
        voltage_name : VDD2;  
        pg_type : primary_power;  
    }  
    ...  
    pin(A) {  
        direction : input;  
        related_power_pin : P1;  
        related_ground_pin : G1;  
        level_shifter_data_pin:true;  
    }  
    pin(EN) {  
        direction : input;  
        related_power_pin : P1;  
        related_ground_pin : G1;  
        level_shifter_enable_pin:true;  
    }  
    ...  
}
```

```
cell (POWER_GATE) {  
  
    ...  
    switch_cell_type : coarse_grain;  
    pg_pin ( VDDG ) {  
        pg_type :primary_power;  
        direction : input;  
        voltage_name : VDD;  
    }  
    ...  
    pg_pin(VDD) {  
        voltage_name : VDD;  
        pg_type:internal_power;  
        direction : inout;  
    }  
    ...  
    pin ( SLEEP ) {  
        switch_pin : true;  
        capacitance: 0.034;  
    }  
    ...  
}
```



Low Power Attributes for Liberty - PMK

```
cell (RETENTION_FLOP) {  
  
    retention_cell:"ret_dff";  
    area : 1.0;  
    ...  
    pg_pin(VDDG) {  
        voltage_name : VDDG;  
        pg_type : backup_power;  
    }  
    ...  
    pin(RETN) {  
        direction : input;  
        capacitance : 1.0;  
        nextstate_type : data ;  
        related_power_pin :VDDG;  
        related_ground_pin:VSSG;  
        retention_pin  
            (save_restore, "1" );  
    }  
    pin(Q) {  
        power_down_function:"!VDD+VSS";  
        related_power_pin : VDD ;  
        related_ground_pin : VSS;  
        direction : output;  
    }  
}
```

```
cell (ENABLE_LEVEL_SHIFTER) {  
  
    is_level_shifter : true;  
    level_shifter_type : LH ;  
    input_voltage_range(0.7,1.4);  
    output_voltage_range(0.7,1.4);  
    pg_pin(P1) {  
        voltage_name : VDD1;  
        pg_type : primary_power;  
        std_cell_main_rail : true;  
    }  
    pg_pin(P2) {  
        voltage_name : VDD2;  
        pg_type : primary_power;  
    }  
    ...  
    pin(A) {  
        direction : input;  
        related_power_pin : P1;  
        related_ground_pin : G1;  
        level_shifter_data_pin:true;  
    }  
    pin(EN) {  
        direction : input;  
        related_power_pin : P1;  
        related_ground_pin : G1;  
        level_shifter_enable_pin:true;  
    }  
    ...  
}
```

```
cell (POWER_GATE) {  
  
    ...  
    switch_cell_type : coarse_grain;  
    pg_pin ( VDDG ) {  
        pg_type :primary_power;  
        direction : input;  
        voltage_name : VDD;  
    }  
    ...  
    pg_pin(VDD) {  
        voltage_name : VDD;  
        pg_type:internal_power;  
        direction : inout;  
        switch_function : "SLEEP";  
        pg_function : "VDDG";  
    }  
    ...  
    pin ( SLEEP ) {  
        switch_pin : true;  
        capacitance: 0.034;  
    }  
    ...  
}
```



2007.03
Attributes
(with 2006.06)

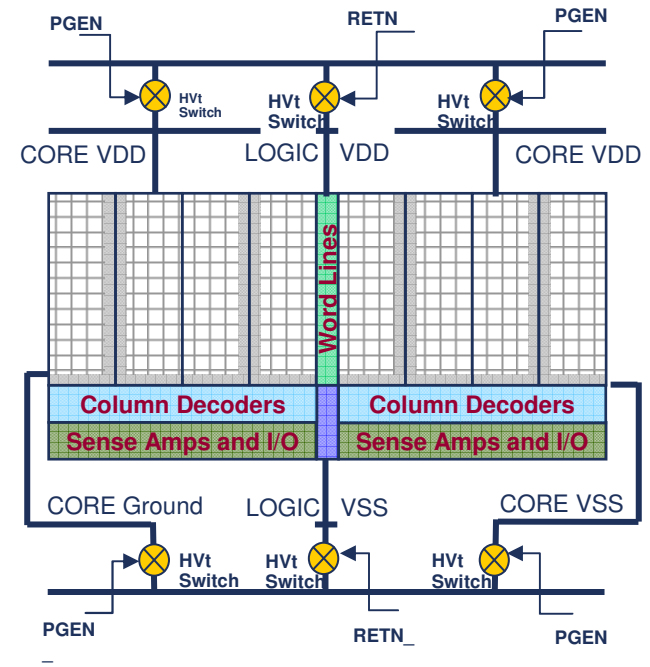
Low Power Attributes for Liberty – Other IP

■ Memories

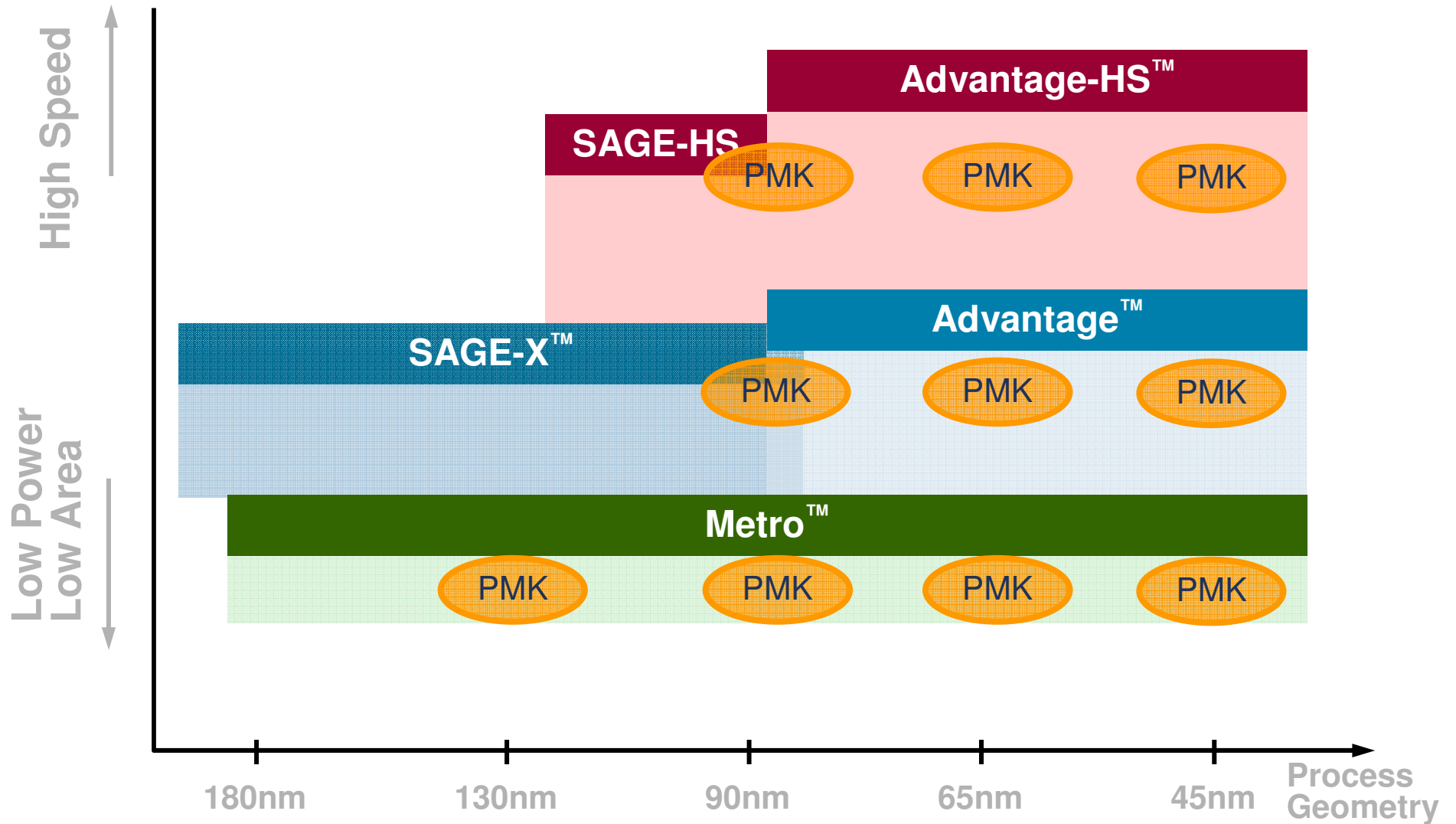
- Include P/G pins
- Multiple power modes
 - Standby mode
 - Retention mode
 - Shutdown mode
- Built-in power gates (compile-time option)
- Working to define / implement Liberty attributes

■ I/Os

- Include P/G pins
- Built-in retention
- Working to define / implement Liberty attributes



Power Management Kit & ARM Standard Cells



What We See as Issues...

- Well connections
 - Liberty now supports power/ground pins, not well pins
 - Well pins ARE in LVS netlist
 - Well pins not necessarily in gate-level netlist from P&R
 - Watch for shorting wells together: can short always-on supply to stackable supply via wells
- IR drop in gates/timing
 - Consider IR drop across power gates early in design to avoid issues in timing closure
- Simulation modelling for memory
 - Modelling complex LP behaviors in consistent fashion
- Dynamic situation
 - 2007.12 and beyond
 - CCS power
 - Expanded cell set in PMK
 - Enhanced modeling in memories, I/Os



Forward Looking...

- Continue to collaborate with EDA companies
 - Regular technical meetings
 - Increase automation for low power flows with enhanced views/modeling
- Release libraries with updated Liberty syntax
- Expand cell sets for low power
- Continue to participate in standards bodies
- Continue technology demonstrators such as SALT

