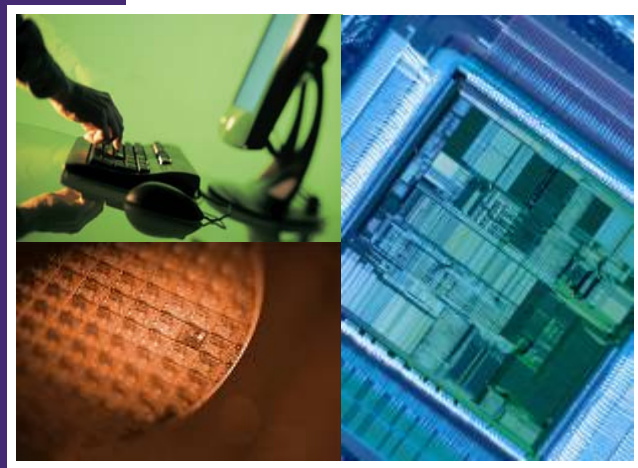
Liberty Low Power/UPF



Tom Chau
Synopsys Inc.

10/24/2007

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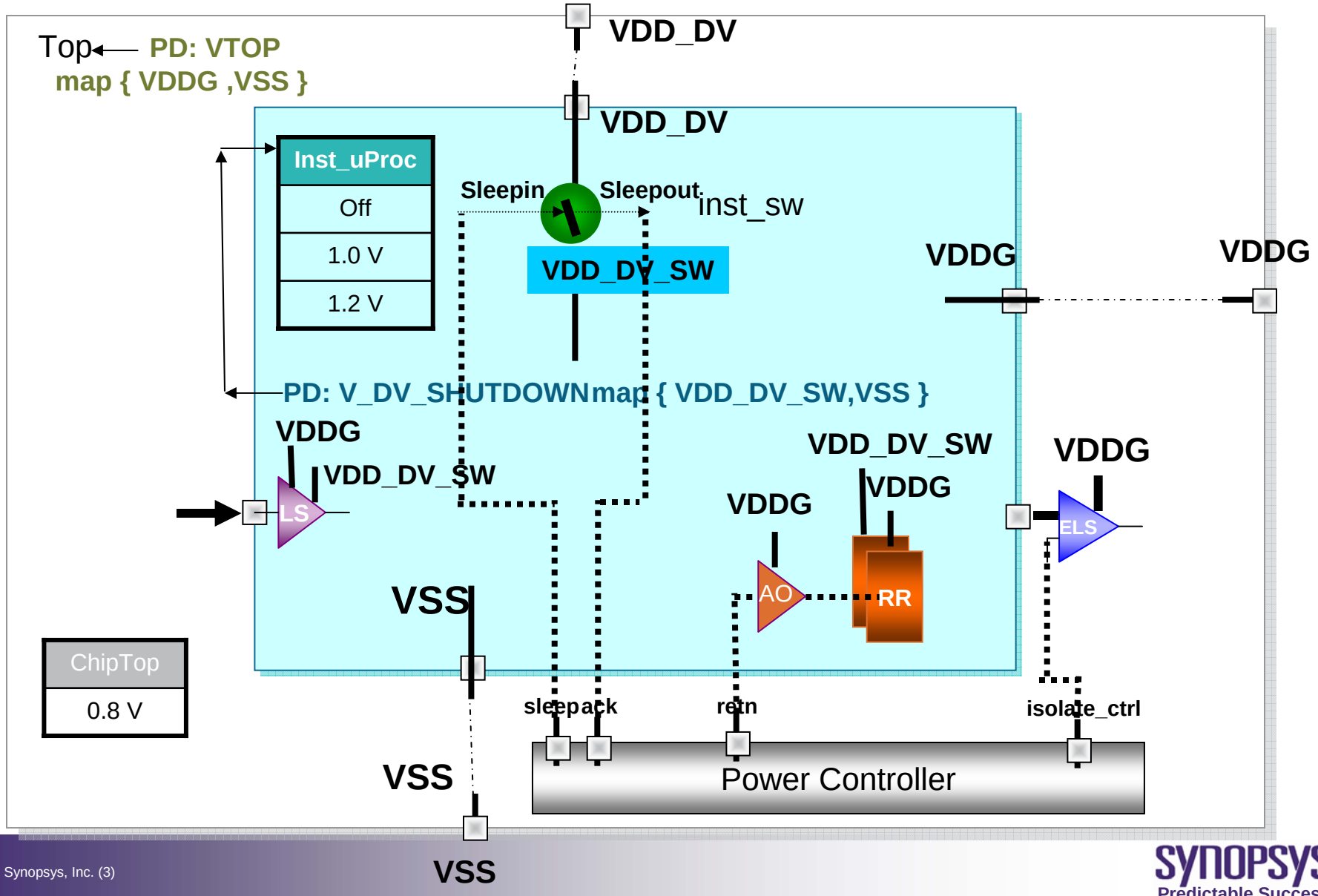
Agenda

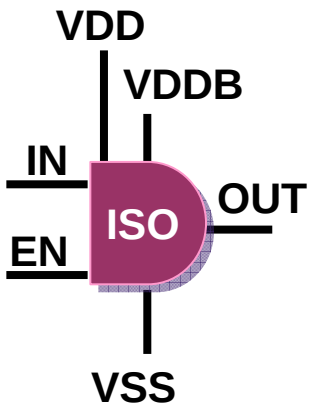
- Liberty Low Power Update
  - Overview
  - PG Pin Syntax
  - Power Management Cell Syntax
- Summary

Low Power Design

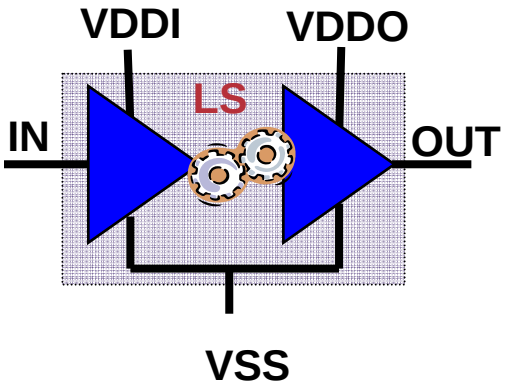


Low Power Infrastructure

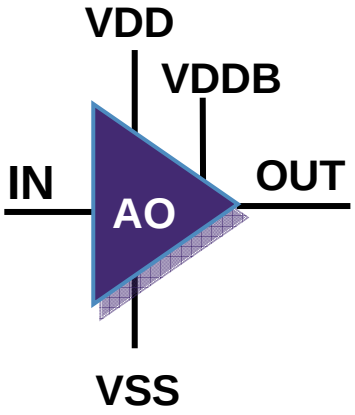
Power Management Cells



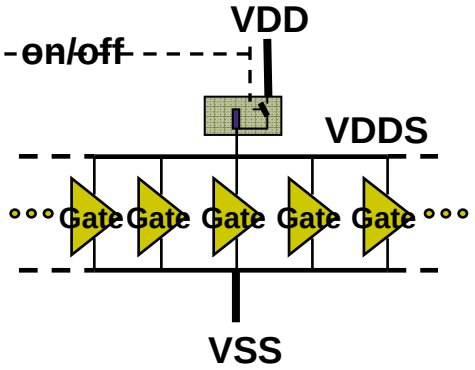
Isolation



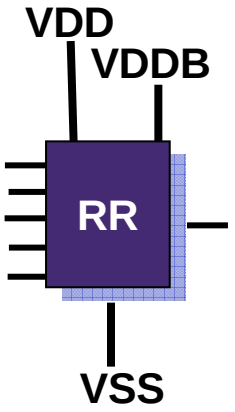
Level Shifter



Always-On



Power Gate



Retention Register

- Low Power designs require new cells with multiple power pins
- Additional modeling information in Liberty is required to automatically handle these cells

Low-Power Infrastructure

PG Pin Syntax

```
library(sample) {
voltage_map(VDD1, 3.0);
voltage_map(VDD2, 3.1);
voltage_map(GND1, 0.3);
voltage_map(GND2, 0.0);
…
cell(test) {
pg_pin(P1) {
voltage_name : VDD1;
pg_type : primary_power;
}
…
pg_pin(G2) {
voltage_name : GND2;
pg_type : primary_ground;
}
…

pin(A) {
direction : input;
related_power_pin : P2;
related_ground_pin : G2;
…
}
pin(Z) {
direction : output;
related_power_pin : P1;
related_ground_pin : G1;
…
```

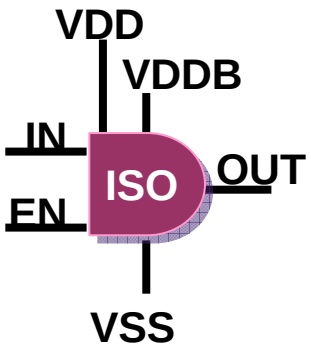
- Needed: PG pin definitions are required for all cells in the library
  - Used to define multiple power ground pin information accurately
- Benefits
  - Power domain driven synthesis
  - Automatic power nets connections
  - PST based optimization
  - PG netlist vs power domain verification
  - Power switch verification
  - CCS-power library accuracy

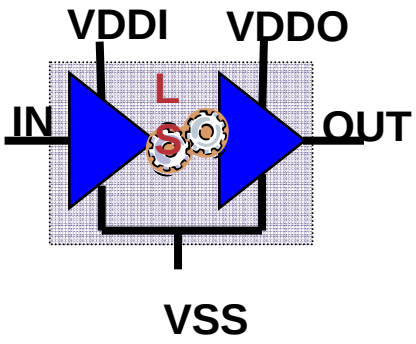
Low-Power Infrastructure

Isolation/Level Shifters

```
cell(Enable_Level_Shifter) {
  is_level_shifter : true;
  level_shifter_type : HL ;
  input_voltage_range(0.7,1.4);
  output_voltage_range(0.7,1.4);

pg_pin(P1) {
  voltage_name : VDD1;
  pg_type : primary_power;
  std_cell_main_rail : true;
}
pg_pin(P2) {
  voltage_name : VDD2;
  pg_type : primary_power;
}
...
pin(A) {
  direction : input;
  related_power_pin : P1;
  related_ground_pin : G1;
  level_shifter_data_pin:true;
}
pin(EN) {
  direction : input;
  related_power_pin : P1;
  related_ground_pin : G1;
  level_shifter_enable_pin:true;
} ...
```



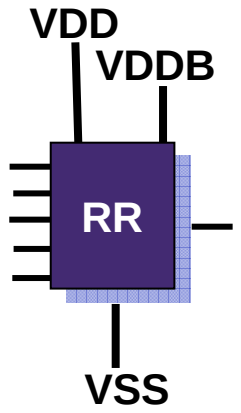


- For all necessary voltage ranges, both L->H and H->L
- Main rails for either input and output power pins to allow placement in source or sink domain
- Always-on level shifters for always-on paths
- Isolation cells to support both high and low clamp and high/low enable signal

Low-Power Infrastructure
Retention Registers

```
cell (RETENTION_DFF) {
retention_cell:“ret_dff";
  area : 1.0;
  ...
 pg_pin(VDDG) {
   voltage_name : VDDG;
   pg_type : backup_power;
 }
 ...
 pin(RETN) {
   direction : input;
   capacitance : 1.0;
   nextstate_type : data ;
   related_power_pin :VDDG;
   related_ground_pin:VSSG;
   retention_pin
        (save_restore, “1” );
    }

 pin(Q) {
power_down_function:"!VDD+VSS";
related_power_pin : VDD ;
related_ground_pin : VSS;
direction : output;
```

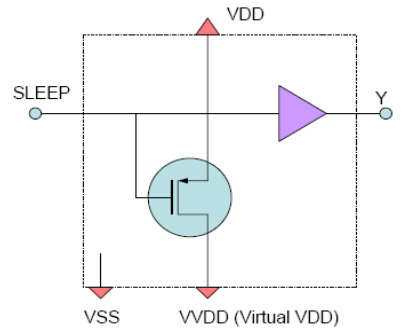


- Populate retention register as other FFs and latches
  - Necessary register configuration options (Preset/Clear, scan, test, etc.)
  - posedge and negedge clock type
  - Latch or edge-triggered
  - Q output may be always-on
  - Both clock dependent and clock independent configurations
- Supports single-pin and two-pin Save/Restore protocols

Low-Power Infrastructure

Power Switches

```
cell ( Simple_CG_Switch ) {
  ...
  switch_cell_type:
                  coarse_grain;
  pg_pin ( VDD ) {
  pg_type :primary_power;
  direction : input;
  voltage_name : VDD;
  }
 ...
  pg_pin( VVDD ) {
  voltage_name : VVDD;
  pg_type : internal_power;
  direction : output;
  switch_function : "SLEEP";
  pg_function : "VDD";
  }
 ...
  pin ( SLEEP ) {
  direction : input
  switch_pin : true;
  capacitance: 0.034;
  }
 ...
 pin (Y) {
 direction : output;
 function : "SLEEP";
 power_down_function : "!VDD + VSS";
...
    }
```



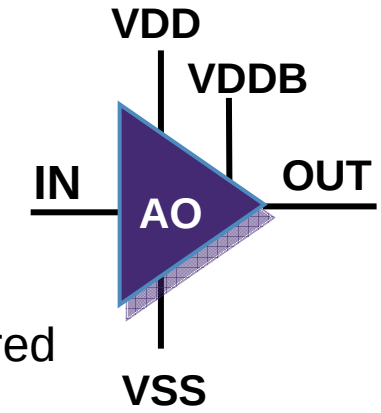
- Logic condition under which the cell turns off
  - Switching function based on signal pins
  - A power-down function based on power pins
- Optional acknowledge output pins which are output pins whose signal is used to propagate the switch signal
- Multiple input signal pins and multiple acknowledge output pins are optional
- Steady state current (I/V) information
  - Determine the resistance value when the switch is on

Low-Power Infrastructure

Always-On Logic

```
cell (buffer_type_AO)  {
  always_on : true ;
...
pg_pin (VDDBAK) {
  voltage_name : VDDBAK;
  pg_type : backup_power; }
pg_pin (VSSBAK) {
  voltage_name : VSSBAK;
  pg_type : backup_ground; }
...
```

```
cell (macro_cell_with_AO_pins)
{
...
pin (A) {
  always_on : true ;
  related_power_pin : VDDBAK ;
  related_ground_pin : VSSBAK
;
...  }
```



- Always-On cell attribute required
  - Buffer and inverter
- Always-On pin attribute required
  - Macro cell
- AO-pins are automatically derived for:
  - Save/restore pins on retention cells
  - Control pins on switch cells
  - Enable pins on isolation cells and Enable Level Shifter

Summary

- Enhanced Liberty PG pin and Power Management cells modelling syntax enable Low Power capabilities
- Update your libraries and tools to take advantage of enhanced Liberty syntax for UPF-based flow
- For more information, see specifications under
  - http://www.synopsys.com/cgi-bin/tapin/login1.cgi

Predictable Success