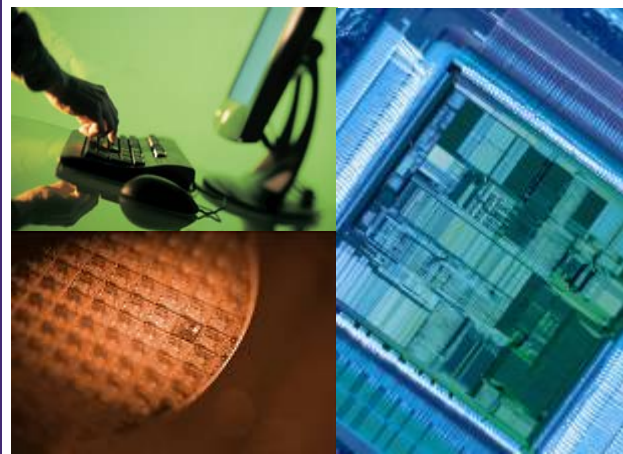


Welcome to the 19th EDA Interoperability Developers' Forum

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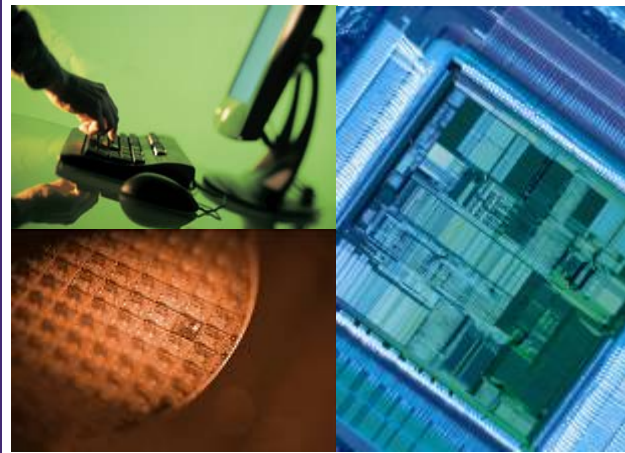


April 26, 2007



SYNOPSYS[®]
Predictable Success

Welcome to the 19th EDA Interoperability Developers' Forum



Rich Goldman
Vice President
Strategic Market Development

SYNOPSYS[®]
Predictable Success

What you've come to expect...

- Interesting keynote presentation
 - *“Making Multicore Work and Measuring its Benefits”*
 - Markus Levy, EEMBC and the Multicore Association
- Industry initiatives and standards
 - Accellera's UPF (Unified Power Format)
 - Tutorial: UPF for EDA
 - Panel discussion: Scaling the Power Wall
 - Liberty Advancements
 - EDAC Anti-Piracy Techniques
 - Open Standards for Custom Analog
 - Open Constraints for Analog Presentations
 - Panel Discussion: IPL Now!
- Plus prizes!

Stay informed. Get involved. Participate in the Process.

- Accellera www.accelera.org
- EDA Consortium www.edac.org
- EEMBC www.eembc.com
- IEEE www.ieee.org
- The Multicore Association www.multicore-association.org
- Si2 www.si2.org
- SPIRIT Consortium www.spiritconsortium.org
- VSIA www.vsia.org
- And more!...



Introducing www.IPLnow.com



- IPL Charter
 - An industry collaboration to promote interoperable PCell libraries (IPLs) on the OpenAccess database
- IPL Benefits
 - Reduce PCell development and support costs
 - Enable foundries and semiconductor companies to support many EDA tools with a single IPL
 - Increase layout tool interoperability
- Founding members include AWR, Ciranova, Silicon Canvas, Silicon Navigator and Synopsys
- Download proof of concept library now at www.IPLnow.com
- Join IPL now! – Accepting new members at www.IPLnow.com

Stay Tuned for the Analog Sessions in the Afternoon

- Technical Presentations on Open Constraints for Analog IC Design *(3:05pm – 4:05pm)*
 - Presenters from Ciranova, Pulsic and Silicon Canvas
- Panel Discussion: IPL Now! *(4:05pm – 5:05pm)*
 - Moderated by Michael Santarini, Senior Editor, EDN
 - Panelists from AWR, Ciranova, Mentor Graphics, National Semiconductor, Silicon Canvas, Silicon Navigator and Synopsys



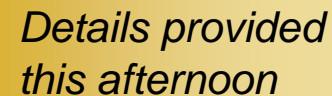
Download Current Versions

- Synopsys Open Source Formats:

www.synopsys.com/partners/tapin

- Liberty 2007.03 **New!**
 - Liberty Parser 2.4 **New!**
- SAIF 2.0
- SDC 1.7 **New!**
- vSDC 2005.12

- OpenVera: www.open-vera.com
 - 1.4.2 Testbench LRM
 - 1.4.1 Assertions LRM



*Details provided
this afternoon*

More on SDC Version 1.7 *New!*

- Supported by Design Compiler 2007.03, PrimeTime 2007.06
- Incorporates:
 - 8 new commands
 - set_units
 - all_registers
 - group_path
 - set_clock_groups
 - set_clock_sense
 - set_ideal_latency
 - set_ideal_network
 - set_ideal_transition
 - 7 new options/arguments of previously supported commands

SDC Parser Version 1.7 *New!*

- Download version 1.7 of SDC Parser and Application Note at:

www.synopsys.com/tapin

- For SDC support contact:
 - sdcsupport@synopsys.com
- For TAP-in Program general information contact:
 - tapin@synopsys.com

Download Current Versions

- Milkyway Access Program (MAP-in):
 - Milkyway Database Environment and C-API Y-2006.06
 - Next version Z-2007.03 – available in June
- Open SystemC Initiative:
 - IEEE 1666™-2005 standard approved in December 2005
 - IEEE 1666-2005 LRM available at no charge
 - SystemC 2.2 open source library released April 2007 *New!*

www.synopsys.com/partners/mapin

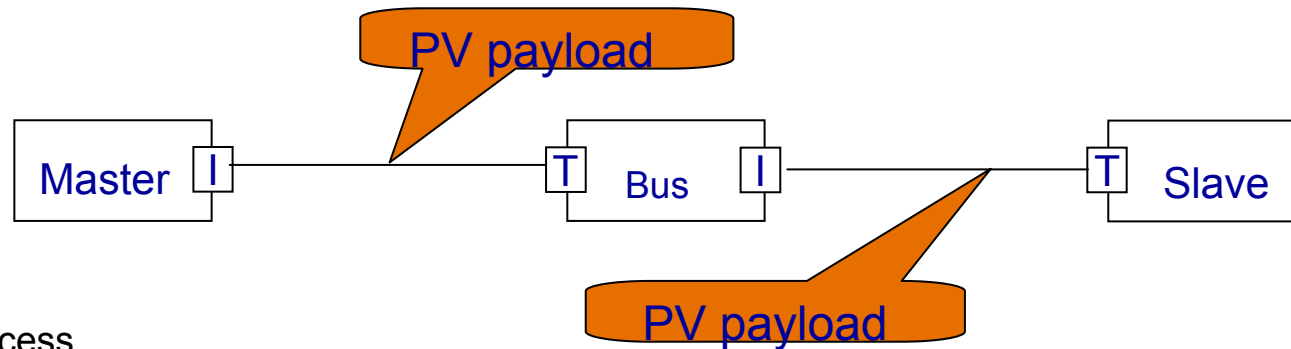
www.SystemC.org

standards.ieee.org/getieee/1666

OSCI TLM 2.0 Activities

- Charter

- Specify interfaces at the Transaction Level, enabling model interoperability for untimed and timed TLM models.
- Mechanism for analysis of transactions
- Application domains: Virtual Platforms, architectural exploration, verification reference models



- The process

- Dec 2006: draft ready
- Dec 2006 – Feb 2007: review period
 - Synopsys took very active role in review, given the experience collected with more than 40 commercially deployed Virtual Platforms. As expected
 - Several good concepts
 - Dedicated areas for improvement
- => Jan 18th, 2007: Synopsys provided enhancement proposal (see next slide)**
- Feb 2007: Trevor Wiemann of Intel becomes new working group (WG) chair
- Feb 2007 – today: WG re-energized, established requirement based process weekly meetings, strong Synopsys involvement



Synopsys' Contribution to TLM WG on January 18, 2007

Process proposal

- Requirement driven
- Based on measurable criteria

Technology proposal:

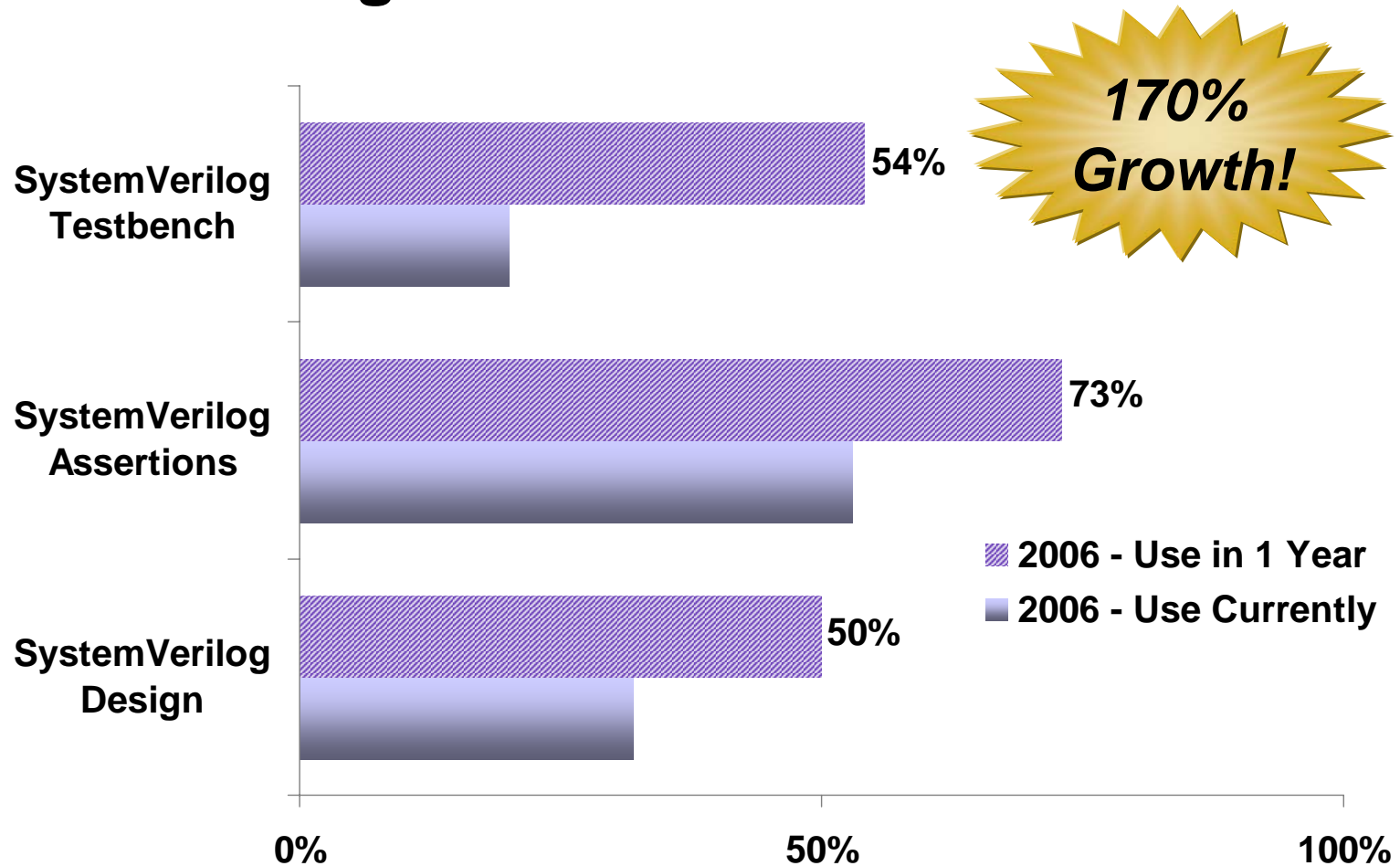
- High-performance modeling style, close to current TLM 2.0 draft
- Proven TLM technology (40+ complete virtual platforms)
- Interfaces for
 - Transport
 - Single interface for PV and PVT
 - Runtime PV → PVT switch
 - More flexible timing annotation
 - Debugging
 - Configuration
 - Direct memory access
 - Master scheduling

Working proof-of-concept implementation of API classes and modeling examples:

- Allows for value analysis based on measurable criteria



SystemVerilog Language Adoption to go Mainstream in 2007



Source: 2006 Worldwide SNUG Surveys



Download Current Versions

- IEEE Std 1800 for SystemVerilog ratified in November 2005
- Download specification at www.ieee.org
- Find products, solutions, technical papers & more at Accellera's www.systemverilog.org
- Learn more at
 - VMM (*Verification Methodology Manual*): www.vmm-sv.org
 - Synopsys SystemVerilog: www.synopsys.com/systemverilog

The image shows two overlapping browser windows. The top window displays the Synopsys SystemVerilog website, featuring the company logo and navigation links for Testimonials, News, Resources, and Books. The bottom window shows the 'Verification Methodology Manual for SystemVerilog' page, which includes a book cover image, a 'What's Hot' section with a list of recent news items, and a quote from Yoshiharu Furuji, senior manager at STARC, endorsing the manual. The STARC logo is also visible. At the bottom of the page, there is a section titled 'Verification Methodology Manual for SystemVerilog' with a brief description of the manual's content.

7th Annual Tenzing Norgay Interoperability Achievement Award

- Presented to a company that
 - Surpasses common levels of interoperability
 - Contributes to overall industry advancement
 - Provides a new view of the future
 - Ensures customer success



*Tenzing Norgay
on Mt. Everest*



Tenzing Norgay Award



• Previous Recipients:

- Electronic Tools Company (2006)
- ARM (2005)
- Novas (2004)
- Silicon Metrics (2003)
- Mentor Graphics (2002)
- CoWare (2001)

• 2007 Nominees

- Ciranova
- Engineering DataXpress
- Library Technology
- Magma Design Automation
- Silicon Navigator
- Verific Design Automation
- Zenasis

And the winner is...

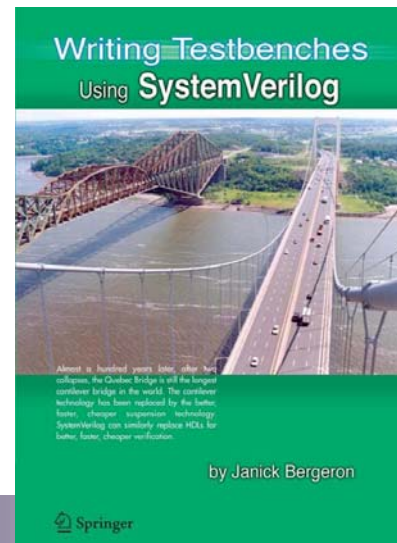
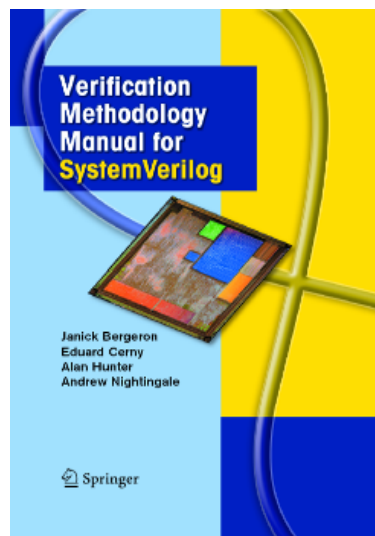


**...to be announced at the Synopsys
Interoperability Breakfast Event at DAC**

Wednesday, June 6, 2007

Presentations & Prizes...

- Presentations will be available for download from the web starting today:
www.synopsys.com/devforum/apr2007/presentations
- Keep your raffle ticket to be eligible* for more prizes:
 - *Verification Methodology Manual for SystemVerilog* by Janick Bergeron, Eduard Cerny, Alan Hunter and Andrew Nightingale
 - *Writing Testbenches Using SystemVerilog* by Janick Bergeron
 - AMC Theatres' Gift Packages
 - 2 Gold Movie Tickets (no restrictions), 2 small drinks & 1 small popcorn
- Complete the feedback forms to enter drawings* for iPod® shuffles



*Must be present to win



Mark Your Calendar!

20th EDA Interoperability Developers' Forum

- October 2007
- Located in Silicon Valley
- Invite your colleagues
- Want to speak? Let us know.

See you then!

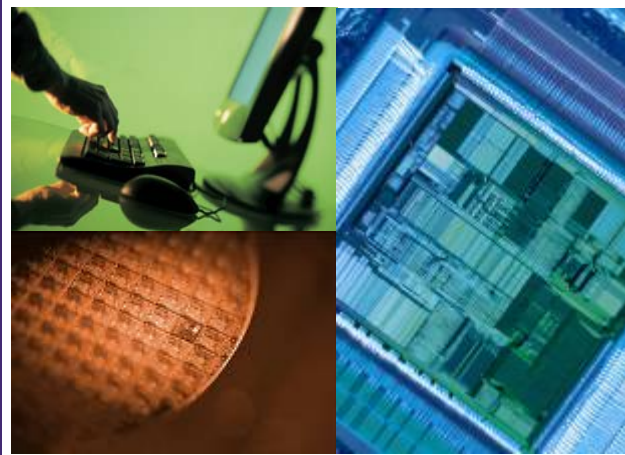
Today's Agenda

- Power of One (9:45AM – 11:45AM)
 - Tutorial: UPF for EDA
 - Panel Discussion: Scaling the Power Wall
- Lunch
- General Session (12:20PM – 2:50PM)
 - EDAC: Software Piracy – Overview of Anti-Tampering Technologies
 - Keynote Presentation by Markus Levy, EEMBC & the Multicore Association
 - *“Making Multicore Work and Measuring its Benefits”*
 - What's New with Liberty 2007
- Open Analog Standards (3:05PM – 5:05PM)
 - Technical Presentations on Open Constraints for Analog
 - Panel Discussion: IPL Now!

Enjoy your 19th EDA Interoperability Developers' Forum

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