



ATRENTA®

SYNOPSYS®



Unifying Low Power Design with UPF

The Power of One



UPF – A Cooperative Effort Under Accellera



Agenda



- Introduction (00:15)
 - Kevin Kranen, Synopsys
- UPF Low Power Design Basics (00:30)
 - Stephen Bailey, Mentor Graphics
- Low Power Design Implementation (00:30)
 - Arvind Narayanan, Magma Design
- Comprehensive MV Verification (00:15)
 - Anand Iyer, ArchPro
- Q & A

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UPF is the New Industry Standard



Built from Silicon-proven Technologies

Technology donations to UPF TSC

- **Mentor**
 - External power configuration file for verification
- **Magma**
 - Power Management commands
- **Vast**
 - System level modeling methodology and format
- **Synopsys**
 - RTL constructs (Verilog and VHDL)
 - Power Management commands
 - Switching activity format – SAIF
- **TI**
 - Retention cell semantics
- **Atrenta, Synchronous DA**

- Feb 07 - UPF 1.0 standard approved by Accellera !
- March 07 – IEEE P1801 PAR / Study Group underway

UPF Participating Companies

- **AMD**
- **ArchPro**
- **ARM**
- **Atrenta**
- **Azuro**
- **Cadence**
- **ChipVision**
- **FreeScale**
- **IBM**
- **Infineon**
- **Intel**
- **LCDM Eng**
- **LSI Logic**
- **Magma**
- **Mentor**
- **Nokia**
- **Nordic Semi**
- **Novas**
- **NXP**
- **Qualcomm**
- **Si2**
- **STARC**
- **STM**
- **Synchronous DA**
- **Synopsys**
- **TI**
- **Toshiba**
- **VaST**
- **Virage Logic**
- **Xilinx**

UPF 1.0 Industry Endorsement & Support



- **Infineon** - The quick development and release of the UPF 1.0 standard is based on our close partnership relations with EDA suppliers who share the same vision and attitude in making things happen. We are convinced that UPF will support us in achieving zero-defect quality and our productivity objectives, which both are key for Infineon's World class Automotive Product Portfolio.

Hartmut Hiller, Senior Director Design Methodology Automotive, Industrial & Multimarket

- **Synopsys** - Applauds Accellera for approving the UPF standard for low power design and verification. We plan to deliver our UPF 1.0-based implementation and verification solution during 2007. In response to customer demand for a standard that enables consistent and interoperable end-user low power flows and methodologies, Synopsys - together with Magma Design Automation, Mentor Graphics, leading end-customers and IP companies - has made strong contributions to UPF 1.0 based on our proven technologies. UPF 1.0 is ready for industry use.

Rich Goldman, Vice President, Synopsys, Strategic Market Development

UPF 1.0 Industry Endorsement & Support



- **Magma** - The speed at which the UPF standard has been developed and approved demonstrates the power of one open, inclusive and cooperative industry-wide effort. Users will realize significant improvements in productivity and quality of results by having a single, portable file and format with which they can specify, modify and maintain design data. Accellera, Magma, Mentor, Synopsys and all the companies that donated technology and expertise should be commended.

Kam Kittrell, General Manager, Design Implementation Business Unit, Magma Design Automation

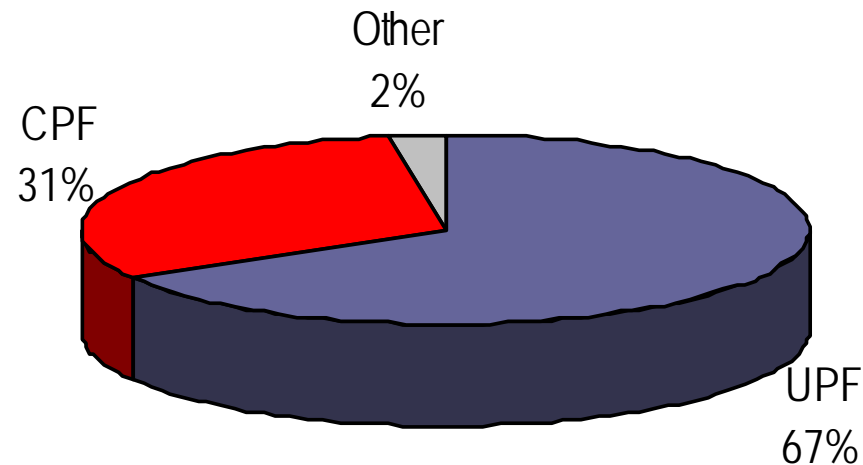
- **Mentor** - Designers want a single format that is simple to use, extensible, and capable of describing complex power behavior. The Unified Power Format (UPF) 1.0 standard achieves this by being open and comprehensive enabling support from leading EDA vendors and customers for industry-wide adoption. Mentor is committed to Accellera's UPF 1.0 standard as we are a leading contributor of our proven technology to this open standard for low power design and verification

Robert Hum, Vice President & General Manager, Mentor Graphics Design Verification & Test Division

Digital Design



COT/ASIC/FPGA Synthesis + Physical Implementation + DFT + Signoff
(TTM Revenue: \$1,042.0M)

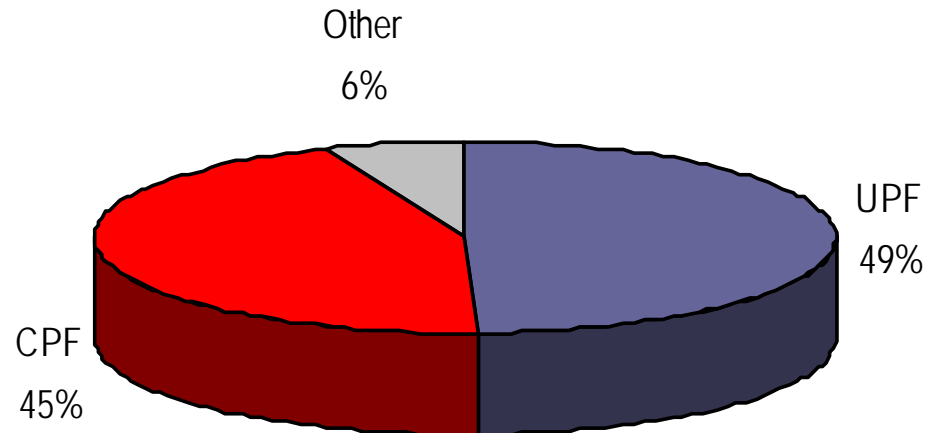


Based on Q4 05 through Q3 06 EDAC MSS data plus other publicly available market data

Digital Verification

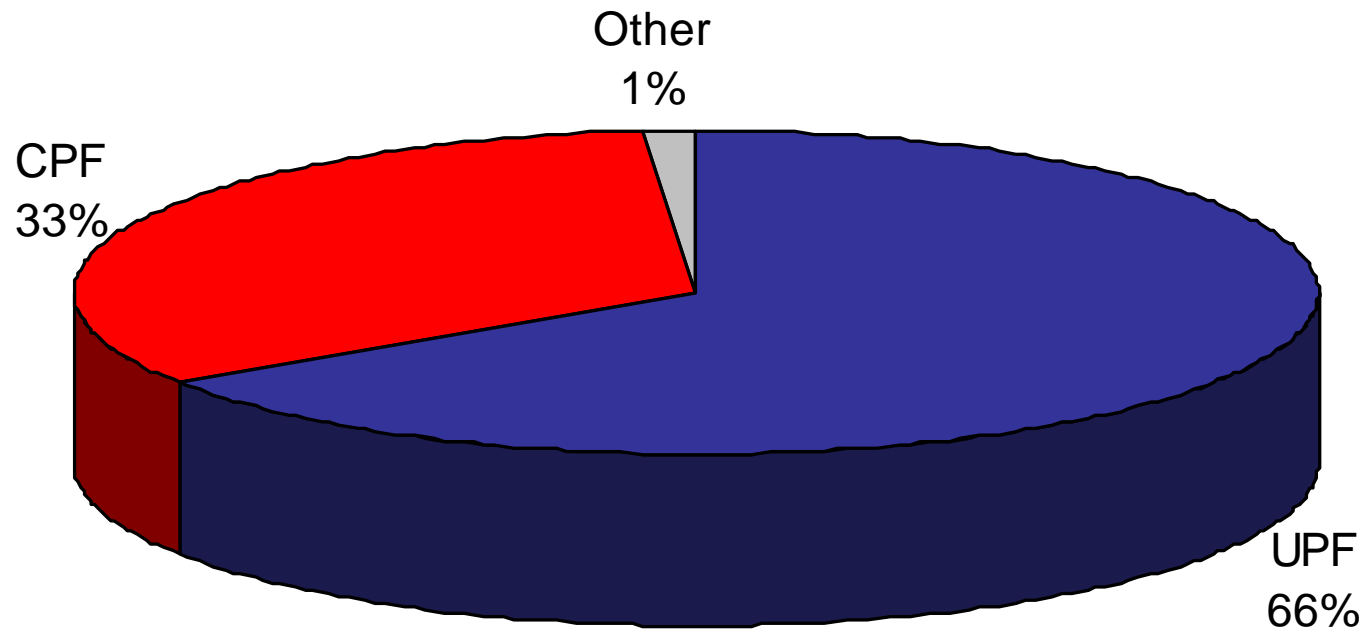


RTL Verification + Formal Verification
(TTM Revenue: \$579.8M)



Based on Q4 05 through Q3 06 EDAC MSS data plus other publicly available market data

Digital Verification ☺



Based on 2007 John Cooley DeepChip Verification Survey “Mindshare” – 818 Respondents

What is UPF?

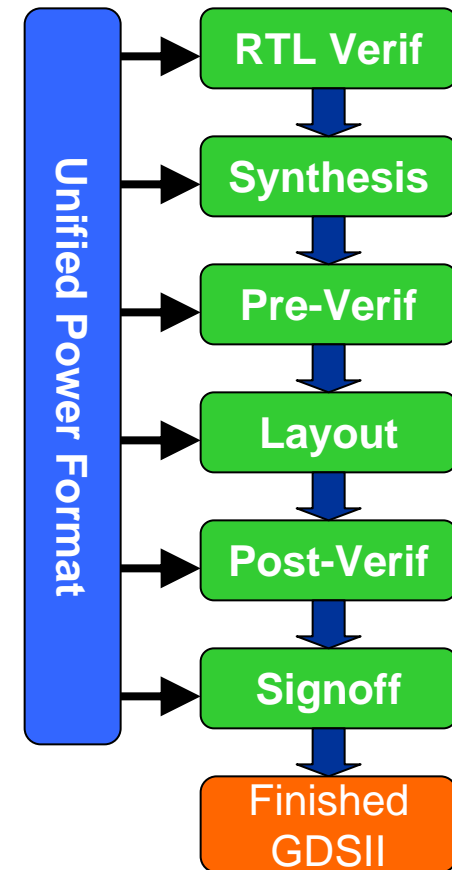


- Unified Power Format
- UPF provides the ability for electronic systems to be designed with power as a key consideration early in the process.
- Why UPF?
 - No existing HDL adequately supports the specification of power distribution and management
 - Vendor-specific formats are non-portable and create opportunities for bugs via inconsistent specifications

Consistent Commands to:



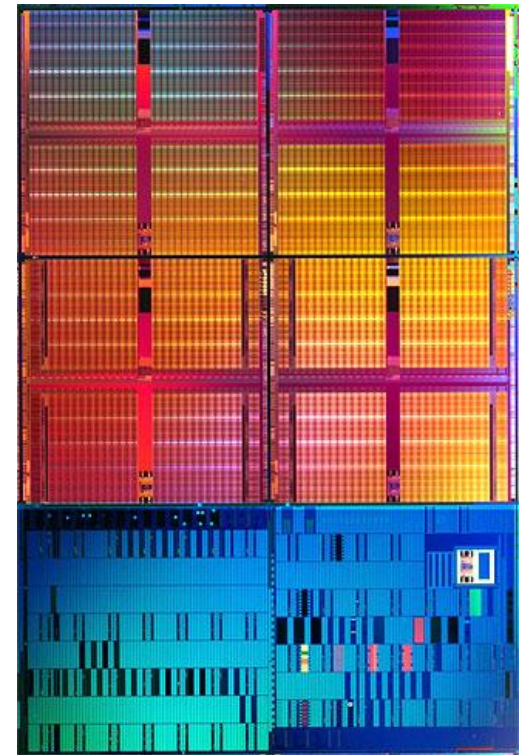
- **Define power distribution architecture**
 - Power domains
 - Supply rails
 - Switches
- **Create power strategy**
 - Power state tables
- **Set up and map**
 - Retention
 - Isolation
 - Level shifters
 - Switches



Why has Power Become THE Dominant Constraint?

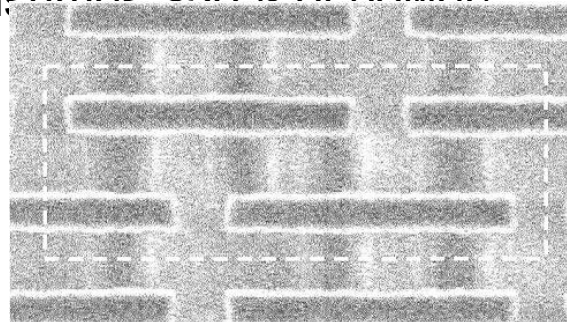


- Low power is key for many (most) applications
 - Mobile, processing, communications, consumer
- Driver: Process technology
 - >100nm:
 - Switching dominates power consumption
 - <100nm
 - Static leakage consumes >50% of power!



Intel 45nm Test Chip

Intel 45nm Memory Cell



Fast Response to Industry Need



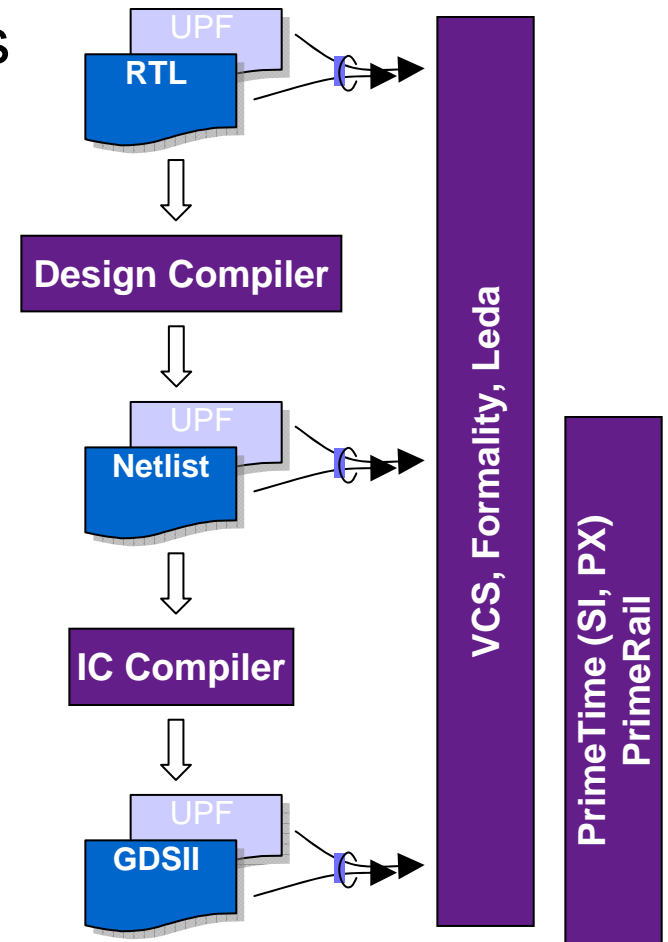
Date	Milestone
11 Sep 06	Accellera TSC formation
18 Sep 06	Design Objectives Document; Weekly meetings start
5 Oct 06	Si2 / Accellera Workshop on Low Power
30 Oct 06	First drafts available for review
30 Nov 06	Submission to Accellera Board for Approval
23 Jan 07	Accellera Technical committee approves standard
22 Feb 07	Accellera Board approves UPF – V1.0 released
23 Feb 07	IEEE study group formed
7 May 07	(expected) Establish IEEE P1801 Working Group to develop a proposed standard for Low Power

Public Download <http://www.accellera.org>

Synopsys UPF Support



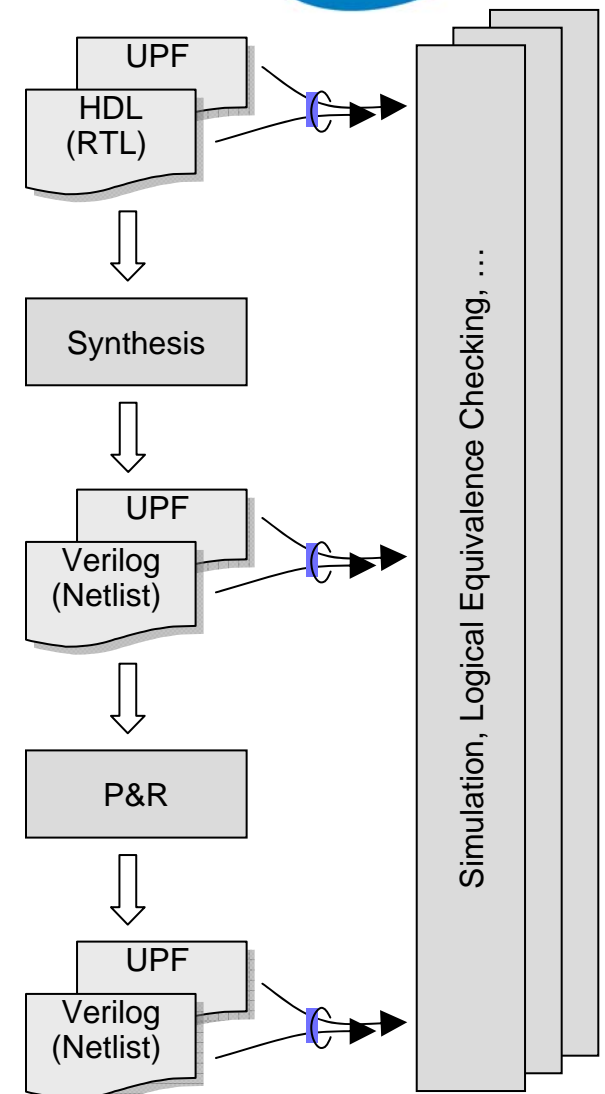
- Based on existing, proven capabilities
 - 2 years prior experience
 - Over 20 Multi-voltage tapeouts
 - Numerous power-gating tapeouts
- Broad Product Support in 2007
 - Verification
 - Synthesis
 - Physical Implementation
 - Checking
 - Signoff
 - Low Power IP



UPF in a Nutshell



- What is UPF?
 - Abstract supply distribution and control network specification
 - Power-aware design intent
 - Used throughout design flow
- Key Concept:
UPF extends without changing the logic design specification
 - Golden source is not touched
 - No re-verification of logic-only
 - UPF augments the HDL specification
- Key Concept:
Matching simulation & implementation semantics



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UPF Value Points



- **TCL**
 - Exploit all TCL scripting capabilities
- **IP Accommodating**
 - Specify how separate from what
 - Which registers require retention
 - Specifics of retention (supplies, control signals)
- **Default, general application**
 - Retention and isolation strategies
 - Recursive inclusion, etc
 - With well-defined precedence semantics
 - More specific has higher precedence
- **Legacy methodology friendly**
 - Set_power_switch
 - User-defined supply net state conversions
- **Semantic integration with logic design**

UPF / Logic Design Relationship



- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy



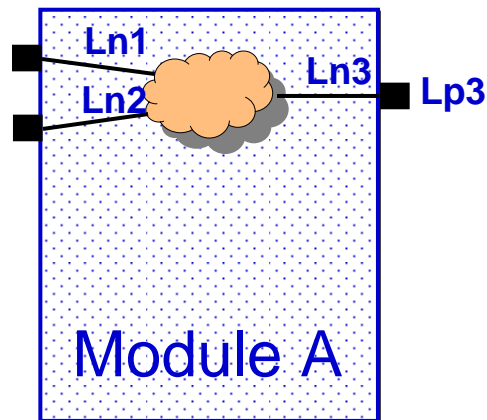
UPF / Logic Design Relationship



- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy

```
create_power_domain pdA  
-include_scope A
```



Logic Design

pdA

create_power_domain



```
create_power_domain domain_name  
  [ -elements list ]  
  [ -include_scope ]  
  [ -scope instance_name ]
```

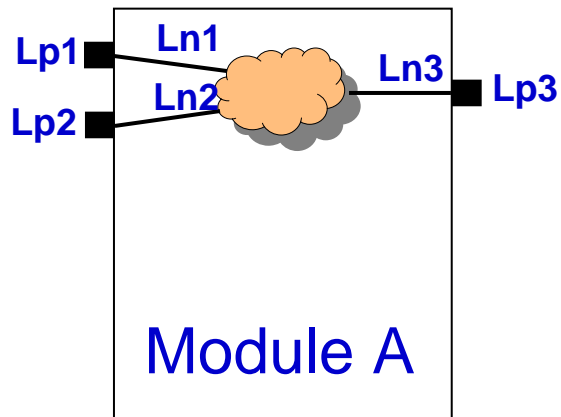
UPF / Logic Design Relationship



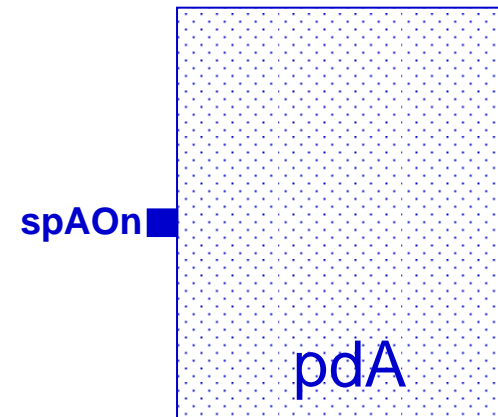
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```
create_supply_port spAOn  
-domain pdA
```



Logic Design



create_supply_port



```
create_supply_port port_name  
  -domain domain_name  
  [-direction <in | out>]
```

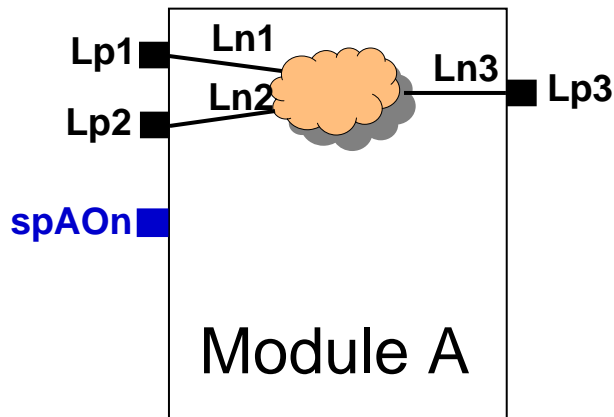
UPF / Logic Design Relationship



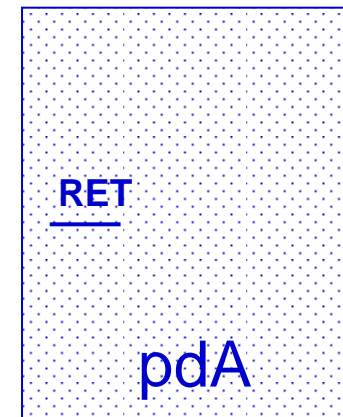
- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy

```
create_supply_net RET  
-domain pdA
```



Logic Design



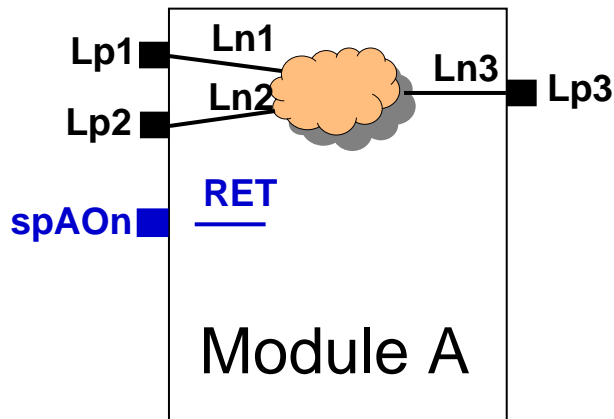
UPF / Logic Design Relationship



- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy

```
create_supply_net PR  
-domain pdA
```



Logic Design



create_supply_net



```
create_supply_net net_name
  -domain domain_name
  [ -reuse ]
  [ -resolve < unresolved
    | one_hot
    | parallel > ]
```

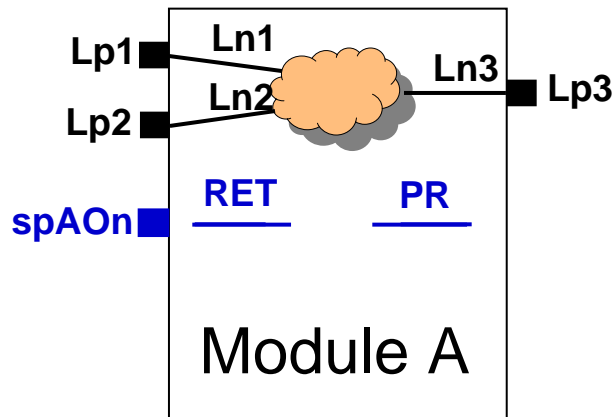
UPF / Logic Design Relationship



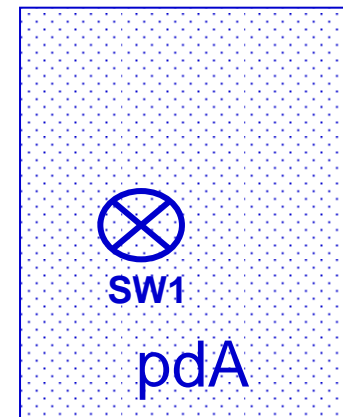
- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy

```
create_power_switch SW1 -domain pdA  
-input_supply_port {inp RET}  
-output_supply_port {outp PR}
```



Logic Design



create_power_switch



```
create_power_switch switch_name
  -domain domain_name
  -output_supply_port { port_name supply_net_name }
  {-input_supply_port { port_name supply_net_name }}*
  {-control_port { port_name net_name }}*
  {-on_state {state_name input_supply_port
    {boolean_function}}}*
  [-on_partial_state { state_name input_supply_port {
    boolean_function }}]*
  [-ack_port { port_name net_name [{boolean_function}] }]*
  [-ack_delay { port_name delay}]*
  [-off_state { state_name {boolean_function} }]*
  [-error_state { state_name {boolean_function} }]*
```

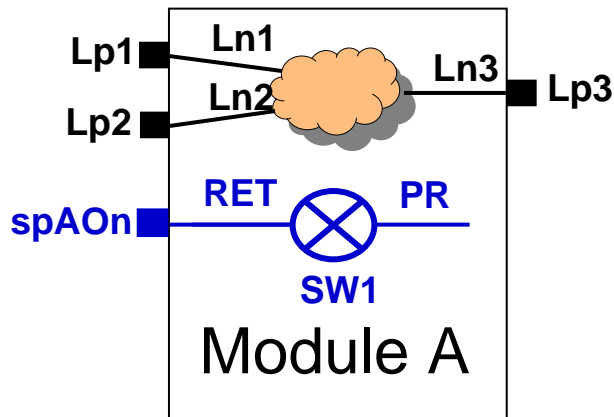
The UPF / Logic Design Relationship



- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy

```
connect_supply_net RET
-ports {spAOn}
```



Logic Design



connect_supply_net



```
connect_supply_net net_name
```

```
[-ports list]
```

```
[-pins list]
```

```
[< -cells list |  
-domain domain_name >]
```

```
[< -rail_connection rail_type |  
-pg_type pg_type >]*
```

```
[-vct vct_name]
```

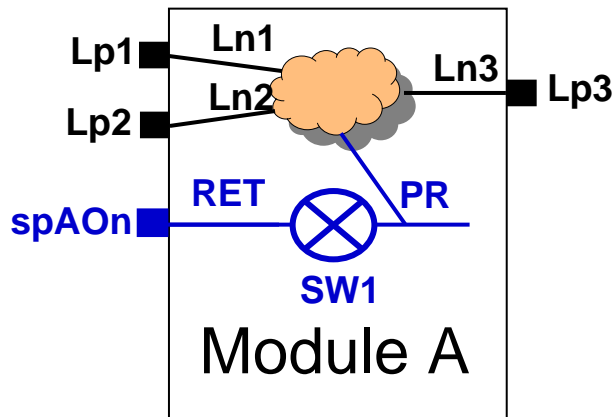
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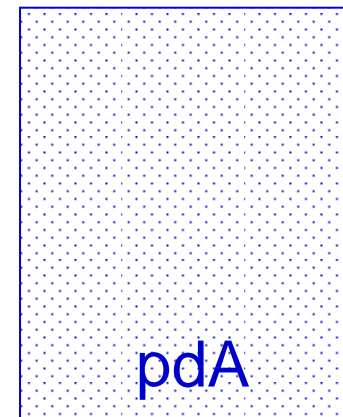
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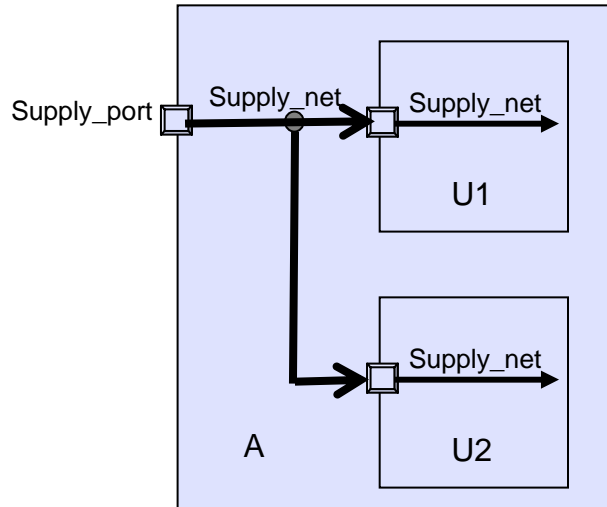
```
set_domain_supply_net pdA
- primary_power_net PR
- primary_ground_net VSS
```



Logic Design

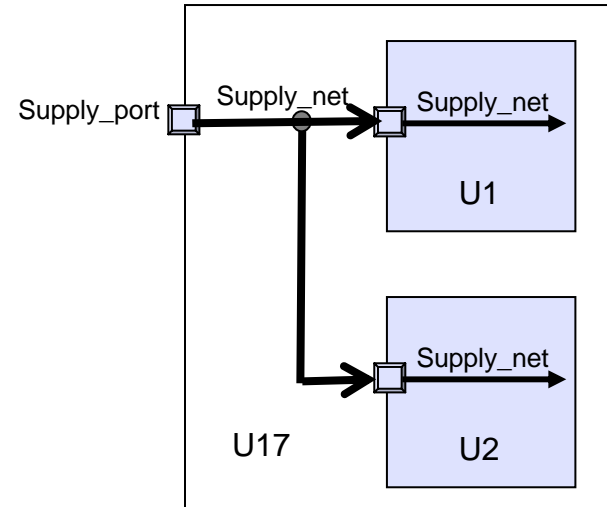


Automation



- Single create_supply_port command
- Single create_supply_net command
- Supply is “routed” to all design elements in PD

Flexibility



- PD can consist of non-contiguous design elements
- PD always has scope
 - Ports, nets, etc created in that scope
- Supply is routed to all design elements
- Auto re-naming avoids conflicts

Simulation Semantics Overview



- Key Concept:
All design elements in a power domain share the same primary power and ground supplies
- ON:
 - Both primary power and ground are ON
 - Supply port drives a voltage value
- OFF:
 - Primary power and/or ground are OFF
 - Voltage value is irrelevant
- PARTIAL_ON
 - For power-aware models may more accurately reflect switching capacitive transition

OFF Means



- All registers are corrupted
 - Retention (shadow) registers have separate supply(ies)
 - Logic types = X
 - Other types = default initial value
- Any signal/net driven by logic that is OFF is corrupted
 - Isolation cells have separate supply(ies)
- No evaluation of logic occurs while it is OFF

ON Means



- When logic is powered on (event)
 - Combinatorial processes are evaluated
 - Including continuous assignments
 - Edge triggered processes are not evaluated until the next active edge
 - Logic (processes) are re-enabled for evaluation

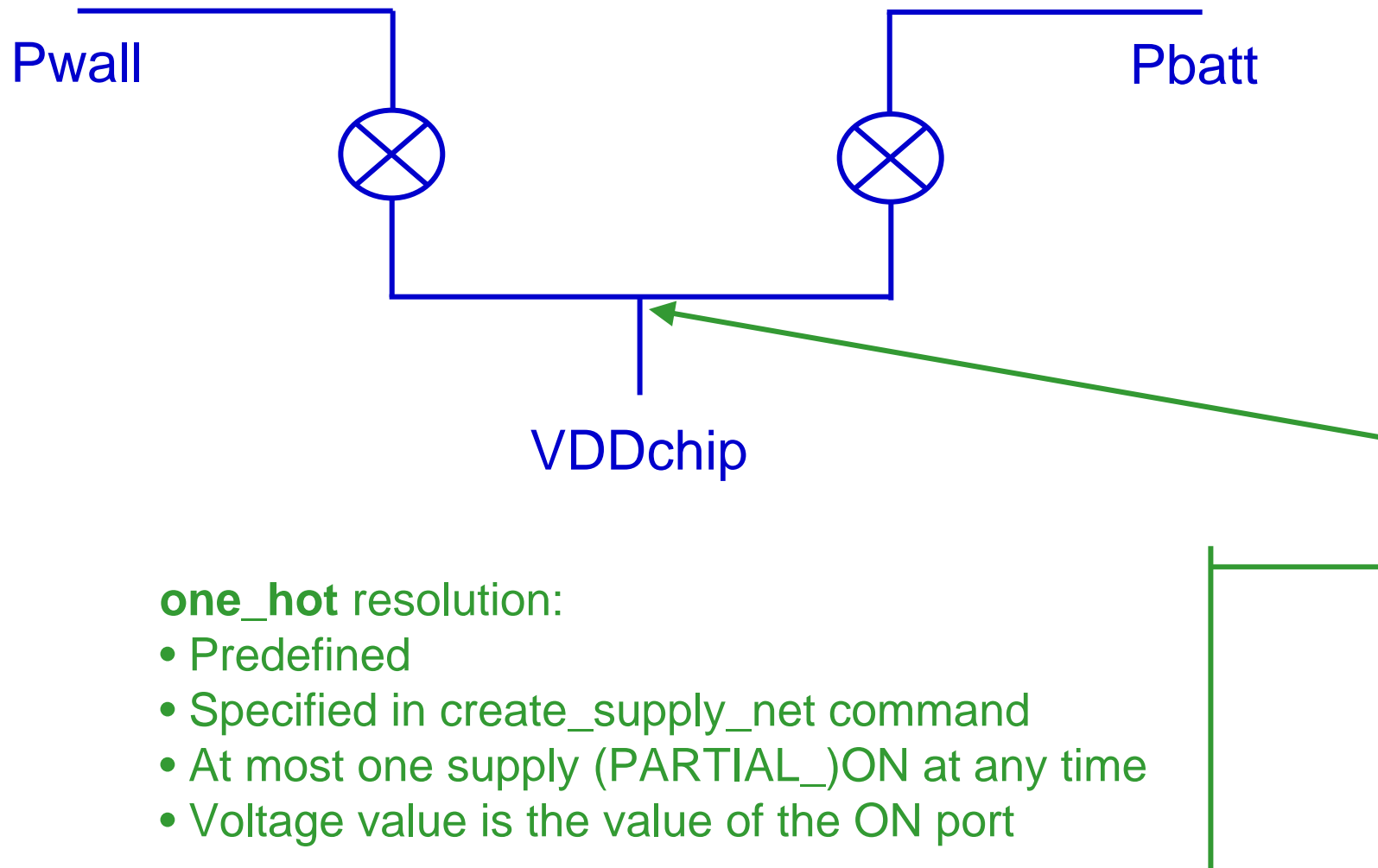
UPF / HDL Interoperability



- Accellera 1.0 UPF Standard
 - Packages

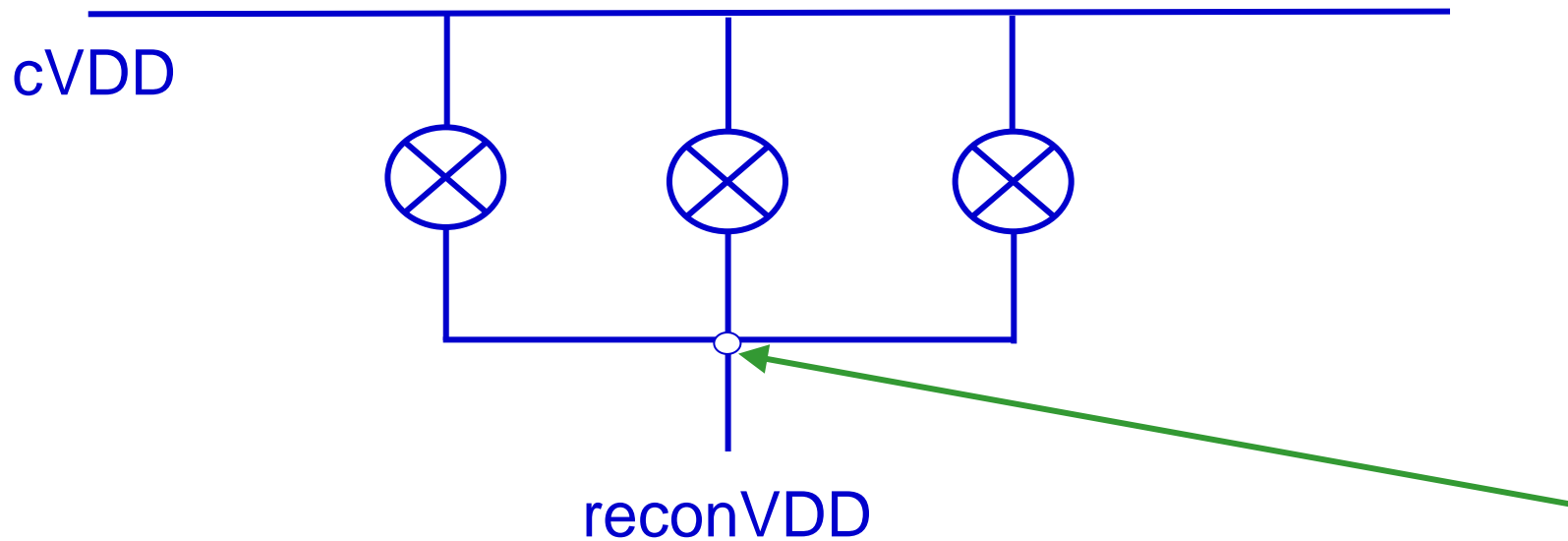
Supply Net Resolution

Distributed Switch



Supply Net Resolution

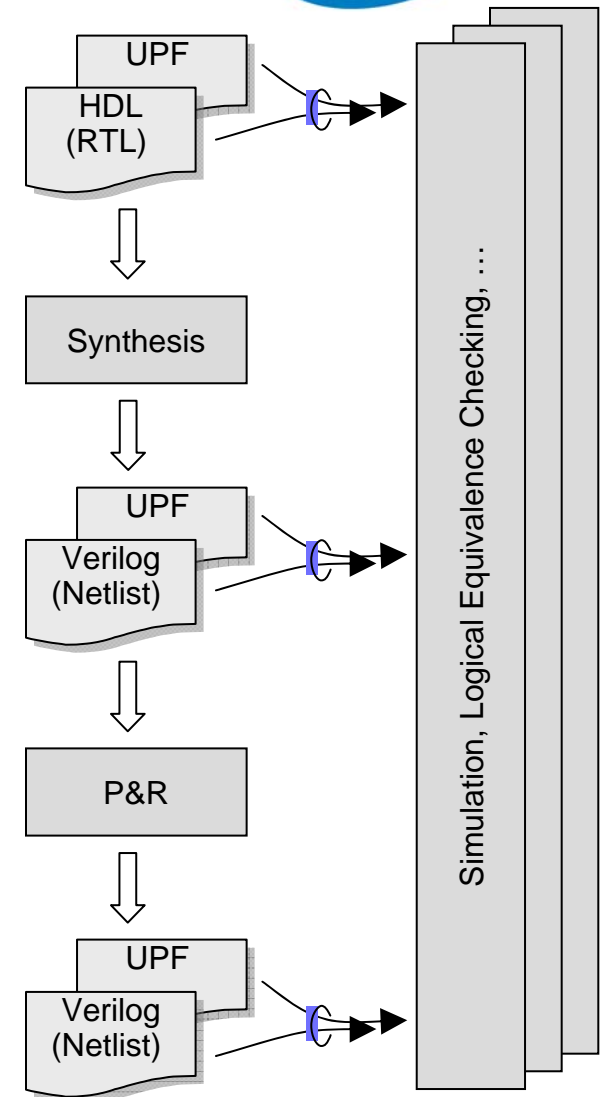
Parallel Switch



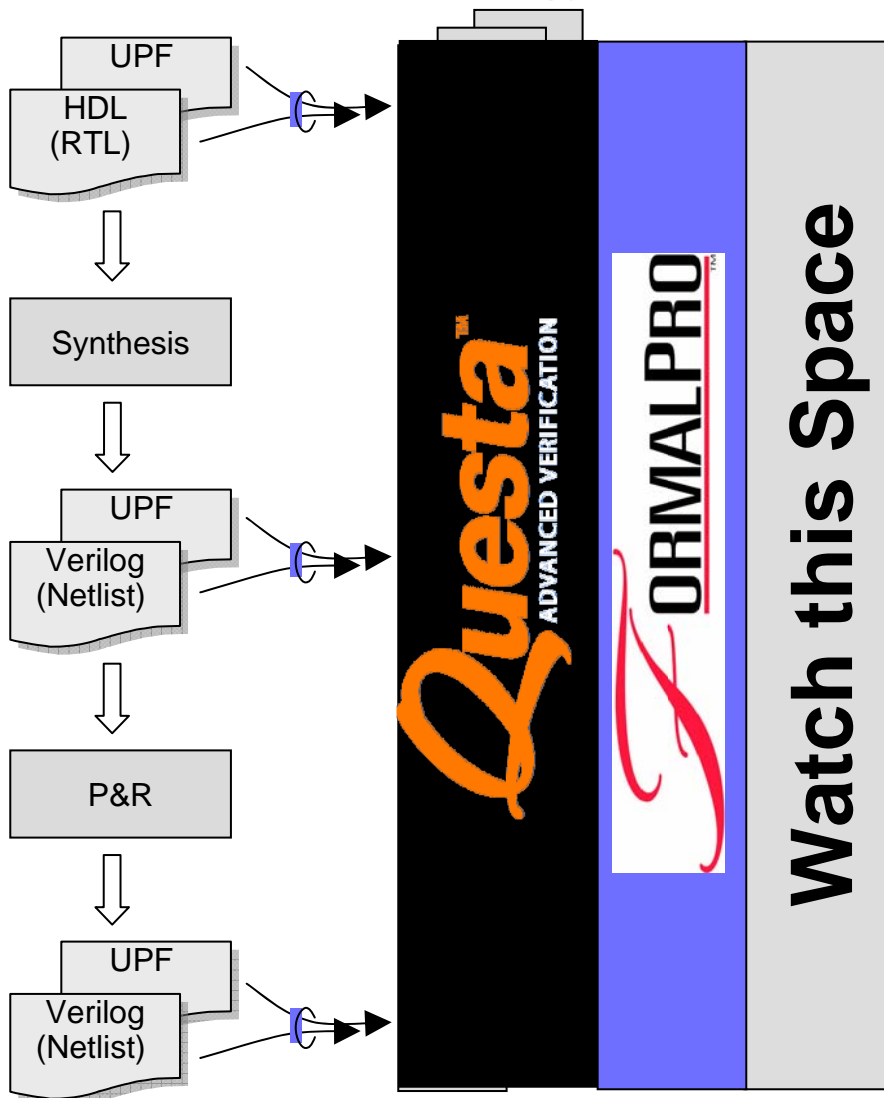
parallel resolution:

- Predefined
- Specified in create_supply_net command
- All must be OFF
- Or all must be ON and at same voltage
- If any PARTIAL_ON, then PARTIAL_ON

Mentor's UPF Low Power Design Verification Solutions

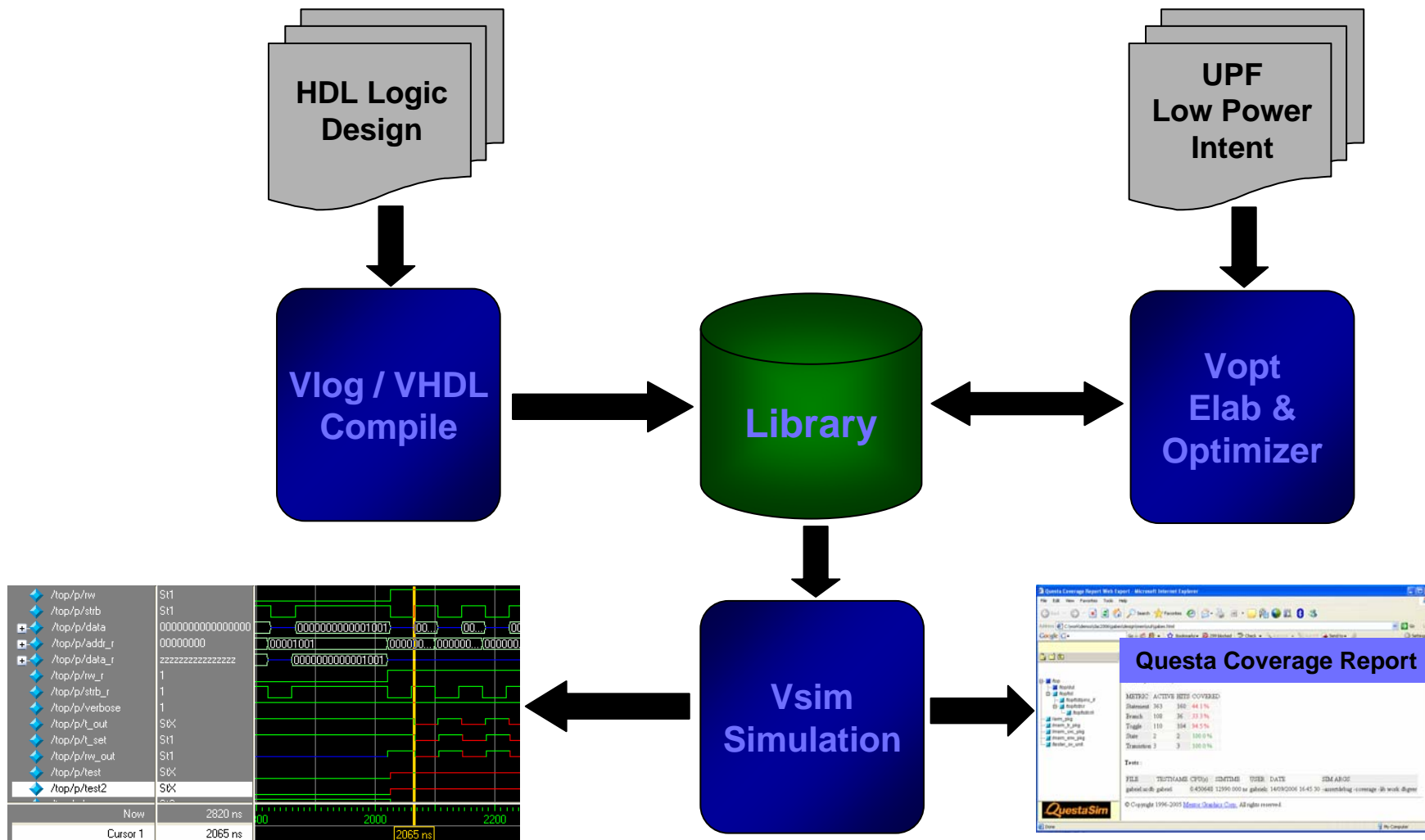


Mentor's UPF Low Power Design Verification Solutions



- Questa Simulation
 - RTL & gate verification of low power design intent
 - Power gating
 - Retention
 - Isolation
- FormalPro
 - Is the implementation equivalent to what was verified?

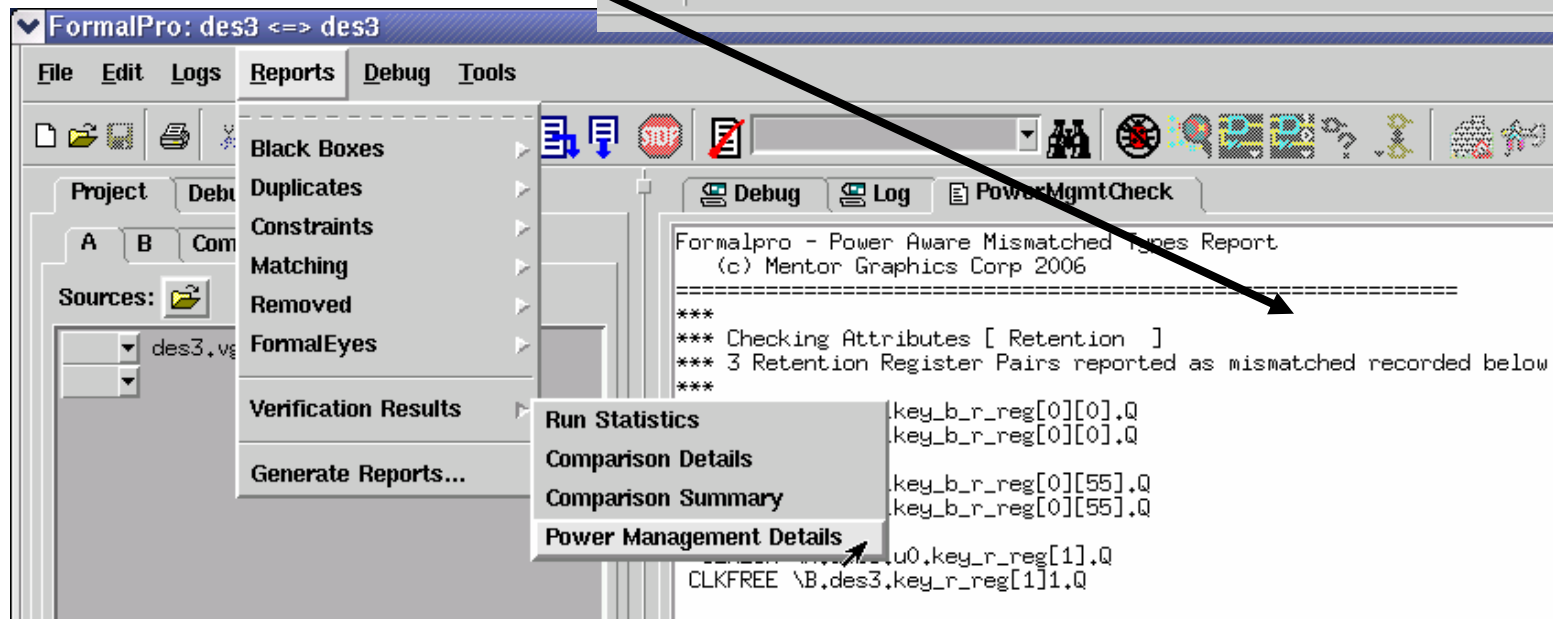
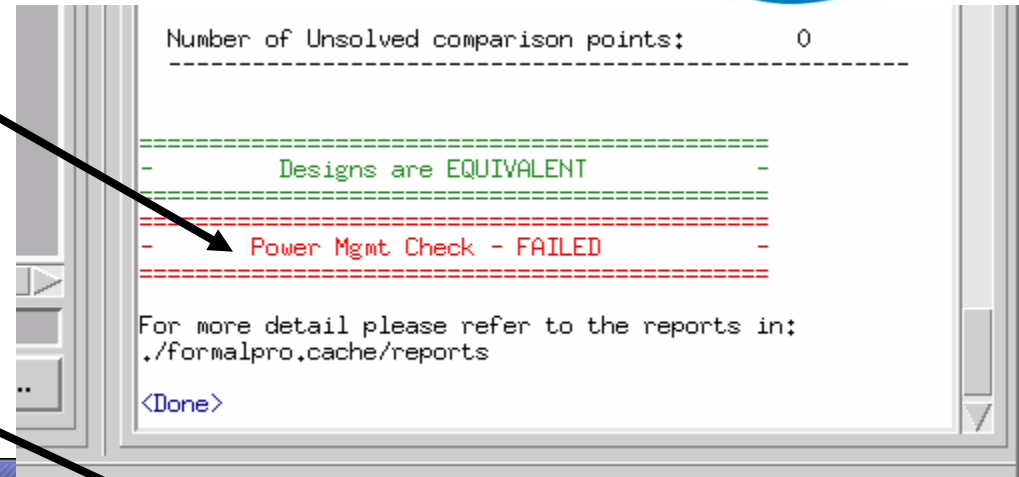
Questa Power Aware Simulation Flow



Low Power Equivalency Checks



- Power Management Status in the main transcript
- Power Management Details Report
 - Failed due to wrong register type





Unifying Low Power Design with UPF
The Power of One

Arvind Narayanan

Agenda



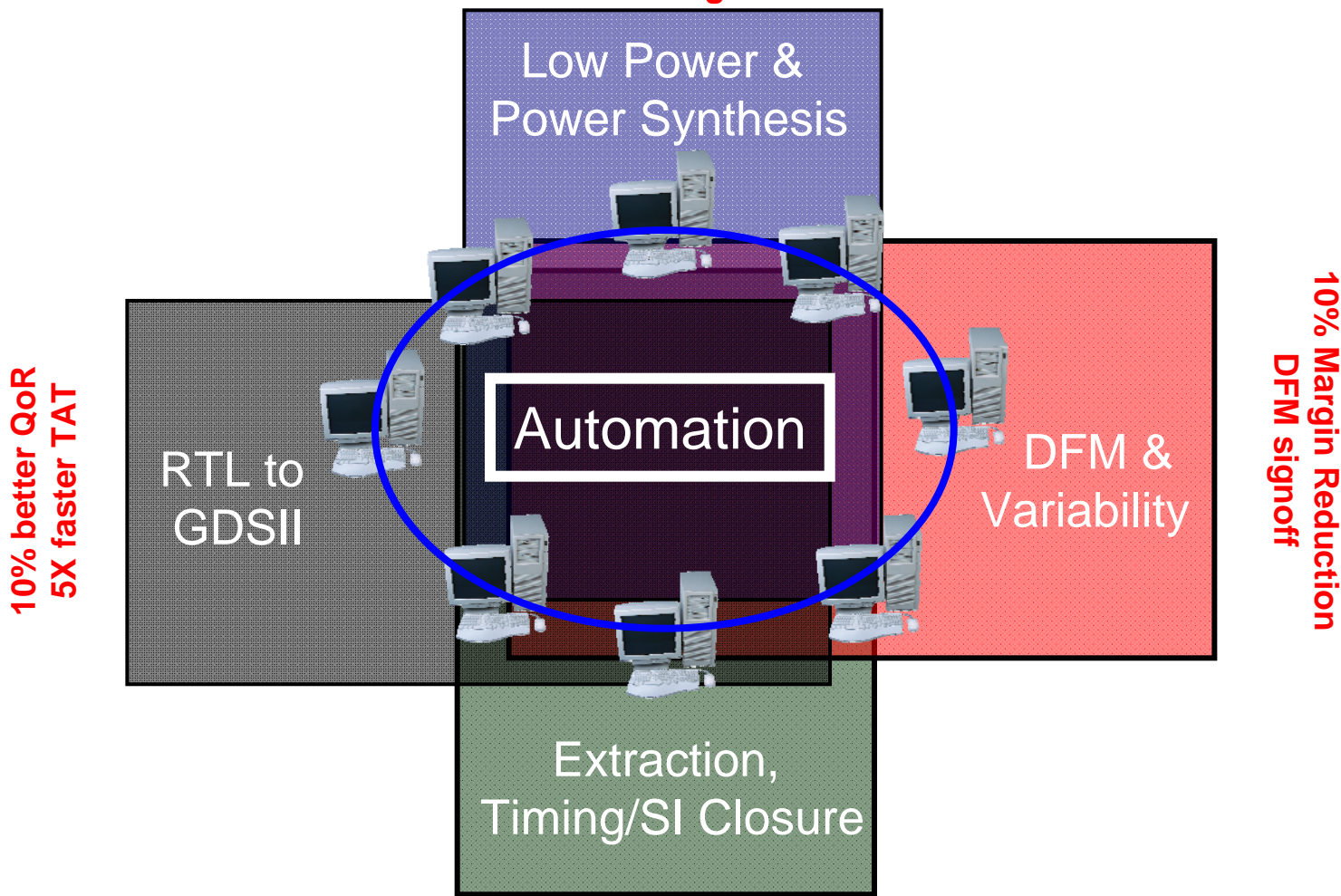
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Talus™ Platform

Rapid concurrent closure of timing, power and yield



25% less power
Power signoff

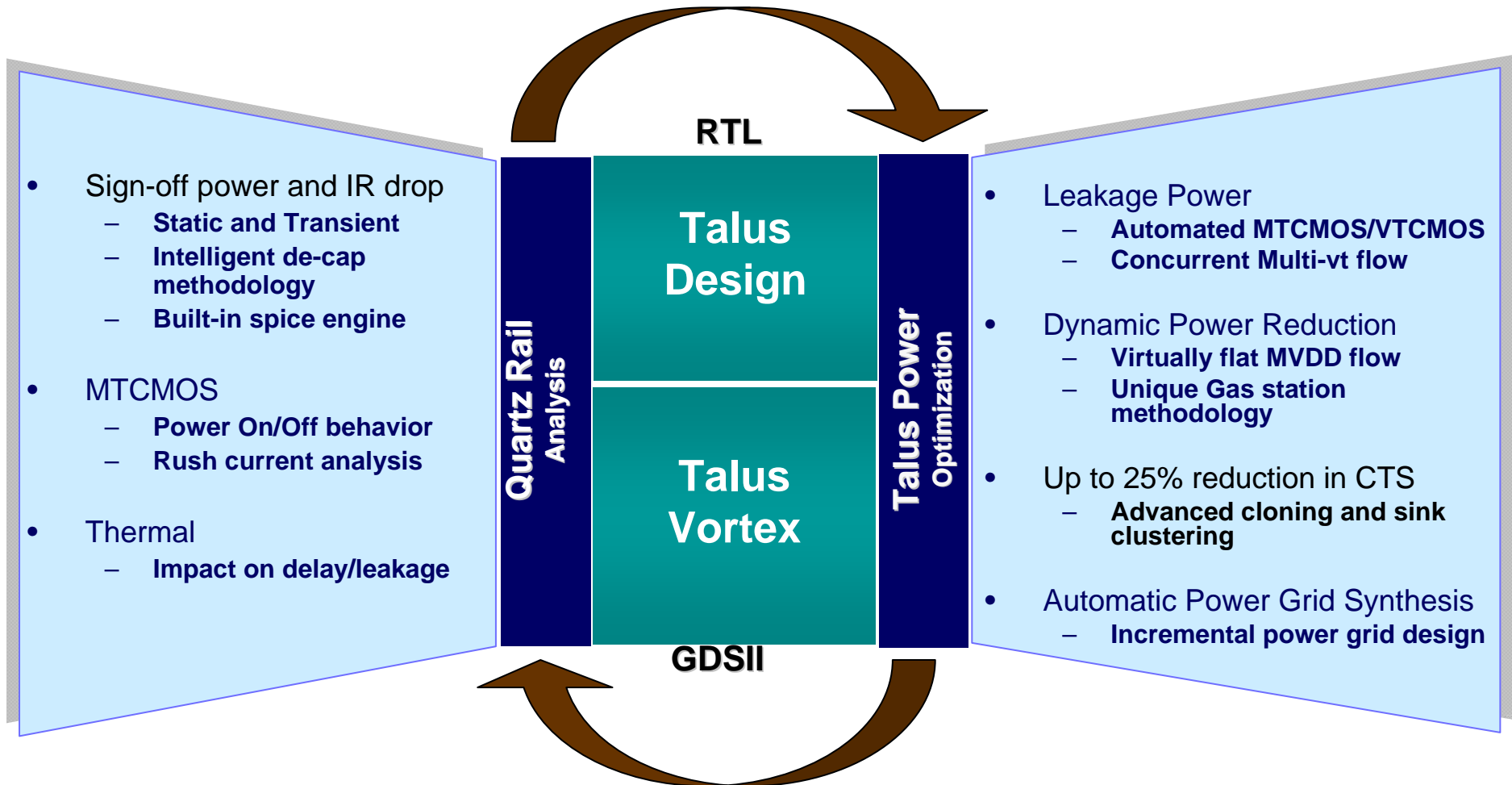


Signoff In the Loop

Total Power Optimization RTL to GDSII



Integration, Innovation, Automation!

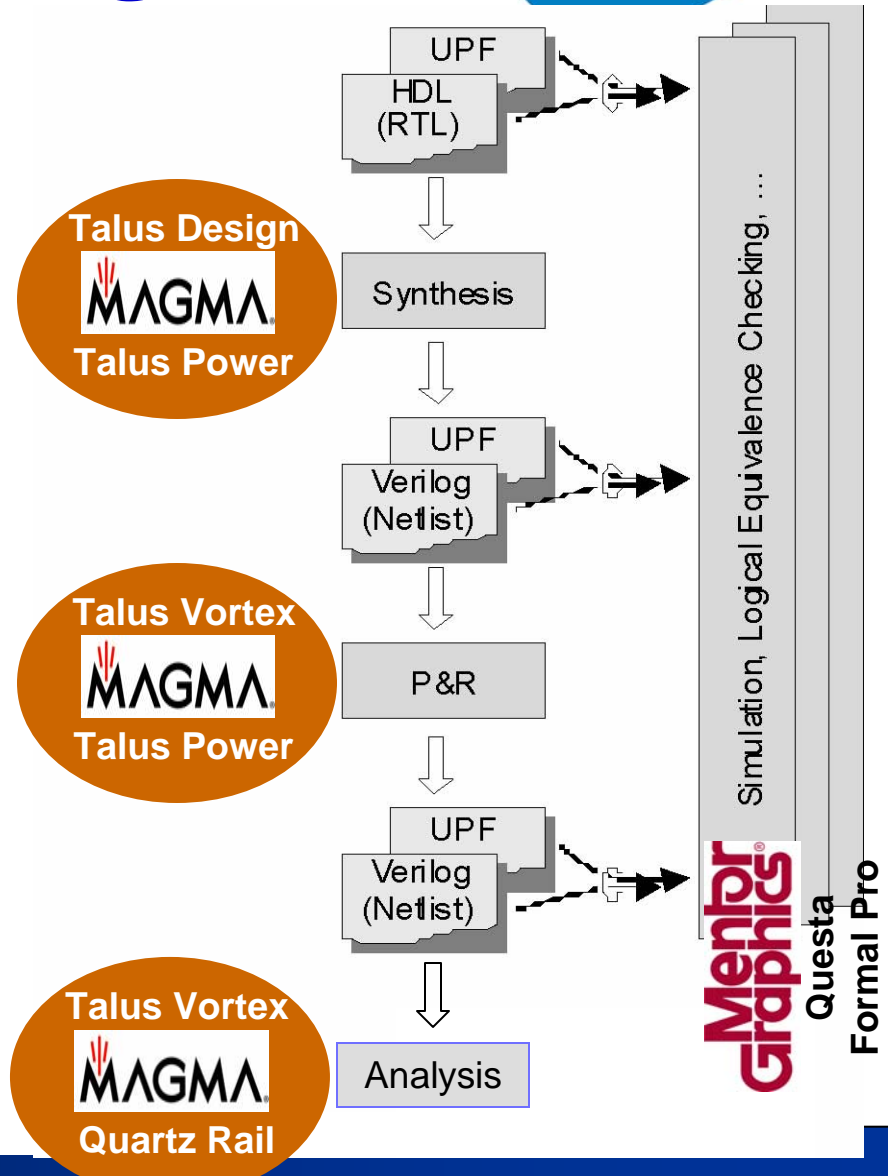


UPF Support in Magma



- Ability to allow the specification of implementation-relevant power information early in the design process
- UPF provides a consistent format to specify power-aware design information
- UPF also defines consistent semantics across verification and implementation
 - create_power_domain
 - create_supply_port
 - create_supply_net

Sample UPF Commands for MVDD flow



Complete Low Power Design Specification = HDL + UPF



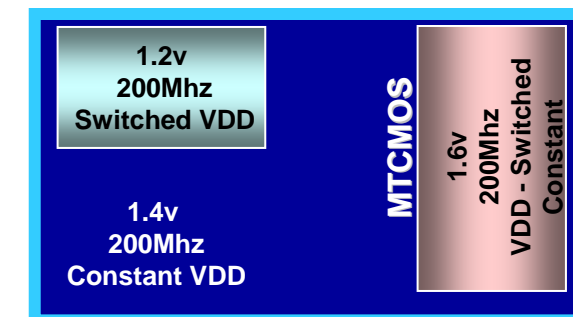
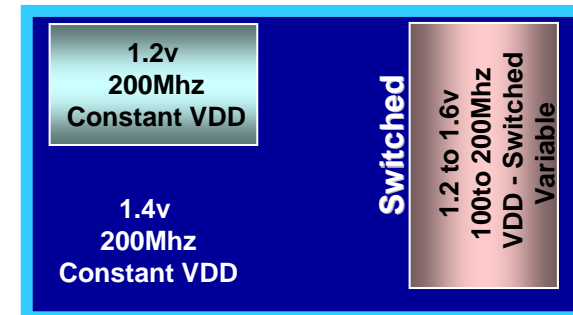
- Power Domains
- Power Distribution Network
 - Switches and Supply Nets
- Power State Table
- Level Shifting
- Isolation
- Retention
- Switching Activity

Automated Voltage Island Methodology

- Complete automated flow for defining and connecting domains
- Maintains virtual hierarchy in the flow
- Handles level shifters and isolation cell insertion
- CTS honors domain boundaries
- Routing and cells contained within domains
- Concurrent analysis and optimization



Types of MVDD Designs



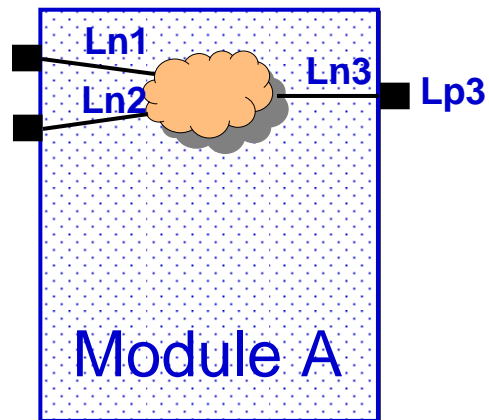
UPF / Logic Design Relationship



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```
create_power_domain pdA
  -include_scope A
```



Logic Design

pdA

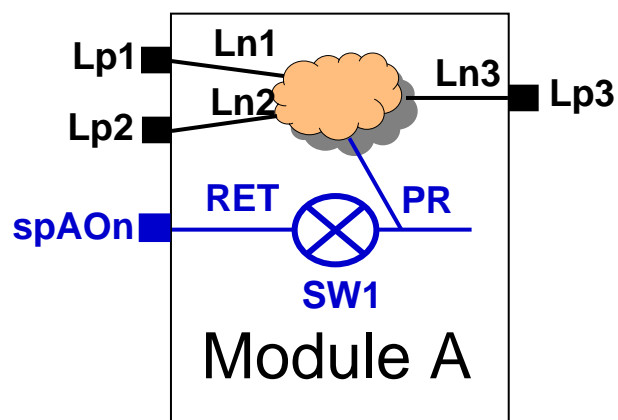
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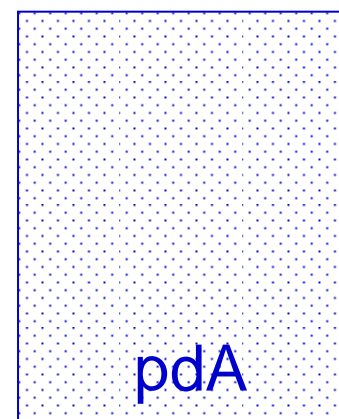
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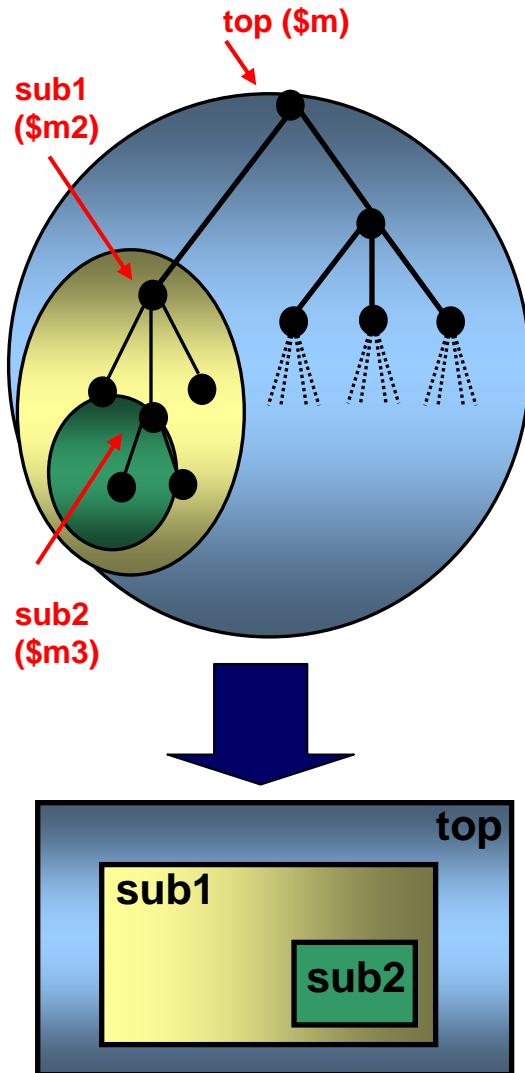
```
set_domain_supply_net pdA
  -primary_power_net PR
  -primary_ground_net VSS
```



Logic Design



Domain Creation and Mapping



- Domain Creation
- Attaching cells



- Domain Parameters
- Libraries for domain



- Floorplans for domains

Logical Mapping

Electrical Mapping

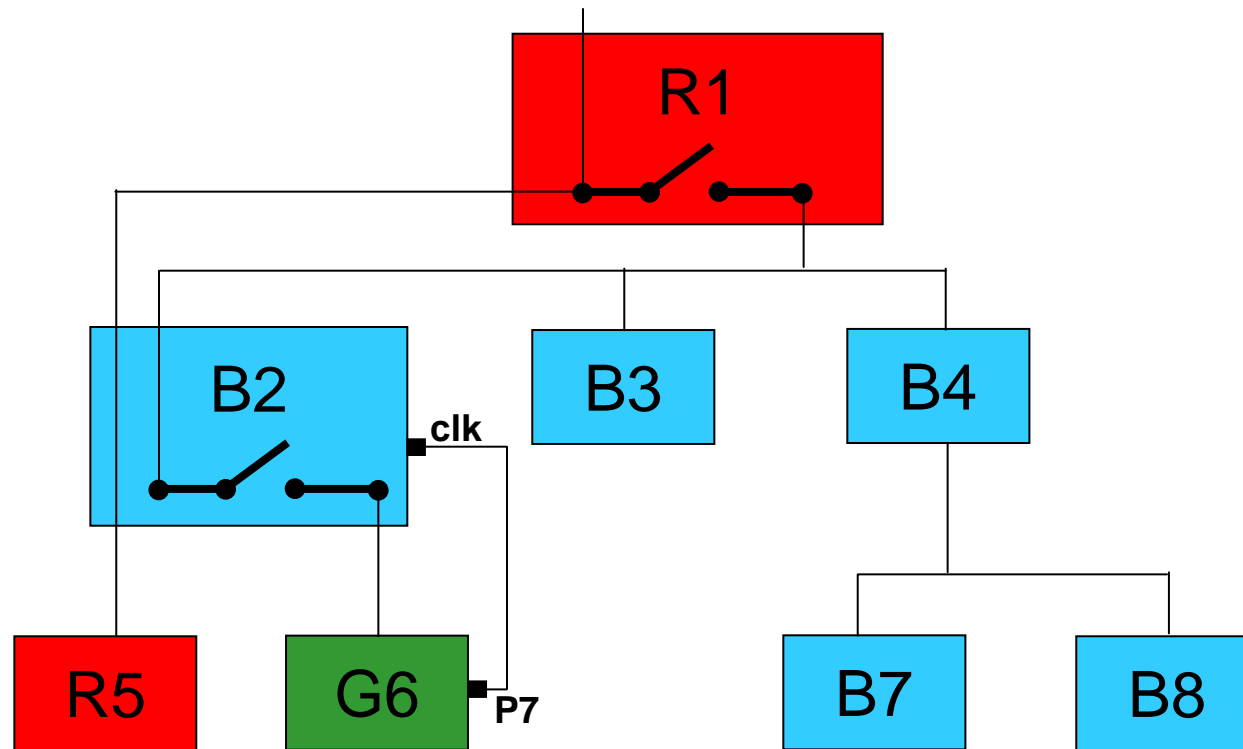
Physical Mapping

Level Shifters in MVDD flows



- Level shifters translate from one voltage swing to another
- Level shifter considerations:
 - Pick a power domain or a set of elements
 - Select input ports, output ports, or both
 - Tolerate a voltage difference threshold
 - UPshift or downSHIFT rule
 - Location (self, parent, sibling, fanout, auto)
 - Do or don't do it

Isolation Cells in MVDD flows



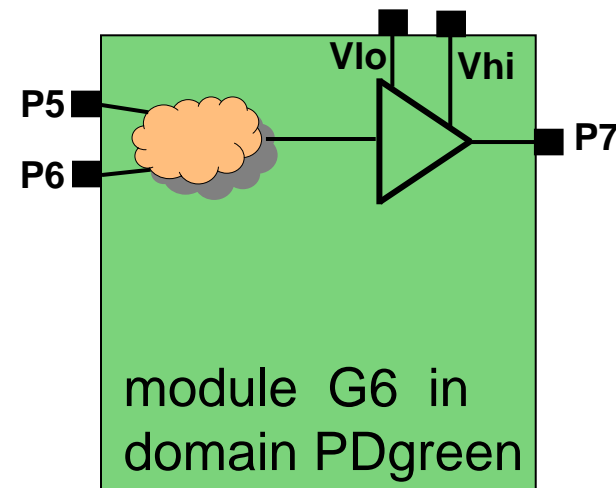
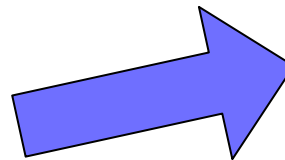
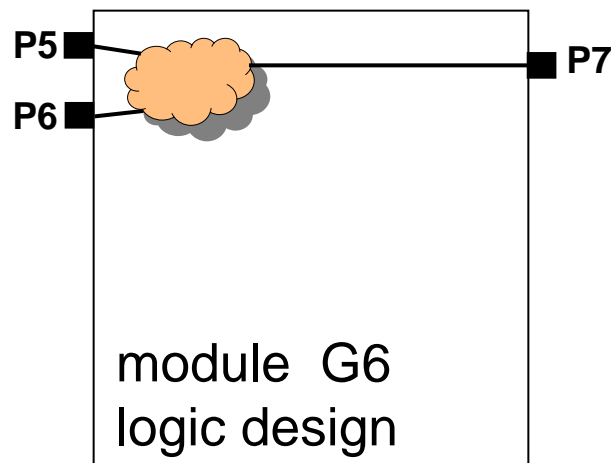
- Floating outputs of power-gated circuits
- Isolation control signals force known value
- Isolation and level shifting can be merged

set_level_shifter Command Example



```
set_level_shifter my_ls
-domain PDgreen
-rule low_to_high
-location self
-applies_to outputs
```

```
map_level_shifter_cell
ls_L2H
-domain PDgreen
-lib_cells { /lib/ls_123 }
```

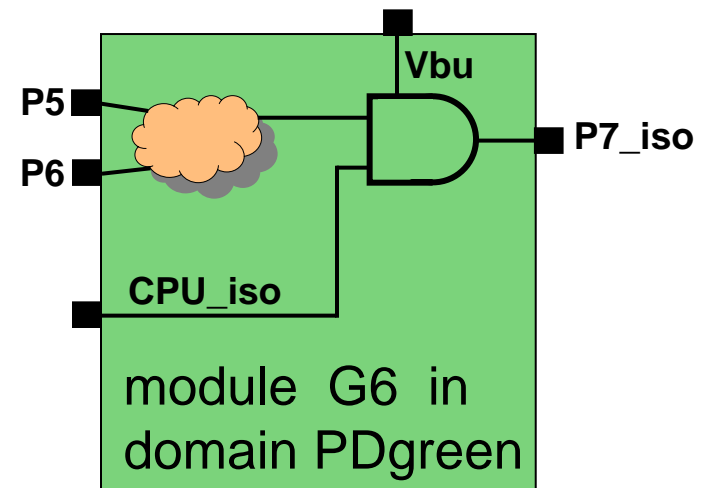
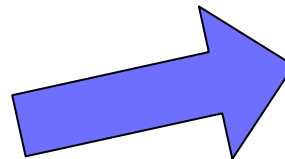
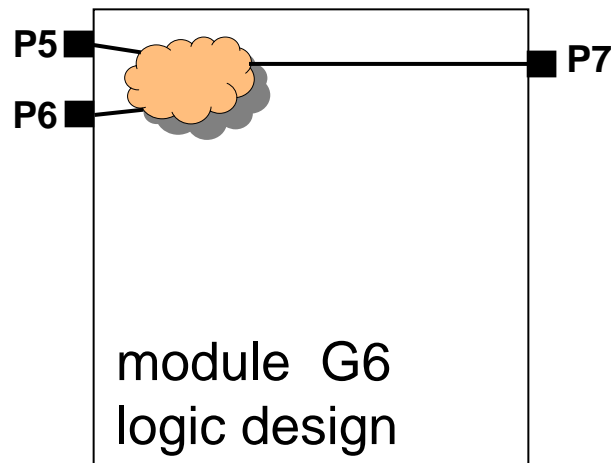


set_isolation Command Example



```
set_isolation iso3
-domain PDgreen
-isolation_power_net Vbu
-clamp_value 0
-applies_to outputs
```

```
set_isolation_control
iso3
-domain PDgreen
-isolation_signal CPU_iso
-location self
```



Level Shifter/Isolation Cell Insertion - Magma



- Uses supply type definition for LS/ISO insertion
- Length and IR drop based insertion

run gate levelshifter -UPF
run gate isolation -UPF

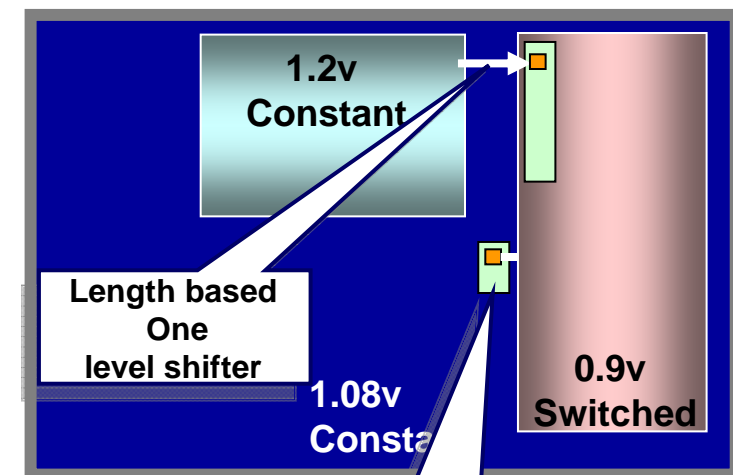
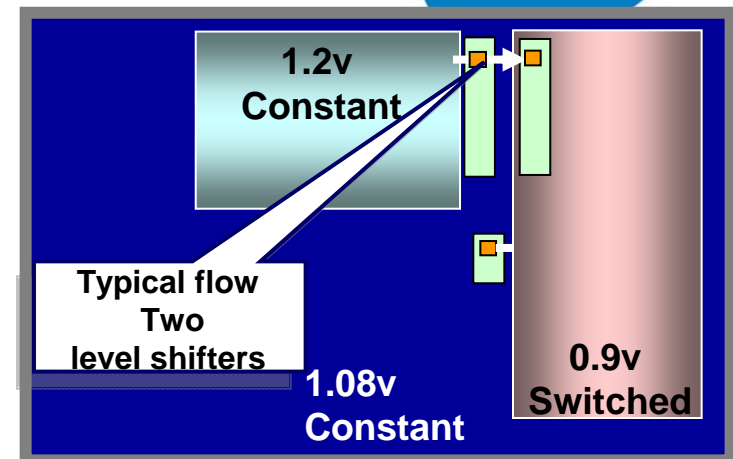
Supply Types

Constant - voltage supply is constant over time

Variable - voltage supply varies over time

Switched constant - constant voltage supply that can be switched off

Switched variable - variable voltage supply that can be switched off

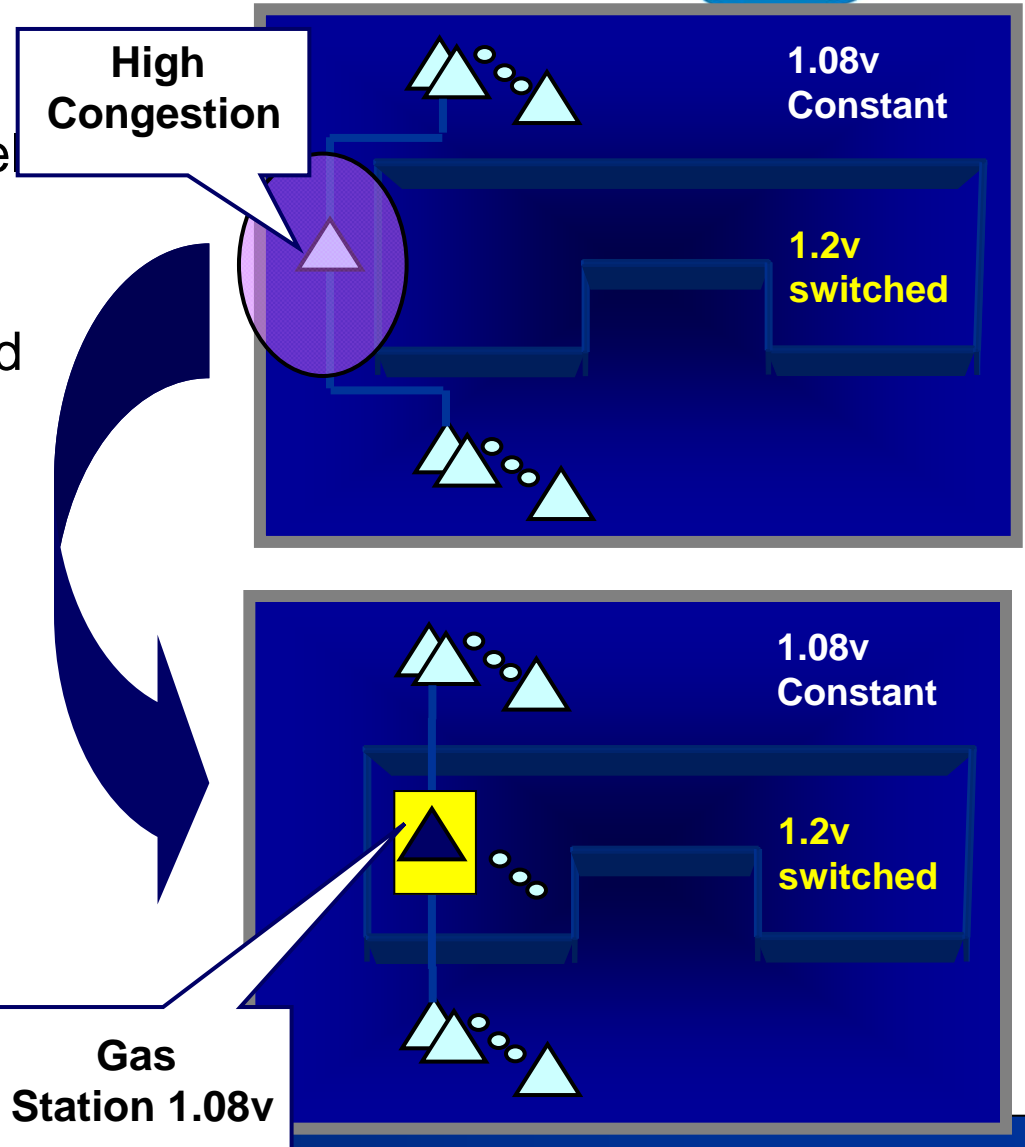


Isolation cell insertion

Gas Station Methodology for MVDD Flow



- Mini islands to help buffering long top level nets without level shifters
- Helps handle doughnut shaped domains with congestions
- Buffering on long nets through switched domains can be gracefully handled
- Automatic power tapping from the top level supply
- Optimal number of repeaters and supply taps inserted

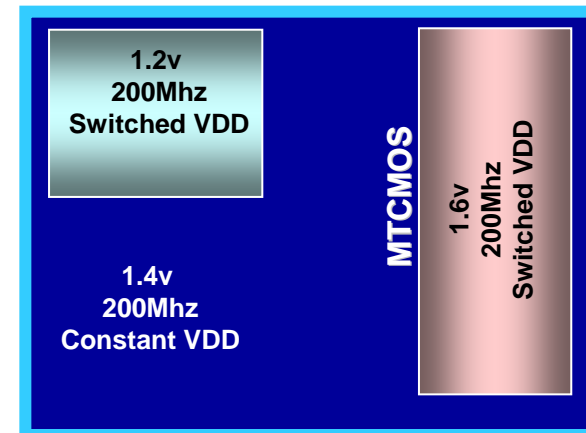


MTCMOS Switches



- Coarse Grain Distributed Switches
 - **Switches placed in rows to control groups of logic**
- Standard cell specific Switches
 - **A domain replaced with cells that have header and/or footer switches**
 - **Easier to implement at the cost of area**
- Fine Grain Distributed Switches
 - **Cones of logic replaced with cells with header/footer switches**
- Global Header/Footer Switches
 - **MTCMOS switches at the periphery of the domains**

MVDD based MTCMOS Methodology



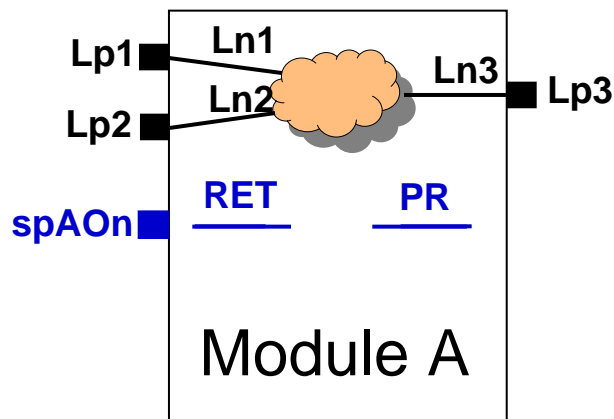
UPF / Logic Design Relationship



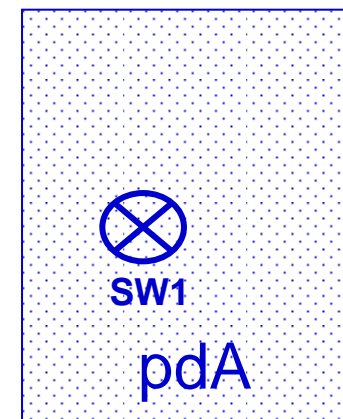
- Key Concept:

Everything defined in UPF exists in the Logic Hierarchy

```
create_power_switch SW1 -domain pdA
  -input_supply_port {inp RET}
  -output_supply_port {outp PR}
```



Logic Design

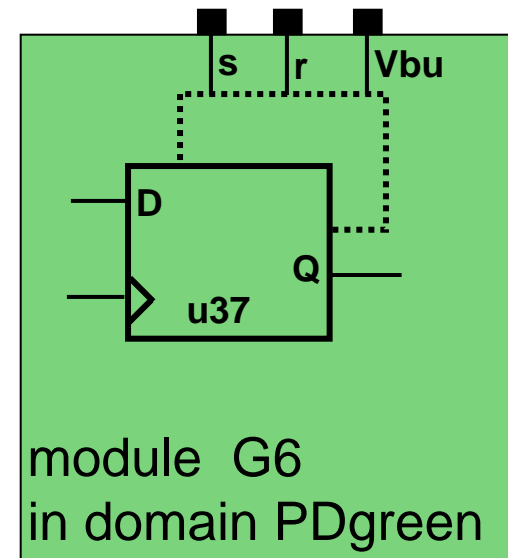
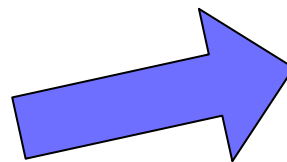
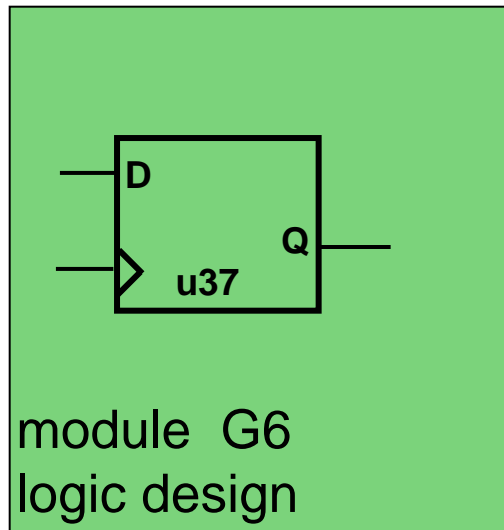


set_retention Command Example



```
set_retention ret3
-domain PDgreen
-retention_power_net Vbu
-elements { u37 }
```

```
set_retention_control
ret3
-domain PDgreen
-save_signal s
-restore_signal r
```

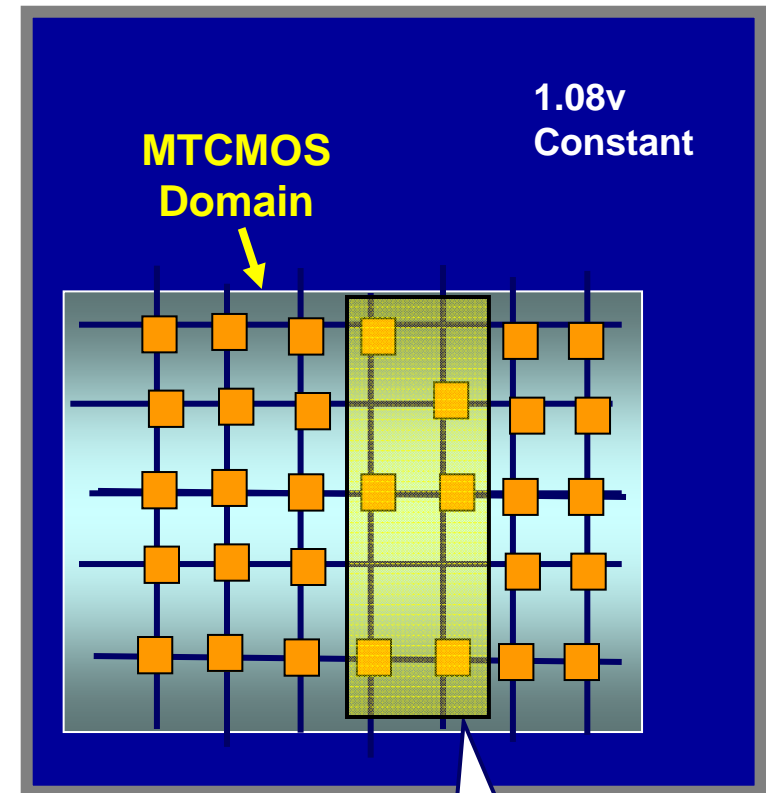


Coarse Grain Insertion Methodology



- Number of switches inserted is based on:

- Explicit – Switches inserted on every grid point
 - Minimum # of switches per row – user defined
- Power – Total power being consumed by a block
 - Evenly distributed over the placeable area
- Voltage Drop – Rail analysis used to determine the location of the current sinks



- Voltage aware incremental switch insertion/removal

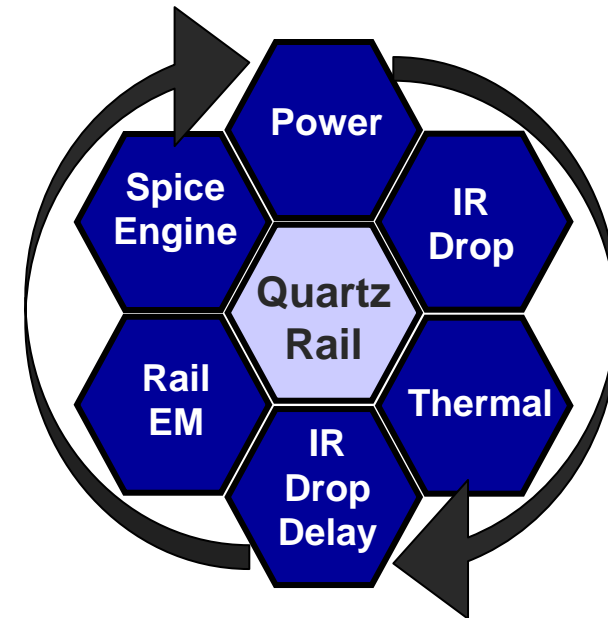
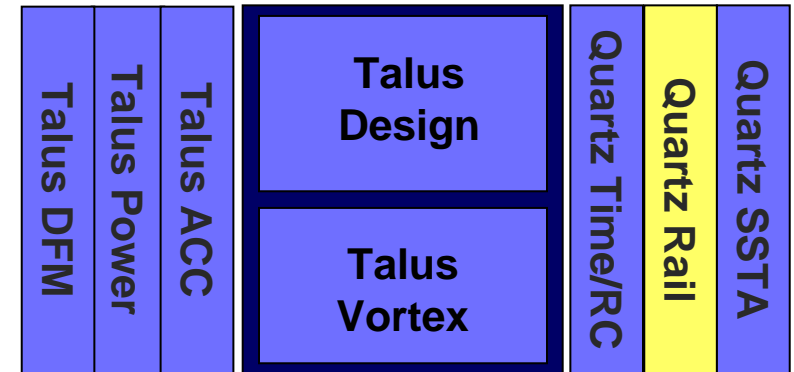
run gate switch **-UPF**

IR Drop based
Incremental
removal/insertion

Quartz Rail - Power Integrity Sign-Off



- Standalone Power sign-off accuracy with early predictability
- Concurrently addresses power, voltage drop, electromigration, Thermal and Timing issues
- Analyze impact of temperature on leakage and performance
- On-the-fly characterization for accurate dynamic IR drop analysis
- Leakage optimization through intelligent de-cap insertion
- MTCMOS power-on and rush current analysis



UPF Roadmap

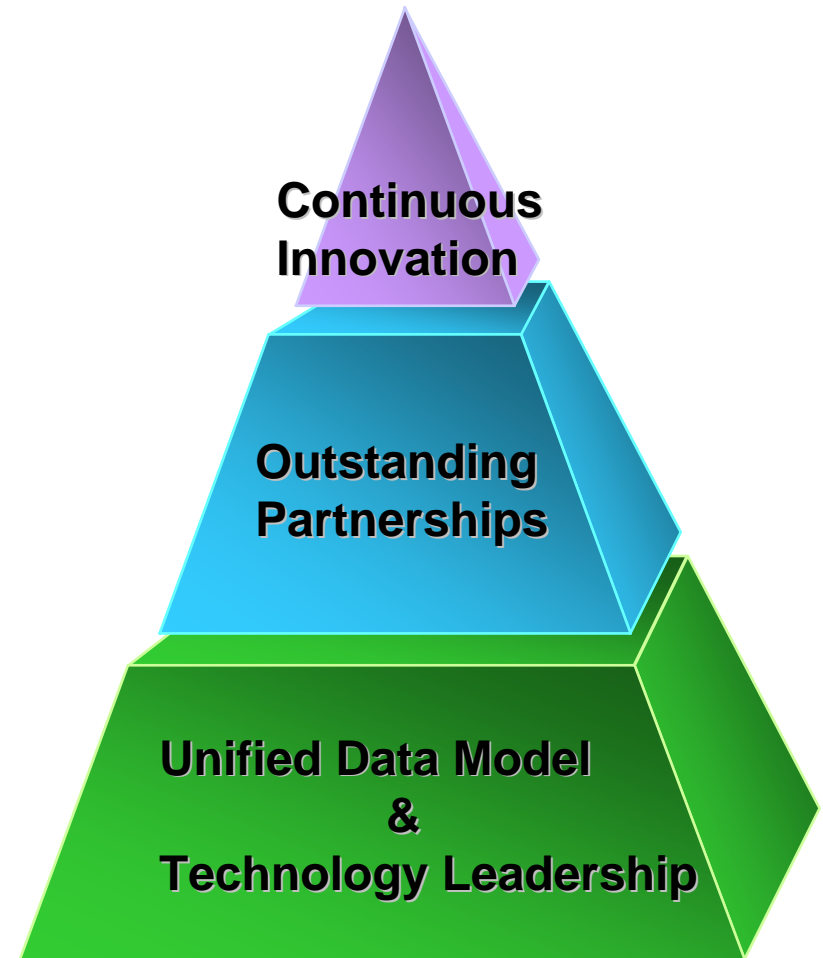


- UPF version 1.0 released – Feb 22nd 2007
- Magma support for UPF
 - UPF Implementation support – May 07
 - Talus Power for Implementation
 - Quartz Rail for Analysis

Comprehensive Power Management Solution



- Advanced power management techniques from RTL-to-GDSII
- Unique architecture - Single executable, Unique data model
- Embedded analysis - enables concurrent power, timing, area tradeoffs
- Reference Methodology provides well-defined design guidelines



Agenda



- Introduction (00:15)
 - Kevin Kranen, Synopsys
- UPF Low Power Design Basics (00:30)
 - Stephen Bailey, Mentor Graphics
- Low Power Design Implementation (00:30)
 - Arvind Narayanan, Magma Design
- **Comprehensive MV Verification (00:15)**
 - Anand Iyer, ArchPro
- Q & A



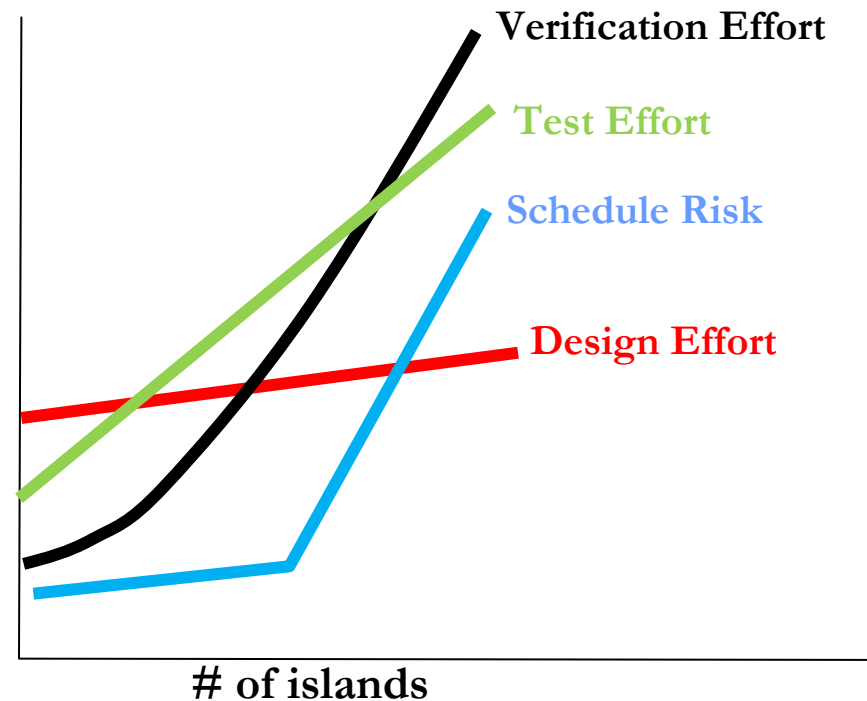
UPF Workshop

Anand Iyer
Senior Director of Marketing
ArchPro Design Automation

Do Designers Need UPF?



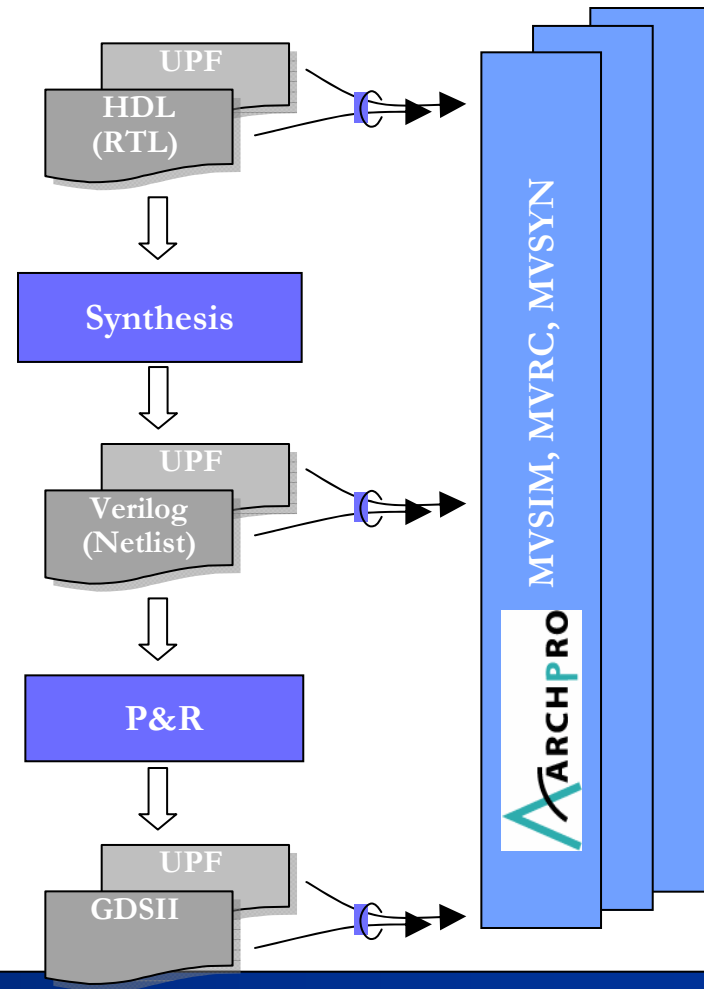
- Manage complexity
 - # of islands in a single chip is growing
 - Adhoc methods/scripts are useless after 3 islands
 - Formal definition of power intent is a must
- Consistent flow across the design stages
 - Support for UPF is available across the flow
 - Descriptive and prescriptive



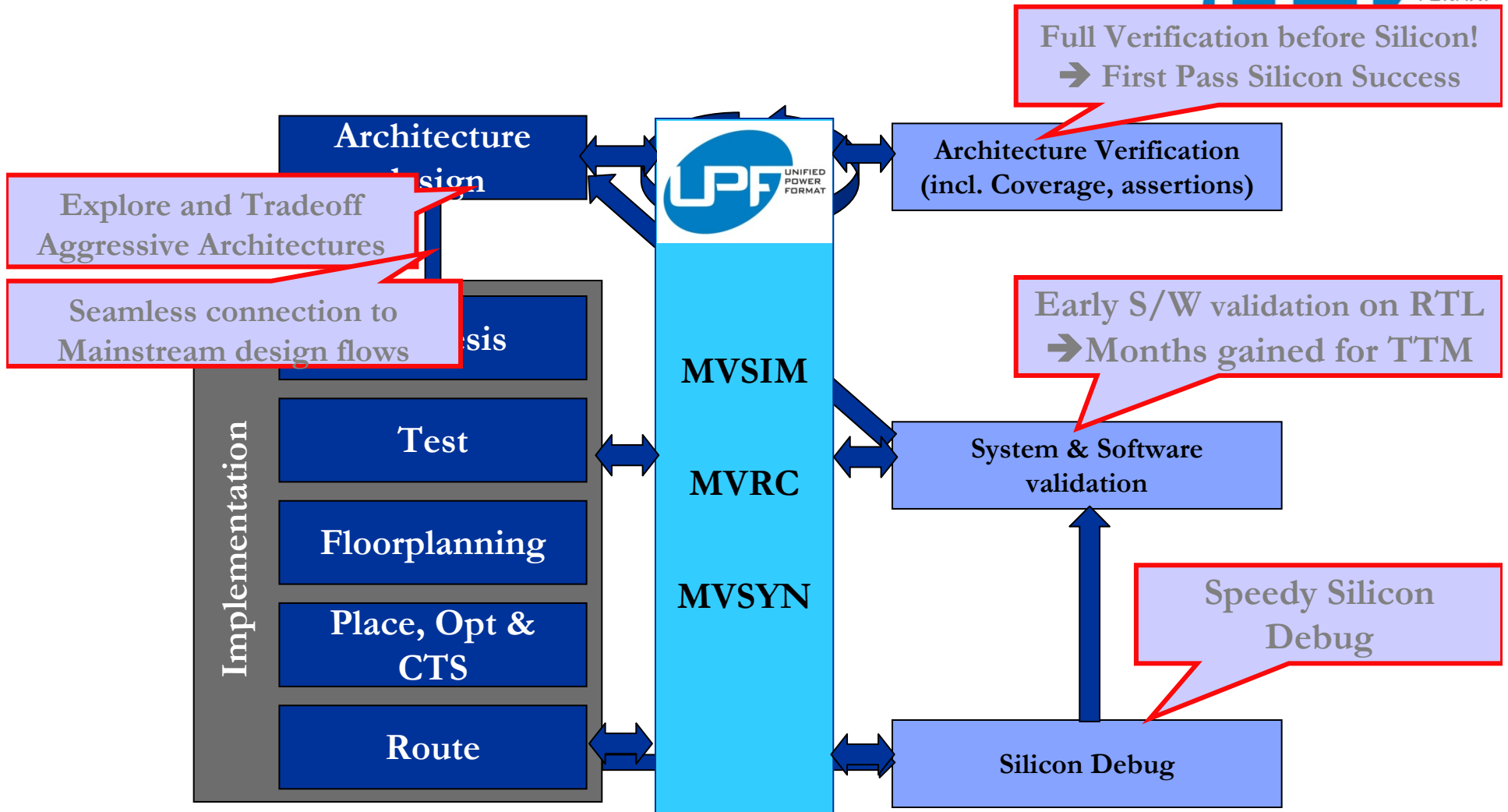
UPF provides a structured design flow

ArchPro Support of UPF

- Comprehensive MV verification based on UPF
- Read-only support of UPF by DAC 07 (June 2007)
- Read/write support – Q4 07



ArchPro : Proven solution at 65nm

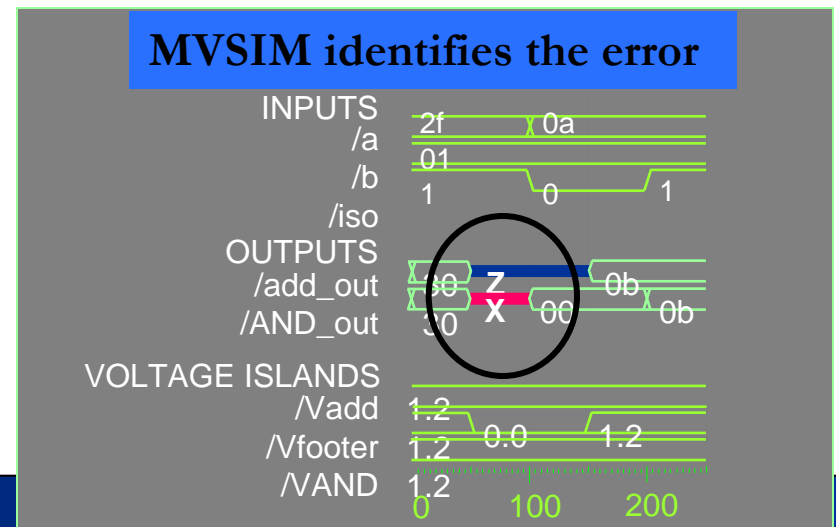
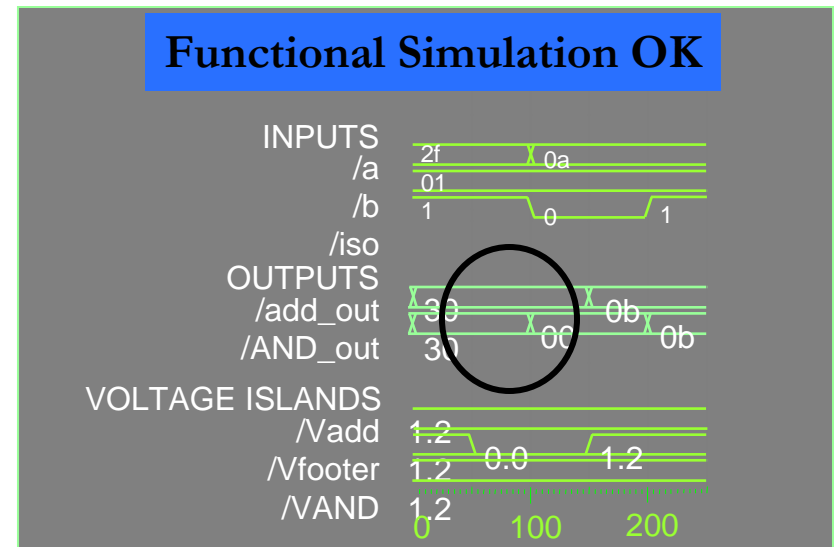


Accelerating Multi-Voltage Low Power Designs

ArchPro Solutions with UPF Support



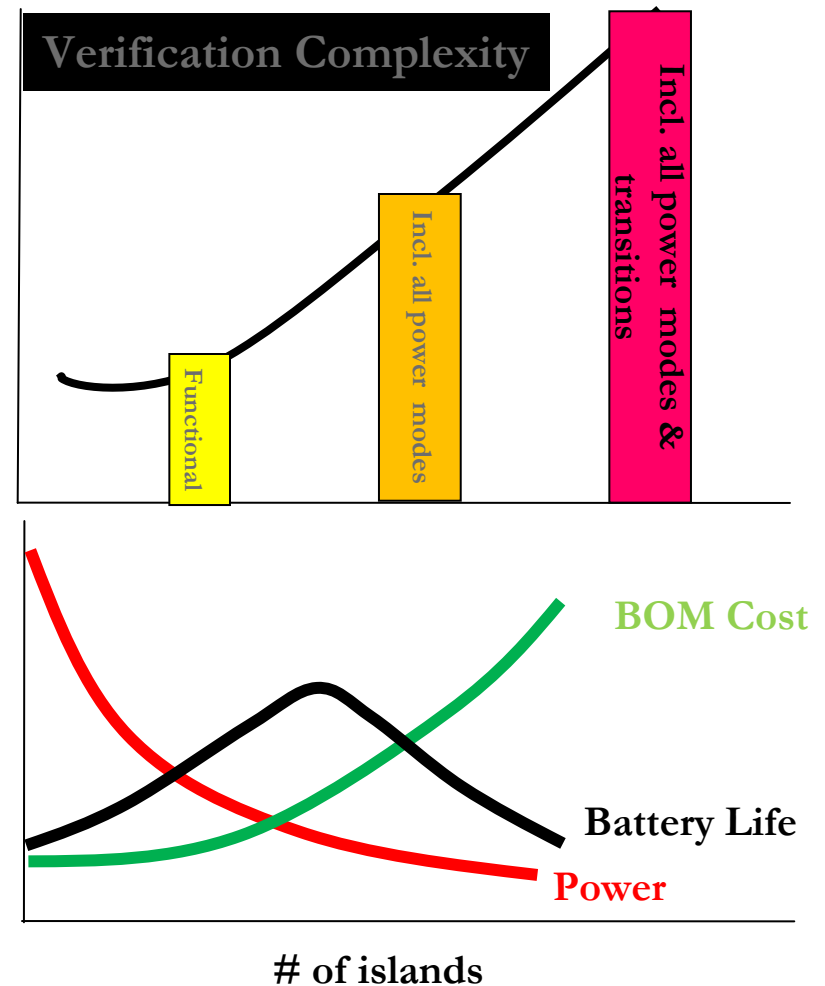
- MVSIM
 - Multi-voltage co-simulator works with ModelSim and VCS
- MVRC
 - Vectorless verification of multi-voltage conditions
 - Power sequence prediction
- MVSYN
 - Scriptless insertion of protection devices into RTL



How Does ArchPro's UPF -based Flow Help You?



- Manage verification complexity
 - Complete coverage of the states and transitions
 - User generated assertions cover all legal conditions
- Implementation is guaranteed to be clean
 - Directives for implementation tools
 - Sign-off checking for any errors
 - Help in silicon de-bug
- Compare multiple power architectures for feasibility



What's Next ...



- The Panel
- Get involved with UPF for your customer's sake
 - Download current standard at accellera.org
 - Join the IEEE P1801 study/working group
 - UPF Workshop at DAC



THANK YOU



Atrenta Support of Unified Power Format (UPF)

Piyush Sancheti

The Need for a Power Standard



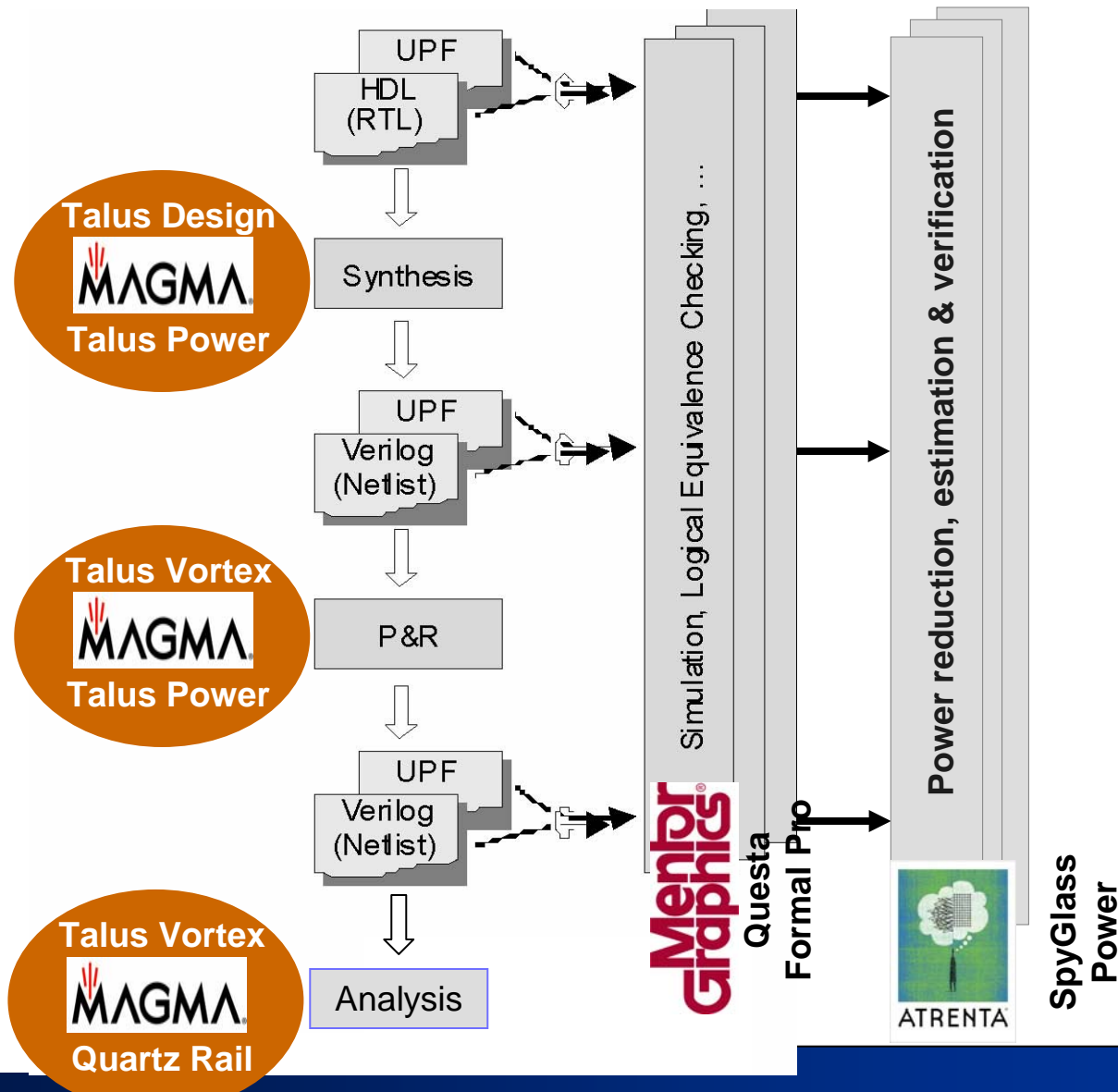
- Power-aware design requires specification of power intent
- No existing standard for power intent specification
 - Power intent described in Atrenta SGDC format for SpyGlass
 - Other EDA tools have proprietary formats
 - Customers have internal formats
- Power standard is important
 - Consistent power intent throughout the design flow
 - Interoperability between EDA tools
 - Ease of adoption and consistent results from power-aware design tools
- Atrenta power solution
 - Voltage and power domain verification
 - Power domain sequencing verification
 - Domain-aware power estimation
 - Power reduction and planning

Atrenta Support for UPF

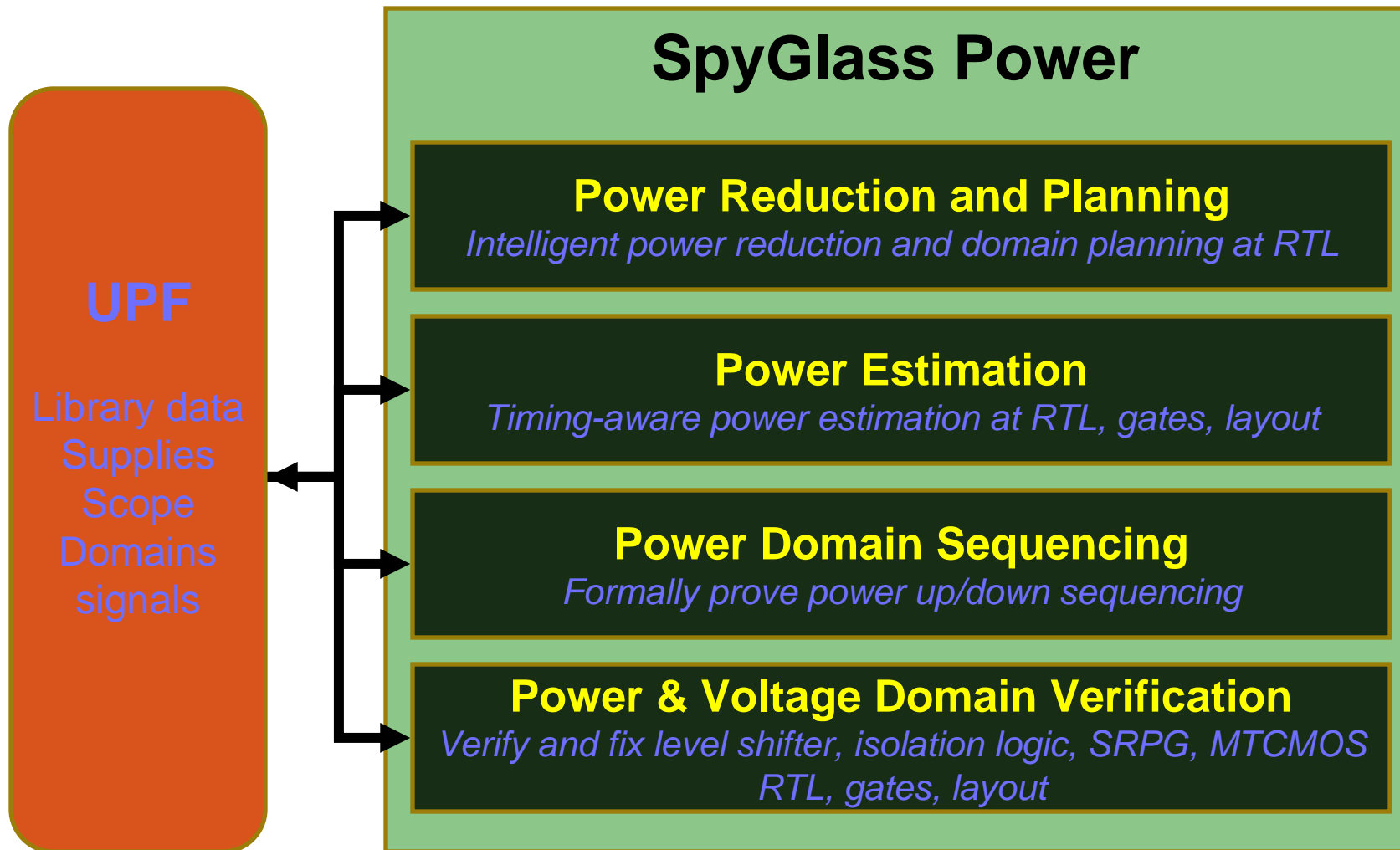


- Atrenta is an active participant in UPF
 - Strongly support efforts for unification of power formats and IEEE standardization
 - Donated SpyGlass SGDC format to Accellera in 2006
 - Participate in technical sub group (TSG) & IEEE p1801 working group
 - Dave Allen (Power Architect) represents Atrenta in UPF
- Atrenta plans to support UPF in SpyGlass Power by July 2007
- Atrenta will work closely with customers for UPF support in SpyGlass Power
 - Provide a transition path from/to SpyGlass SGDC format to/from UPF
 - Ensure UPF support in SpyGlass is adequate and robust for use in design projects
 - Work with UPF members to resolve any tool interoperability issues

UPF Support in SpyGlass Power



SpyGlass Power Requirements from UPF

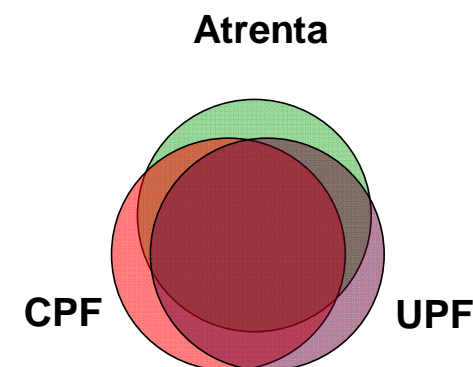


UPF examined



- UPF contains all the major categories required by Atrenta SpyGlass
- Atrenta is planning a power format translator for our customers

CPF	Atrenta	UPF	CPF	Atrenta	UPF
Library			Design - powerswitches		
define_always_on_cell	always_on_cell	set_pin_related_supply	create_power_switch_rule		create_power_switch
define_isolation_cell	always_on_pin	set_power_switch	update_power_switch_rule		map_power_switch
define_level_shifter_cell	aonbuffer		Design - always on		
define_open_source_input_pin	apcell		identify_always_on_driver	aonbufferedsignals	
define_power_clamp_cell	inisocell		Design - scoping		
define_power_switch_cell	isocell		end_design	current_design	load_upf
define_state_retention_cell	pgcell		set_design		set_design_top
identify_power_logic	pgpins_naming		set_instance		set_scope
	powerswitch		Design - modes		
	retencell		create_mode_transition		add_pst_state
Design - supplies			create_power_mode		create_pst
create_bias_net	supply	create_supply_net	update_power_mode		
create_power_nets			Multimode analysis		
create_ground_nets			create_analysis_view		
Design - domains			create_nominal_condition		
create_power_domain	voltageDomain	add_domain_elements	create_operating_comer		
update_power_domain	pinvoltage	create_power_domain	set_switching_activity		
		merge_power_domains	update_nominal_condition		
		set_domain_supply_net	Simulation semantics		
Design - levelshifters					bind_checker
create_level_shifter_rule	levelshifter	map_level_shifter_cell			create_hdl2upf_vct
update_level_shifter_rules		set_level_shifter			create_upf2hdl_vct
Design - retention cells			Miscellaneous		
create_state_retention_rule		map_retention_cell	create_global_connection		add_port_state
update_state_retention_rules		set_retention	define_library_set		connect_supply_net
		set_retention_control	set_array_naming_style		create_supply_port
Design - isolation logic			set_cpf_version		get_supply_net
create_isolation_rule	ignorepdcrossing	map_isolation_cell	set_hierarchy_separator		name_format
update_isolation_rules		set_isolation	set_power_target		save_upf
		set_isolation_control	set_power_unit		upf_version
			set_register_naming_style		
			set_time_unit		



UPF Support in SpyGlass Power



The screenshot displays the SpyGlass Desktop interface. The main window shows a Verilog module named `simple1` with inputs `a`, `b`, `VDD1`, `VDD2`, and `GND`. It includes level shifters `LS21` and `LS12`, and a block `ua`. The message tree below the code shows two warnings: `lowpower[2]` (WARNING -> 2) and `spyglass[1]` (INFO -> 1). The `spyglass[1]` message is expanded to show the warning details.

The translated command line window shows the following text:

```
Current_design simple1
supply -name VDD1 -alwayson 1 -value 1.0
supply -name VDD2 -alwayson 1 -value 2.0
voltage_domain -name Vtop -modname simple1 -value 2.0 \
  -supplyname VDD2
voltage_domain -name VA -instname simple1.ua -value 1.0 \
  -supplyname VDD1

levelshifter -name LS12 -from VA -to Vtop \
simple1gate.sgdc_from_upf 1,1 Top
set_design_top simple1

# Logical information
create_power_domain Vtop -elements simple1
create_power_domain VA -elements simple1.ua
set_level_shifter A_to_top -domain VA -applies_to outputs
set_level_shifter A_to_top -domain Vtop -applies_to inputs
set_level_shifter top_to_A -domain Vtop -applies_to outputs
set_level_shifter top_to_A -domain VA -applies_to inputs

# Physical information
create_supply_net VDD1
create_supply_net VDD2
set_domain_supply_net Vtop -primary power net VDD2
simple1gate.upf 1,1 Top
```

An arrow points from the text "Translation command line" to the highlighted line in the translated command line window.

Agenda

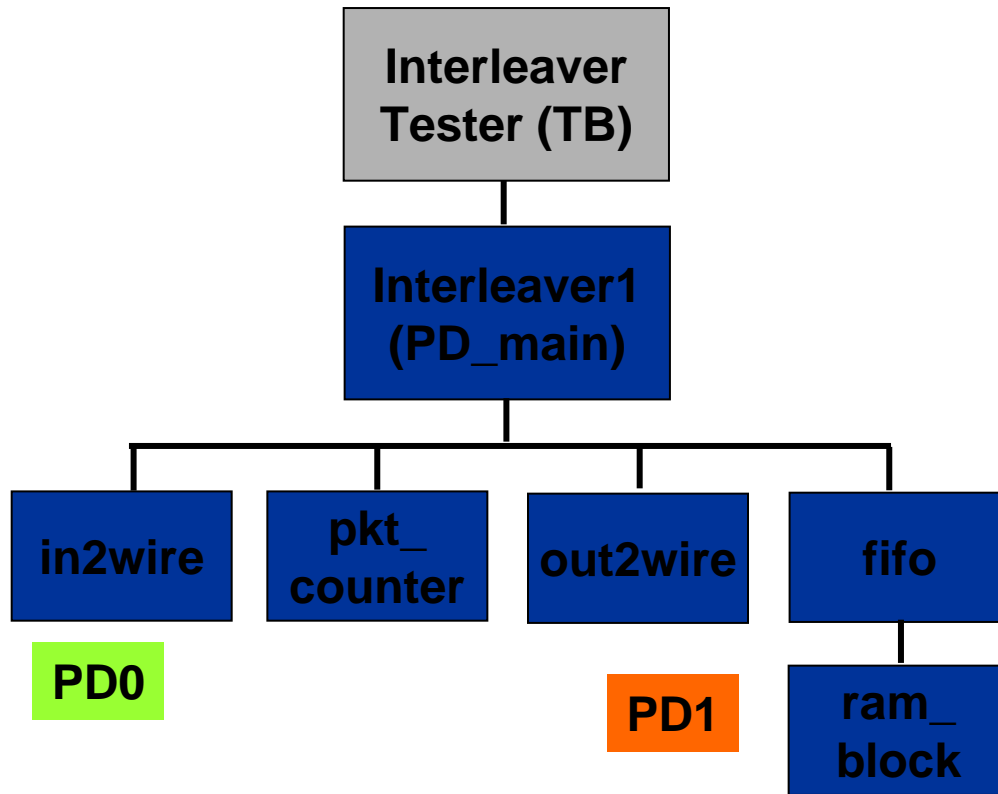


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- Power Intent Checking (00:15)
 - Piyush Sancheti, Atrenta
- Q & A

Interleaver UPF Demo



Logic Hierarchy View



Floorplan View

