



Low-Power Coalition

***Industry Commitment to Successful Adoption of Low-Power
Design Flows***

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Innovation Through Collaboration



Executive Summary

- **Design tool flows need enhanced low-power capabilities**
 - ◆ Current flows highly fragmented
- **Standards for interoperable low-power flows urgently required**
- **Several, recently emerged efforts need unification and focus on removing adoption barriers**
- **Industry mandate for new Low-Power Coalition to ensure:**
 - ◆ Consistency across: Multiple vendors, digital and analog flows, & abstraction levels
 - ◆ All interested parties come together under a neutral organization with anti-trust protection, and trusted open processes for decision-making, conflict resolution, etc.
 - ◆ Fairness in membership, voting rights, and shared control of standards
 - ◆ Collaboration and synergy with related efforts and groups
 - ◆ Maximize opportunity for convergence in low-power standards

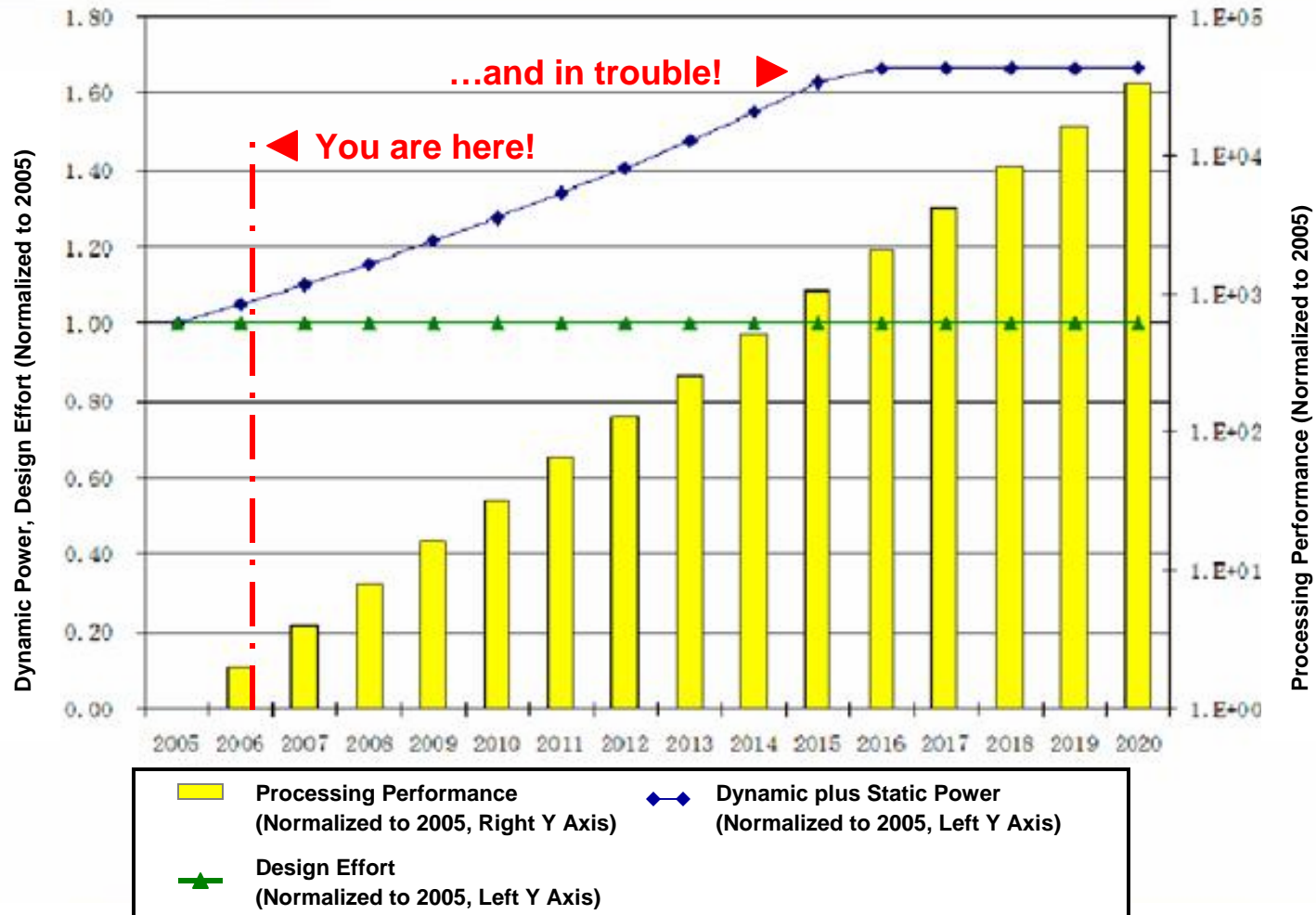


Problem Statement

- **Design tool flows need enhanced capabilities for managing low-power chip design requirements**
 - ◆ Specification of low-power design intent
 - ◆ Architectural tradeoffs
 - ◆ Logic implementation
 - ◆ Physical implementation
 - ◆ Design verification
 - ◆ Testability
- **Existing piecewise solutions and workarounds highly fragmented**
 - ◆ Cumbersome across multi-vendor flows
 - ◆ Excessive and error-prone, costly re-entry



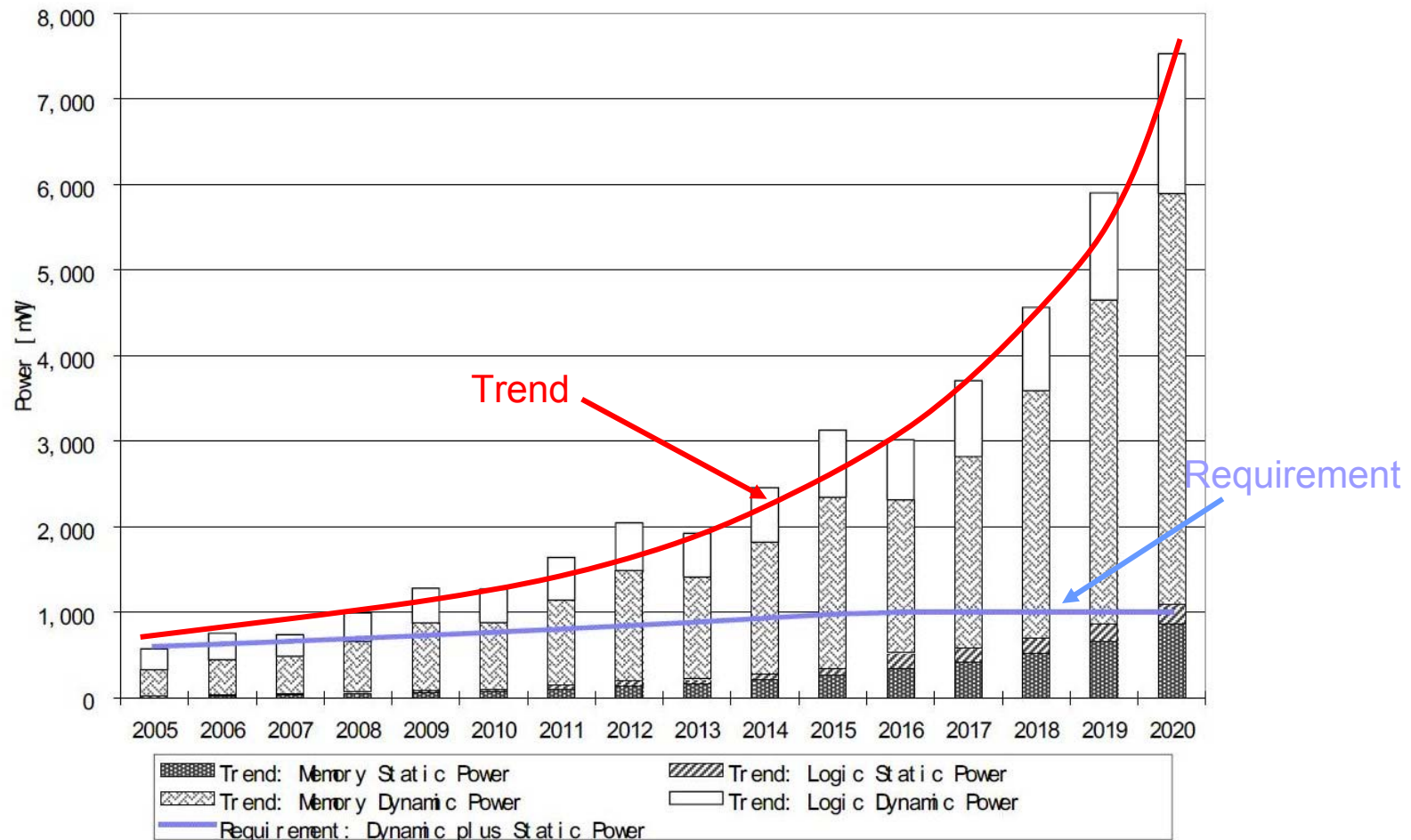
Power Hits the Ceiling!



Source: ITRS 2005 Power Consumption Trends for SoC-PE



Low-Power Design Is Now Critical



Source: ITRS 2005 Power Consumption Trends for SoC-PE



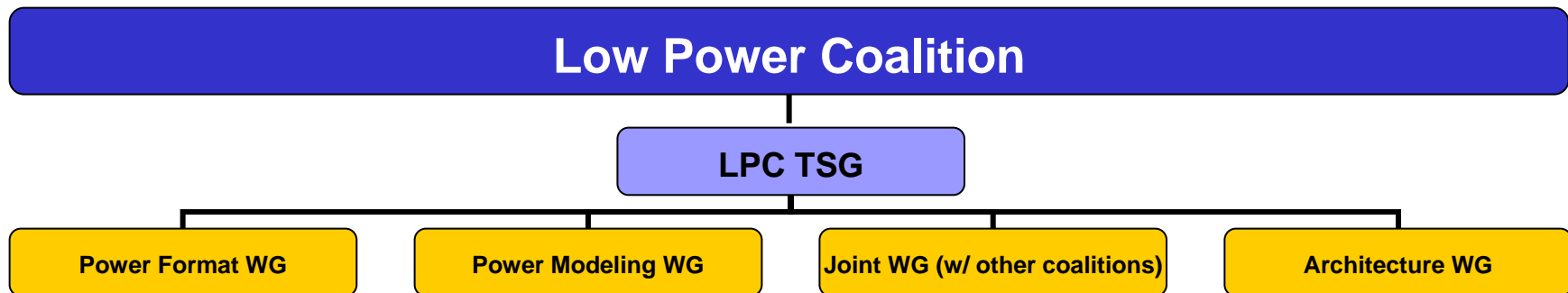
What Is The Low-Power Coalition?

- **User-centric and comprehensive**

- ◆ Focused on user needs for successful adoption into production chip design flows
- ◆ Owns roadmap requirements and priorities defined by members (users, EDA partners)
- ◆ Industry alignment & outreach via books, training, software, conferences, articles, etc
- ◆ Broad industry participation with founding members: AMD, Apache, Atrenta, Azuro, Cadence, ChipVision, Intel, LSI, Magma, NXP (formerly Philips Semiconductor), Sequence, ST Microelectronics, TI, ... (stay tuned for others to come)

- **Flow-based**

- ◆ Standards to promote integration of open technologies (formats) into cohesive flows
 - CPF spec. (read-only) available to LPC, derivative works rights starting 02/01/2007
- ◆ Analyze / develop semantic consistency across data exchanges
- ◆ Synergy with other Si2 groups – OAC, OMC, Liberty TAB
- ◆ Partnerships with other standards organizations (Accellera, SPIRIT, VSIA,...)



Technical Steering Group (TSG)

Structure

- 12 members, with 75% super-majority vote to approve standards, guidelines or specs
- Initial three Architect model
- Transition to Chair/Vice Chair elected for 1-year terms

Responsibilities

- Drive / own roadmap and deliverables
- Define problems to be solve
- Start, manage, and end working groups
- “Champions” to serve as liaisons to working groups

Working Groups

Created and disbanded by TSG

- Champion from TSG is a member
- WG participants are from coalition
- Chairperson is appointed by TSG

Proposed/potential initial list of WG’s

- CPF WG
- Power Modeling WG
- Joint WG a la JDM WG
- Architecture WG

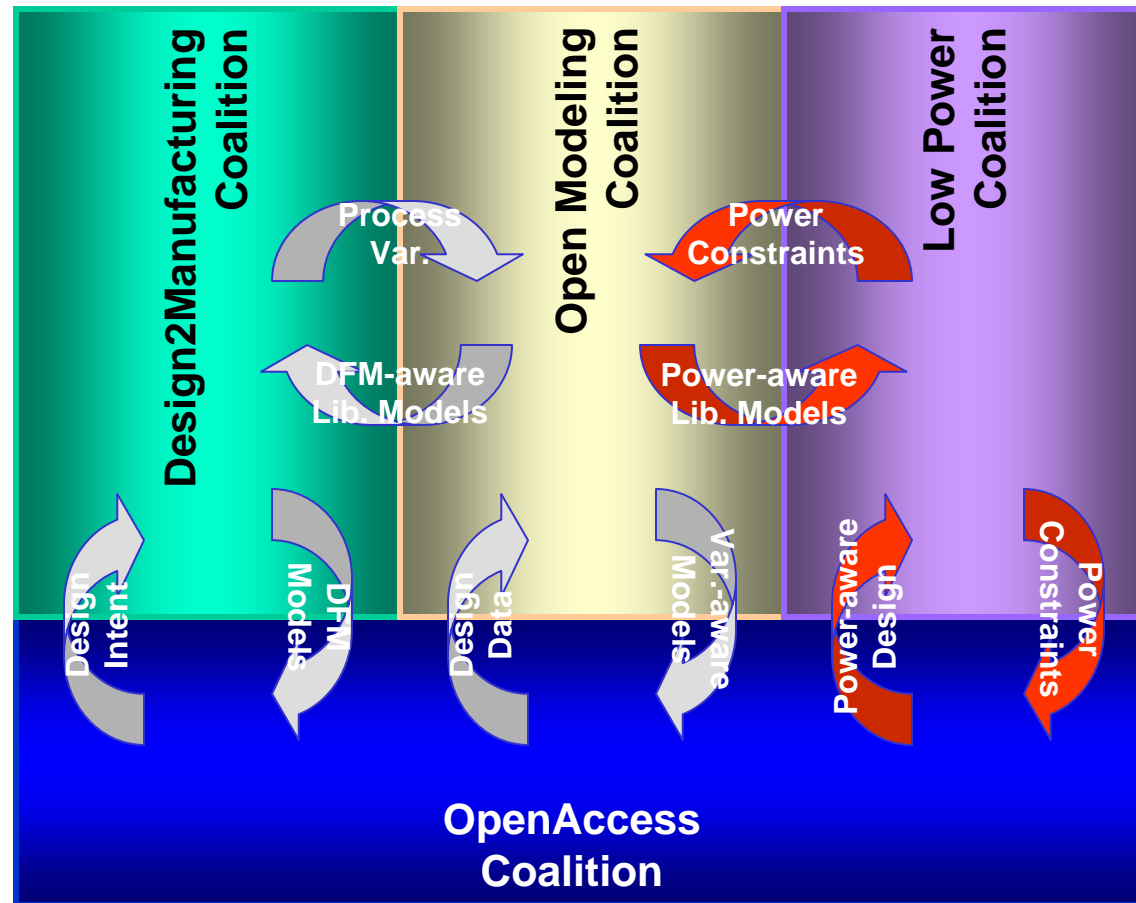


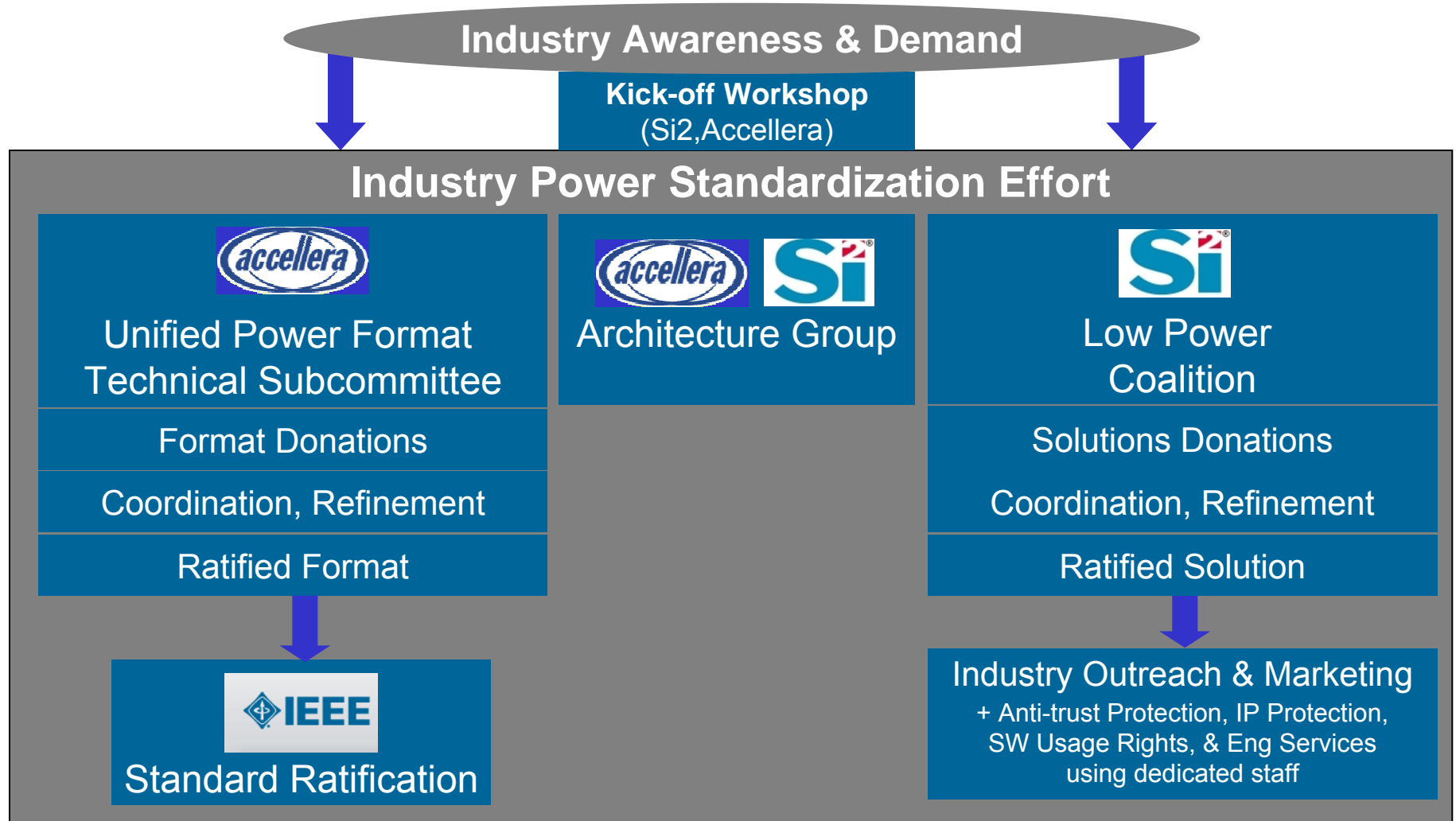
Si2 / LPC Openness Criteria

- **Rights of IP not accepted into standard revert to contributor**
- **Si2 standards resulting from IP contributions must satisfy the following minimum requirements:**
 - ◆ Si2 granted perpetual, worldwide, fully paid-up, exclusive rights to license, and create derivative works of, the contributed IP within the standard's specified field of use
 - ◆ Si2 must be able to license / sub-license contributed IP, and all derivative works, under non-discriminatory terms in accordance with Si2 Bylaws
 - ◆ Any relevant patents, or pending patents, found in the IP must be licensed to all members and Si2 under RAND terms, and must also permit RAND licensing to non-members if approved as an Si2 standard




LPC – Synergy with Other Si2 Coalitions







Immediate Next Steps

- **Conduct first coalition meeting** 11/08/2006 
 - ◆ Appoint / elect leaders, start TSG
- **Get the coalition rolling:**
 - ◆ Member companies appoint representatives: 11/2006
 - ◆ LPC-TSG defines and starts WG's 11/2006
 - ◆ Members engage CPF 11/2006
 - Download CPF, read and discuss CPF & derivative works
 - ◆ Define short-term roadmap 1Q2007
 - Begin derivative works with CPF
 - Identify means to align to a single standard
 - ◆ Hold first LPC election 01-02/2007
 - ◆ Define long-term roadmap 2-3Q2007

- **The industry's new Low-Power Coalition is here:**
 - ◆ User-centric, Flow-based, Comprehensive and Focused on rapid, sustainable adoption
 - ◆ Leverages existing work that can meet Si2 / LPC openness criteria
 - CPF specification (read-only) available **NOW**
 - CPF derivative works rights starting 02/01/2007
 - Alignment with Accellera to drive single standard
 - ◆ 13 current members,... with more on the way



Moving Forward!

- Your support of the LPC is critical to achieving convergence success!
- For more information, visit: www.si2.org
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