



# Update on Accellera Unified Power Format Standardization Initiative

Presented by Jim Sproch  
At the EDA Interoperability Developer's Forum  
November 9, 2006

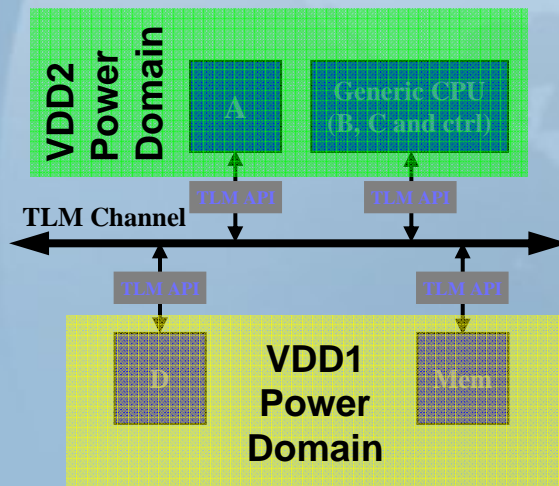
# Industry Need

- Power is a dominant design factor
  - Wireless mobility is the way to go
  - Even non-portable products face power constraints
    - Heat generation and dissipation
    - Practical power supply & management
- Designers use a variety of power management tools
  - Commercial and captive suppliers
    - Looking for enhanced interoperability
  - Specification of power aware design characteristics
    - Need to specify power intent earlier in design cycle
  - Verification tools often assume power distribution
    - Need to explicitly verify correctness of power-aware functionality



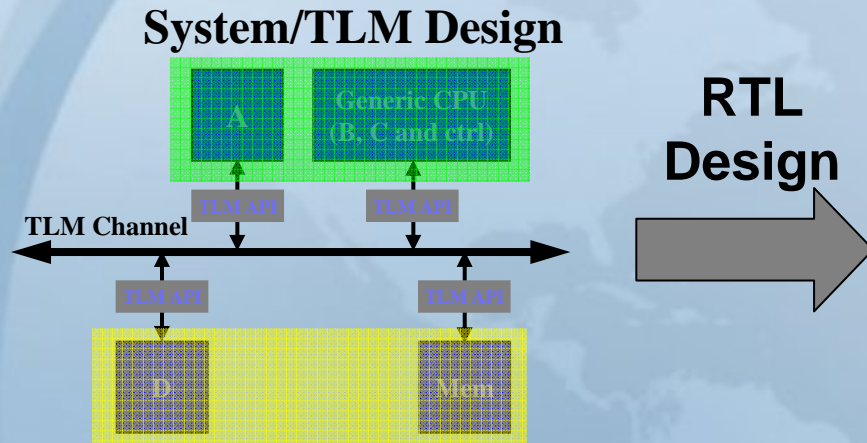
# Low Power Design Overview

## System/TLM Design

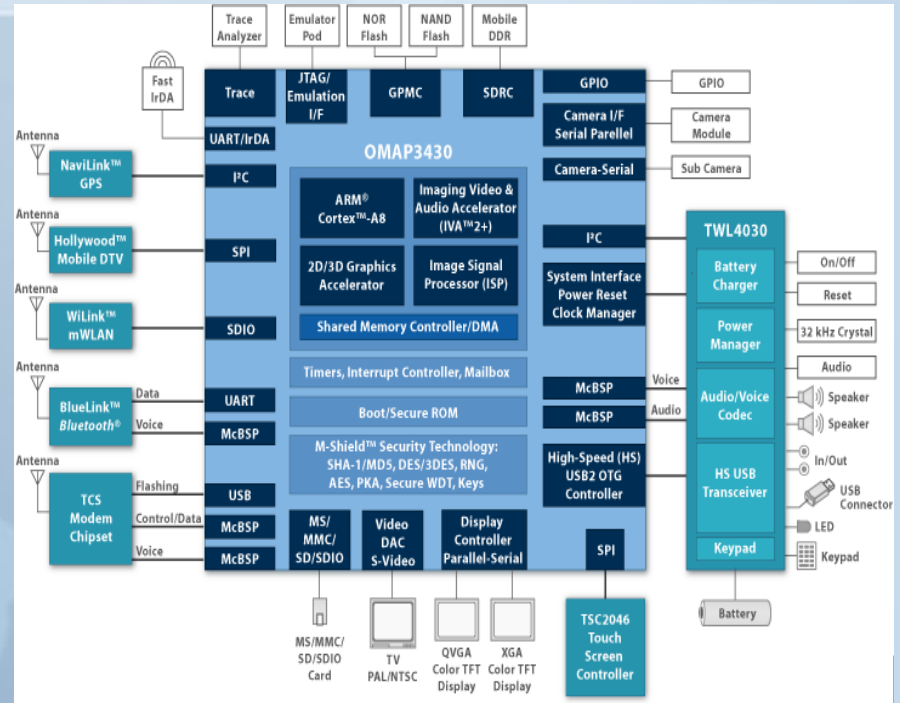


- At System/TLM level:
  - Explore power domain partitions
  - Budget dynamic power
  - Estimate dynamic power usage
  - Power management strategy
- Standardization areas:
  - Save and restore state information
  - Set operating voltages
  - Power aware design, verification & analysis

# Low Power Design Overview (2)



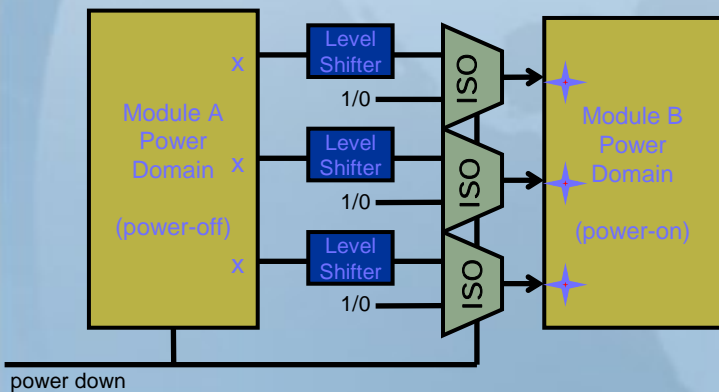
- Power-aware design elements
  - Power distribution network
  - Switches, regulators, controllers
  - Isolation, level shifters
  - State retention
  - di/dt constraints
- Power-aware design process
  - Specification of power intent
  - Functional verification
  - Constraint-driven synthesis
  - Power-aware simulation
  - Dynamic power estimation and analysis



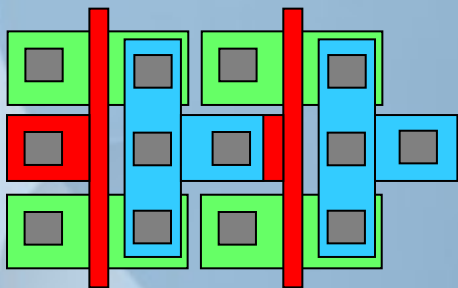


# Low Power Design Overview (4)

## Gate Implementation



- Gate implementation
  - Netlist with power, ground
  - Power behavior
    - Gate sims match verified RTL
  - Equivalence checking RTL v. Gate
  - Confirm constraints
  - Dynamic power calculation



- Physical implementation & verification
  - Power distribution connectivity
  - Voltage level compatibility
  - Static power consumption



# Accellera Unified Power Format TSC Mission Statement

- Rapid development of an open, comprehensive standard for the specification of power-aware requirements and design intent as well as implementation, verification and analysis across all design abstraction levels.

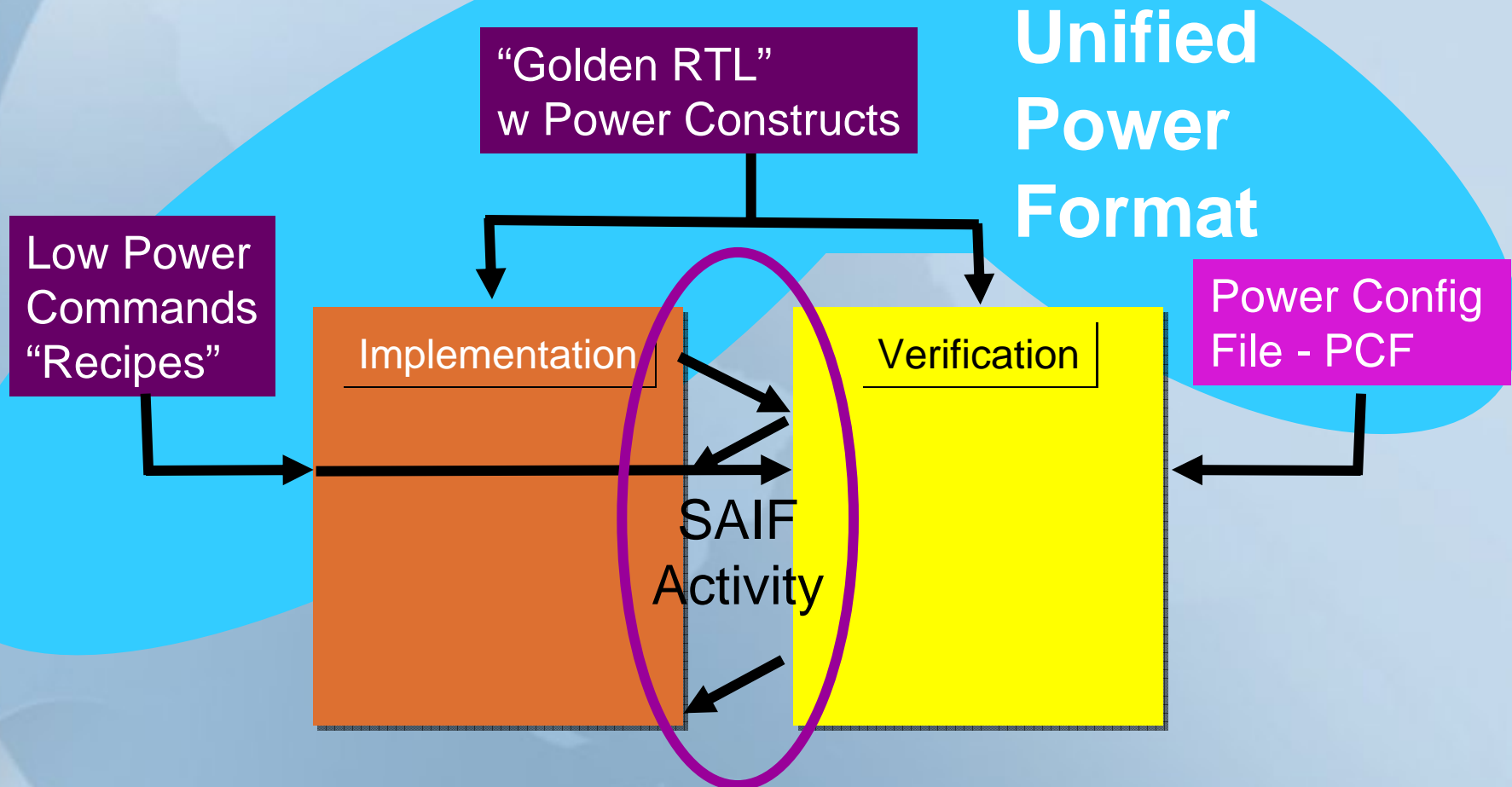


# Scope of UPF TSC

- Abstraction levels
  - Phase 1: RTL2GDSII
  - Phase 2: System TLM, behavioral/algorithmic
- Specification
  - Design requirements
  - Design constraints (hard and soft)
- Implementation
  - Power distribution network
  - Intended power-aware functional behavior (e.g., retention)
- Verification
  - Power-off corruption semantics
  - Retention behavior
- Analysis
  - Estimation / calculation of static & dynamic power



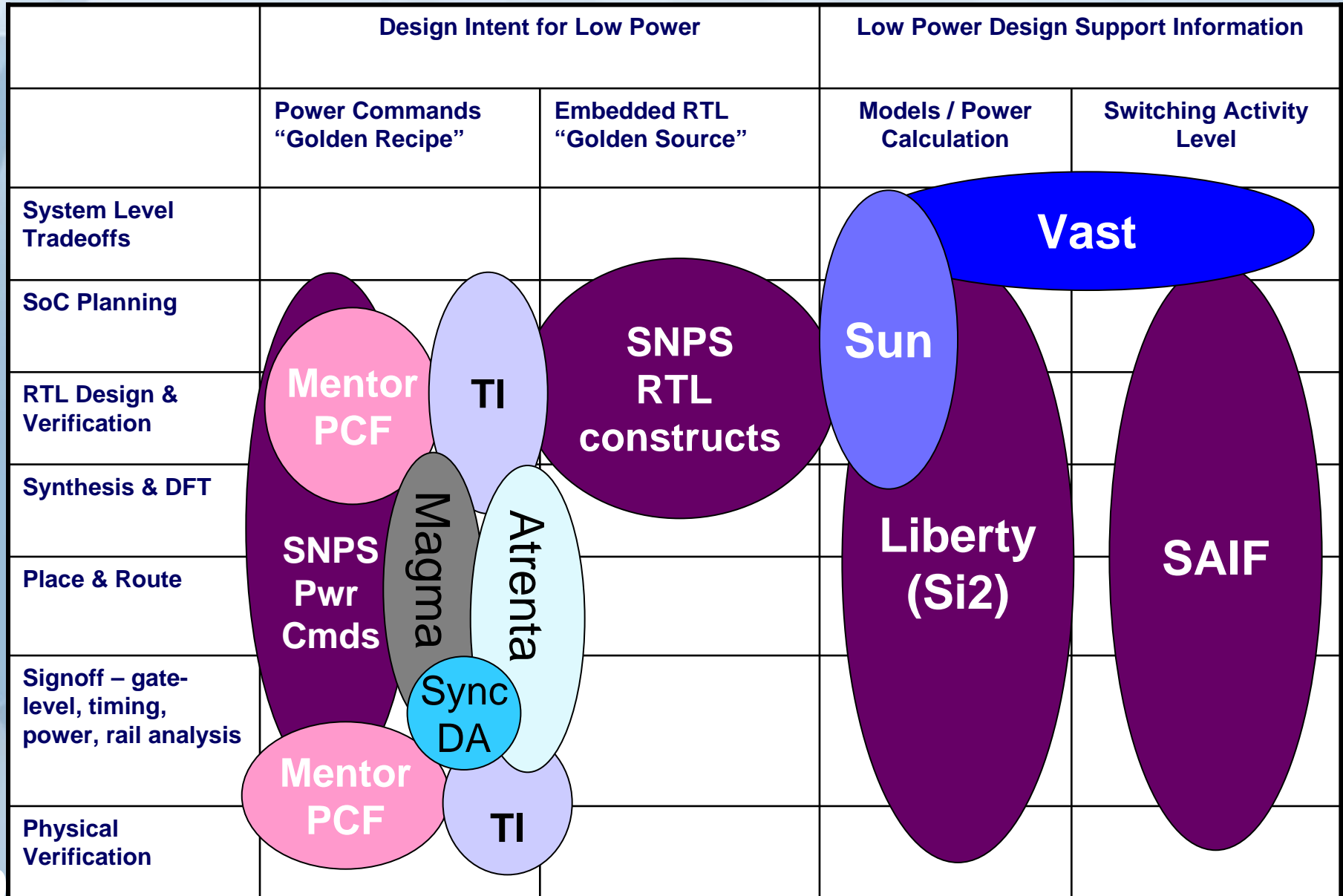
# Low Power Methodologies



Design engineers want "all of the above" !



# UPF Technology Donations



# UPF Accomplishments

- **Accellera Unified Power Format Technical Sub-Committee formation**
- **Accellera/Si2 Sponsored Workshop**
- **Design Objectives Document published**
- **Numerous donations accepted**
- **Productive technical working sessions**
- **Weekly meetings underway**



# Status

- Preliminary architecture defined
- Semantics established
  - Power domains
  - Isolation
  - Level-shifting
  - Retention
- Command syntax outlined
- Incorporating user feedback
- Upcoming working sessions in Dallas and Munich

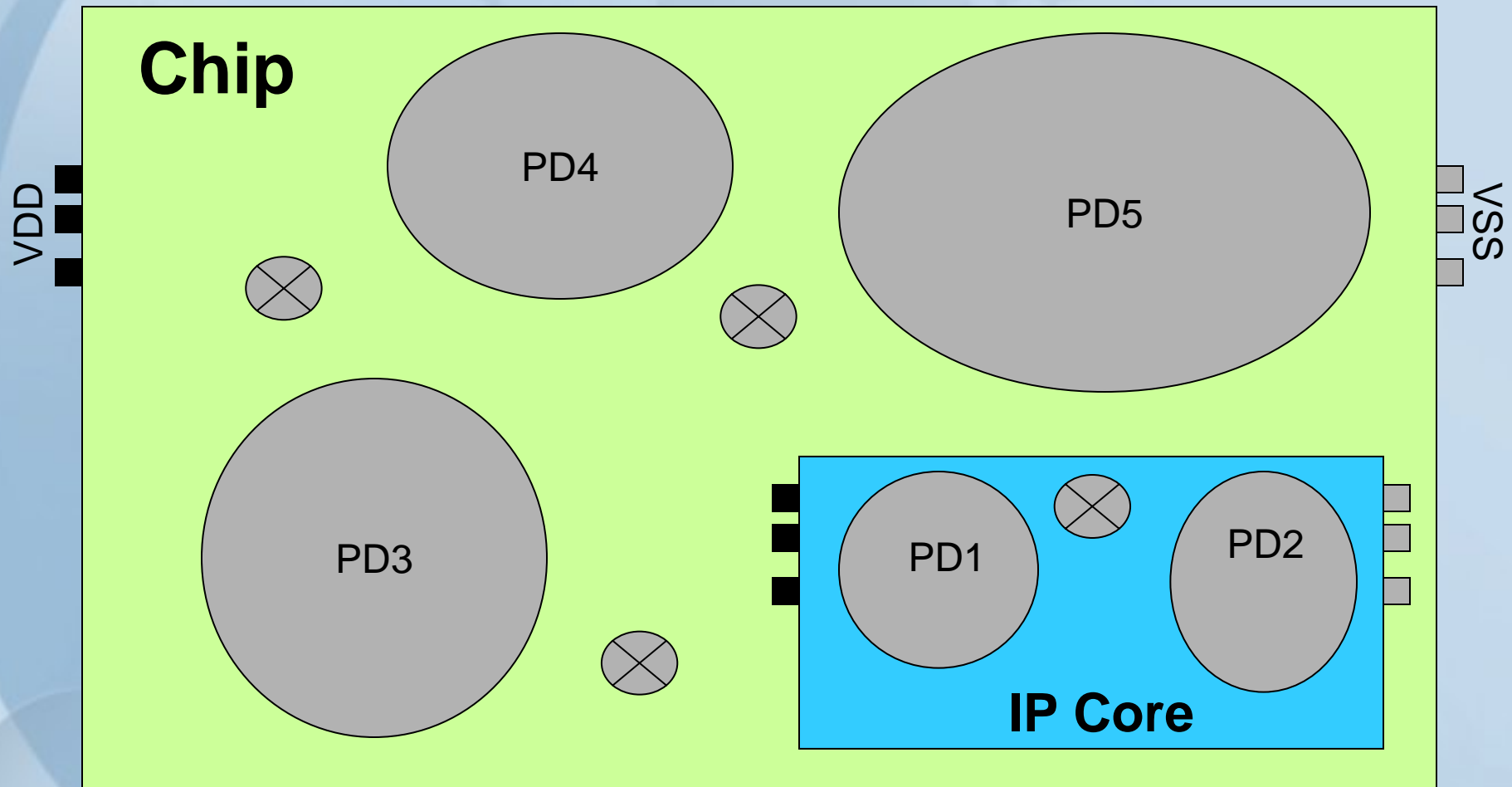


# Upcoming Milestones

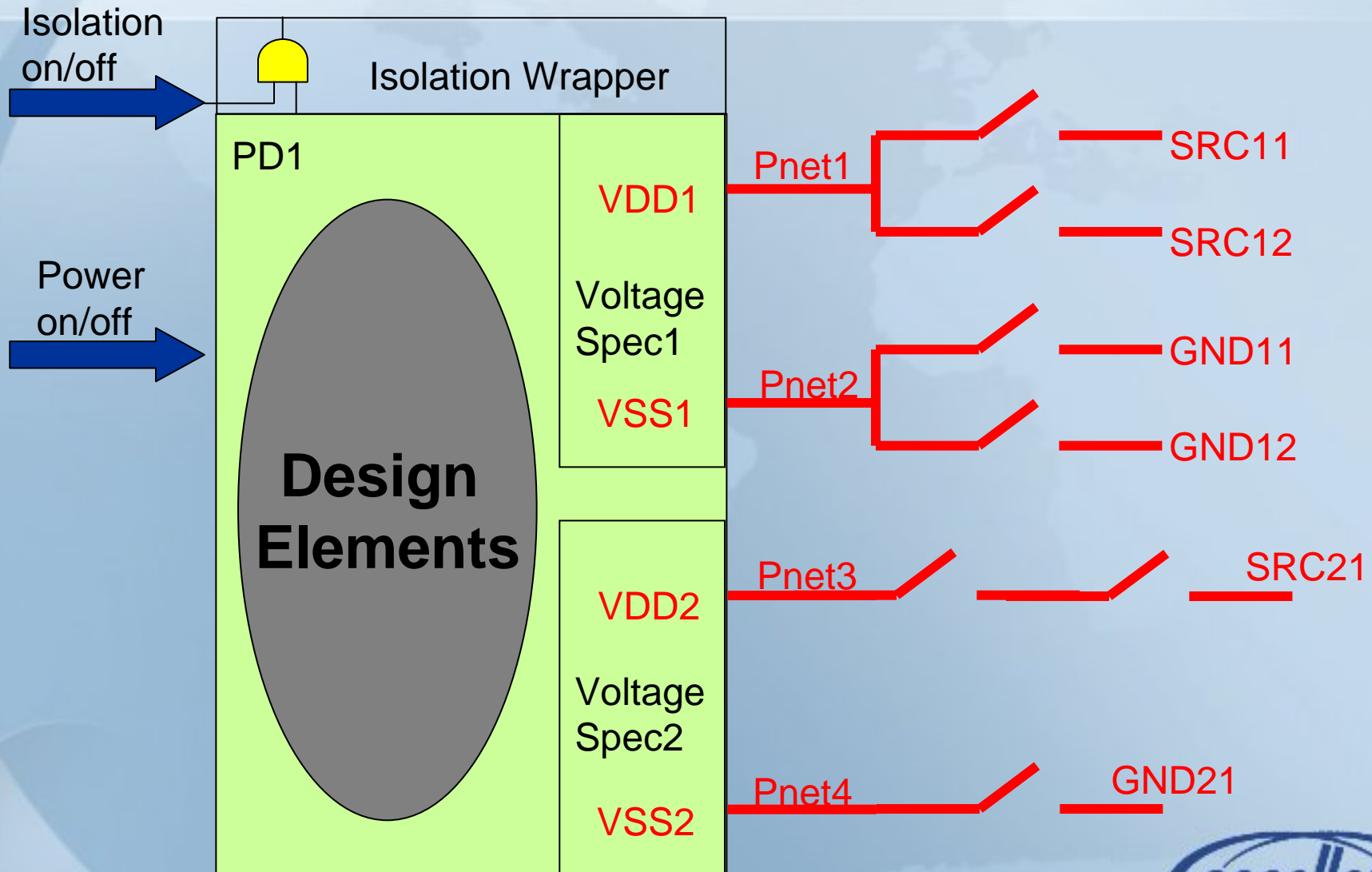
- **Draft Unified Power Format proposal**
- **Circulate draft document for review**
- **Submission to Accellera Board for approval**
- **Hand-off to IEEE in January 2007**



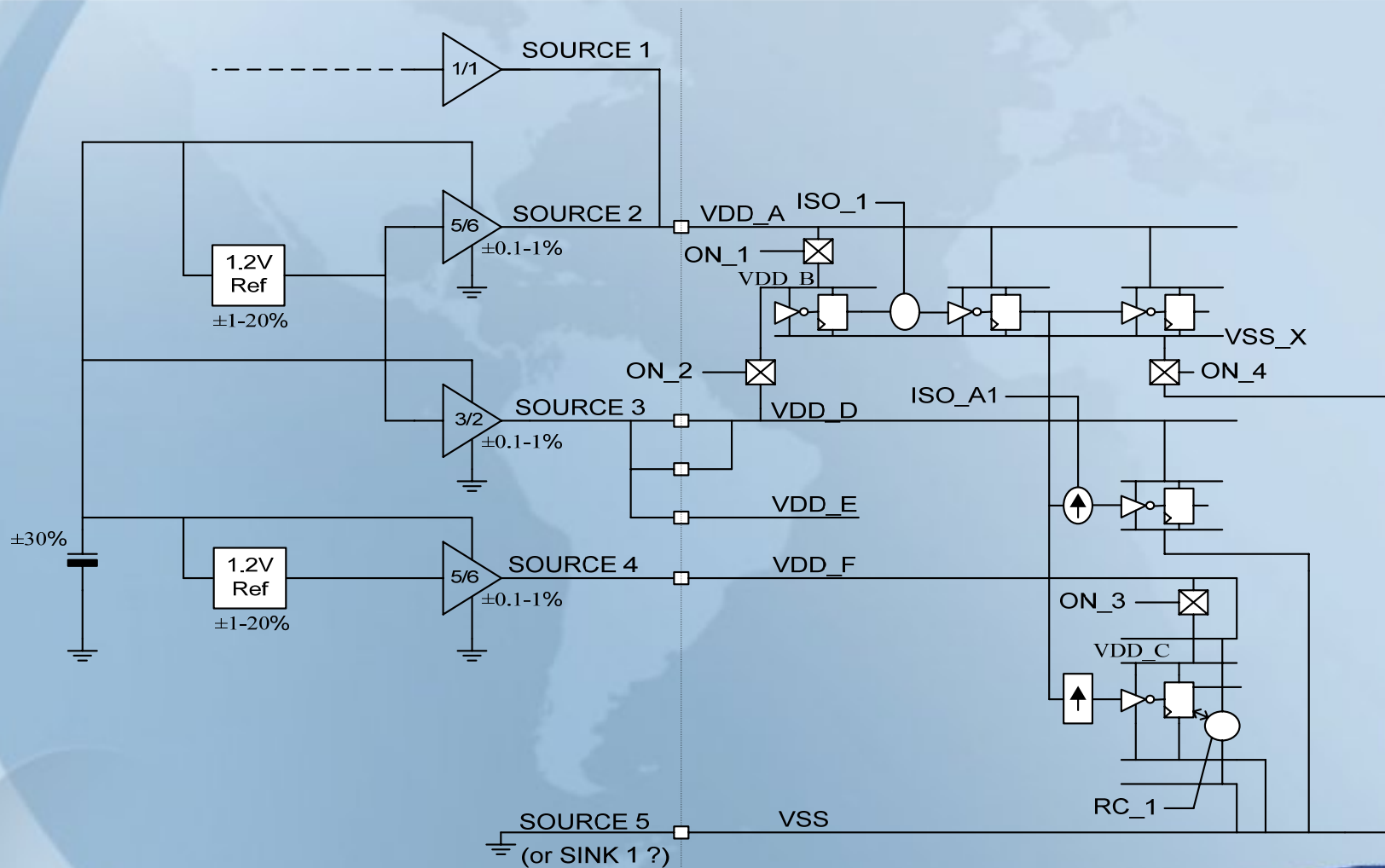
# Logic & Physical Power Domains



# Multi-Supply Power Domain



# Conceptual Schematic



# Do you care about power?

- If Power Management Standards are important to you...
  - Check out the Accellera website  
**[www.Accellera.org](http://www.Accellera.org)**
  - Follow the link under Technical Activities to Unified Power Format

