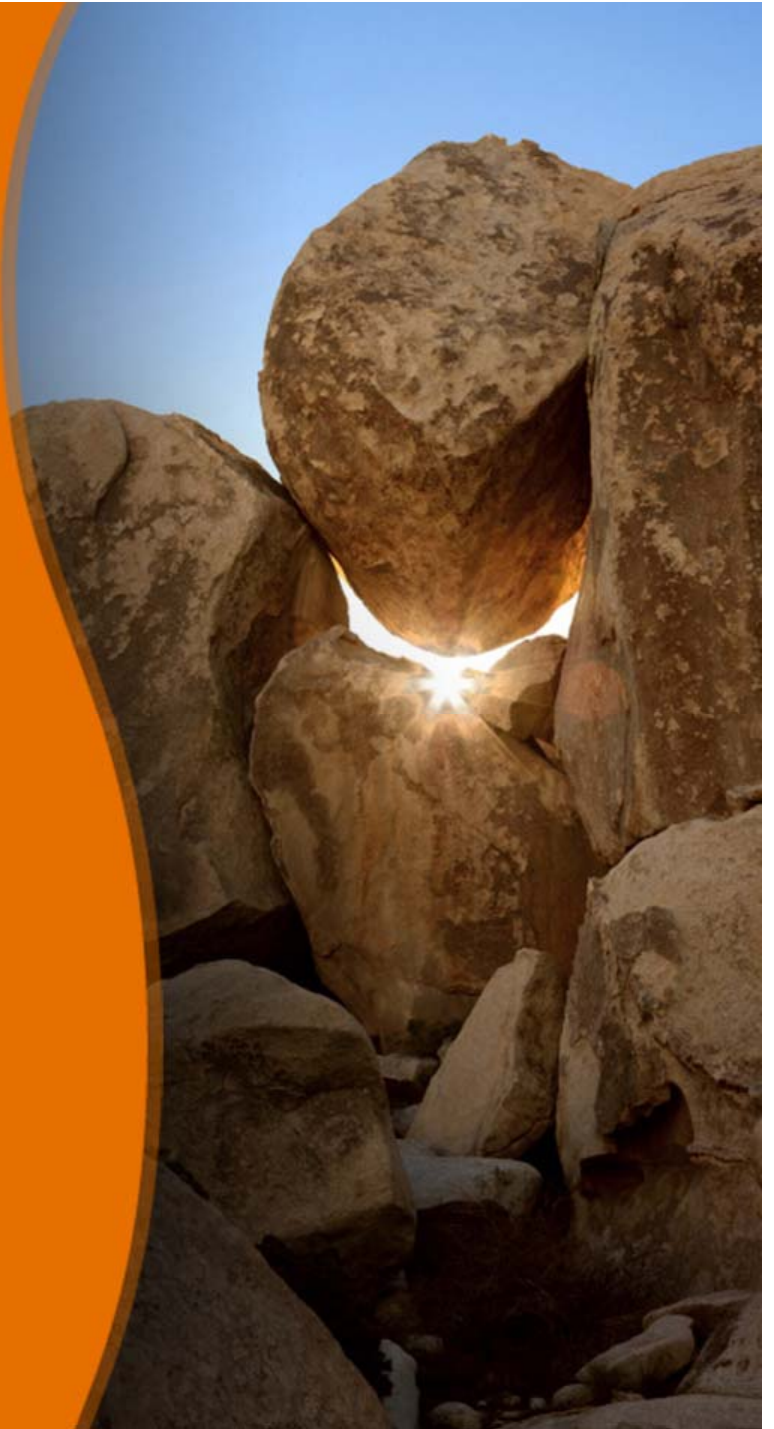


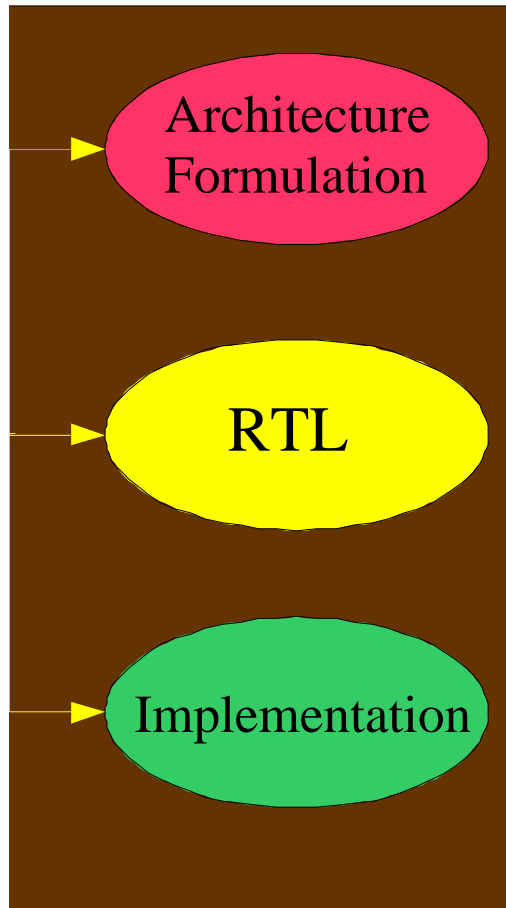


# Power @ Sun

Rob Mains  
Senior Distinguished  
Engineer  
Systems Group  
Sun Microsystems  
11/9/06

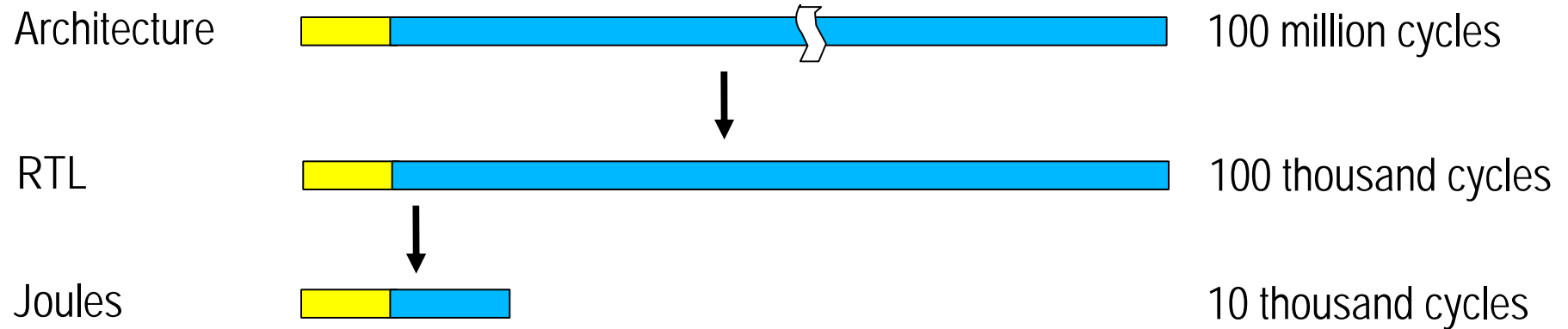


# Divining Accurate Power throughout the Design Process



- Ad hoc at best
  - > Formerly a afterthought
- Power budgeting & prediction
  - > Similar to the timing problem
  - > How to predict during architecture & maintain?
    - > Feedback throughout design process
    - > Correlation of architecture models to real stuff
  - > Power Grid Design
  - > Optimization
    - > What-if tradeoffs?
      - Architecture
      - RTL
      - Gates/Circuits
- Need a unified approach

# Predicting Power: Good Power Diags



 Initialization codes

 Testbench execution (power analysis is only meaningful during this period)

- Isolation of realistic power diagnostics tough
- Need to run multiple, different variety of diags to get good average power
- Further work needed to predict & isolate: statistical approach?

# Can EDA tools handle the challenge?

- IP Reuse
- Power grid design with multiple voltage domains
- Multiple operational voltages for circuits
- Clock design for skew & power
- Custom circuit configurations for leakage control
- Optimization
  - > Repeater planning
  - > Selective back biasing
  - > Vt adjustment
- *How do we consistently handle power in design methodology & tools?*

# Why a unified power standard?

- Want one format digestible by any vendor
  - > Need to assess & access best of breed tools
  - > Want usable for design: tradeoffs at architecture, rtl, circuit, and gate level
  - > Needs to be robust enough for optimization & process variation modelling
- Need format that works at all levels of the design process
  - > Need to be able to provide feedback mechanisms to improve accuracy of models
    - > Architecture, RTL, gates, circuits, integration & silicon

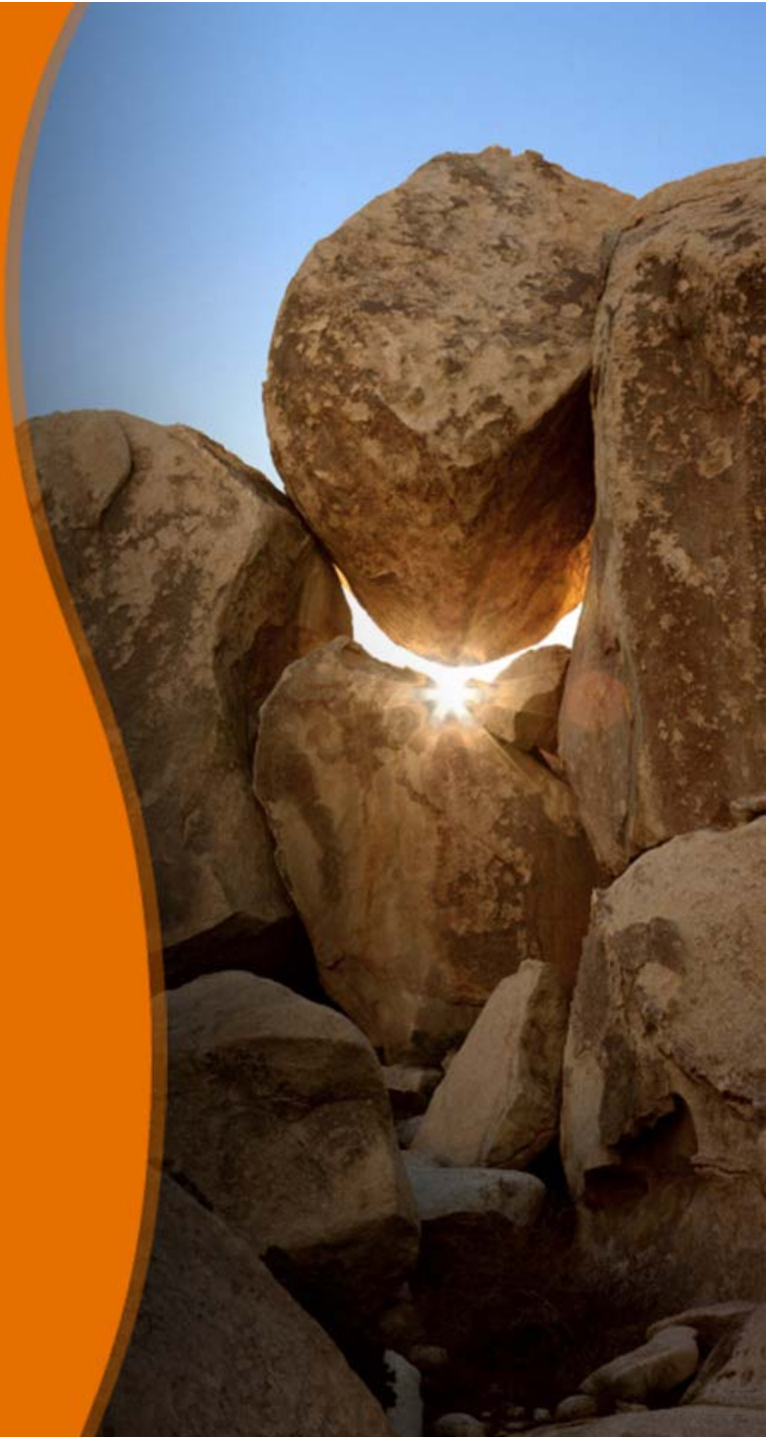
# How is Sun Participating?

- We donated our building for this meeting!
- Donation of Sun's Power abstract for cell modelling
- IP Disclosure of Sun's Internal Power Analysis tool: Joules
- Member of the Low Power Coalition
- Need all major EDA players to participate



# Power @ Sun

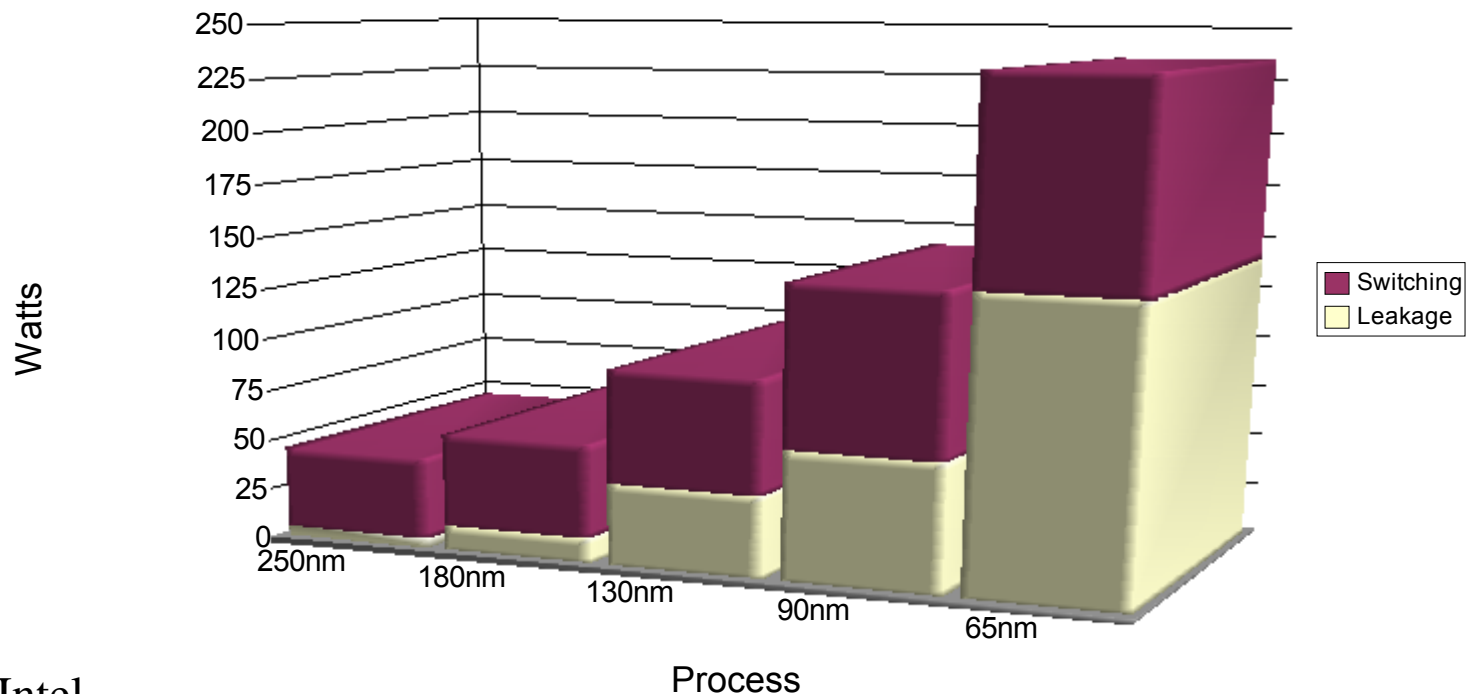
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# Trends in Chip Power

- Chip power consumption is increasing as the transistor count and frequency increase
- Leakage power will soon dominate the total power

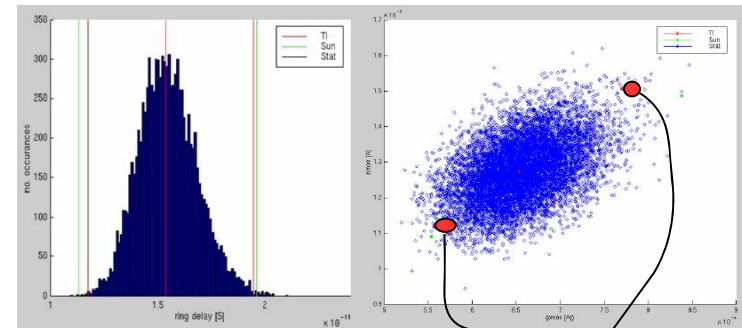
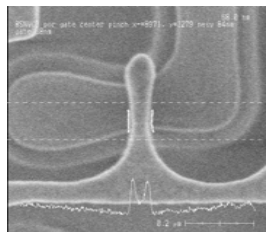
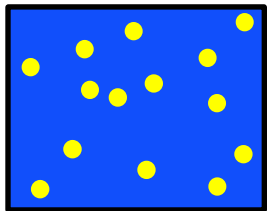
Processor Power Consumption



Source: Intel

# Process & Environment Variations

- Process change & drift
- Systematic variations
- Random variations
- Voltage & temperature



Corner Models

- Abstracted to 2, 4 or more process corners
  - > FF & SS corners in Ckt simulation
  - > min/max power models
- Are corner models sufficient going forward?
  - > Either too pessimistic or optimistic