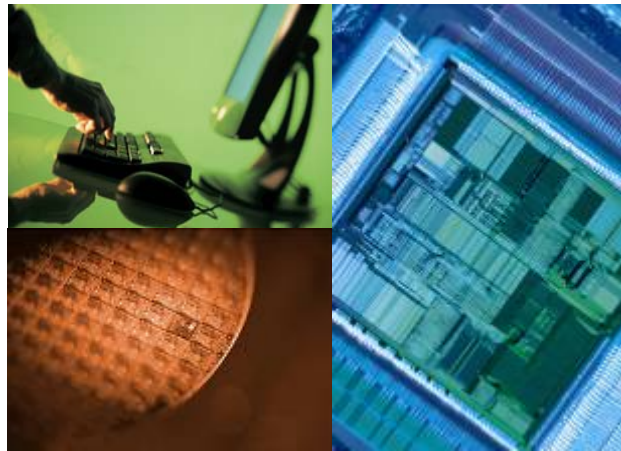


Synopsys SystemVerilog and VMM Methodology Update

Tom Borgstrom
Director, Marketing
Synopsys Verification Group



SystemVerilog – A Vision Delivered

A vision of unified design and verification ...

... for higher productivity ...

... as an industry standard ...

... with broad vendor support ...

... throughout the design flow.

SystemVerilog: Unifying Design and Verification

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SystemVerilog Increases Productivity

- Extends Verilog to Higher Abstraction
- 2-5x less code
- No change in synthesis flow

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SystemVerilog is an IEEE Standard

IEEE APPROVES SYSTEMVERILOG® and VERILOG® STANDARDS FOR ELECTRONIC DESIGN

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70 SystemVerilog Catalyst Program Members

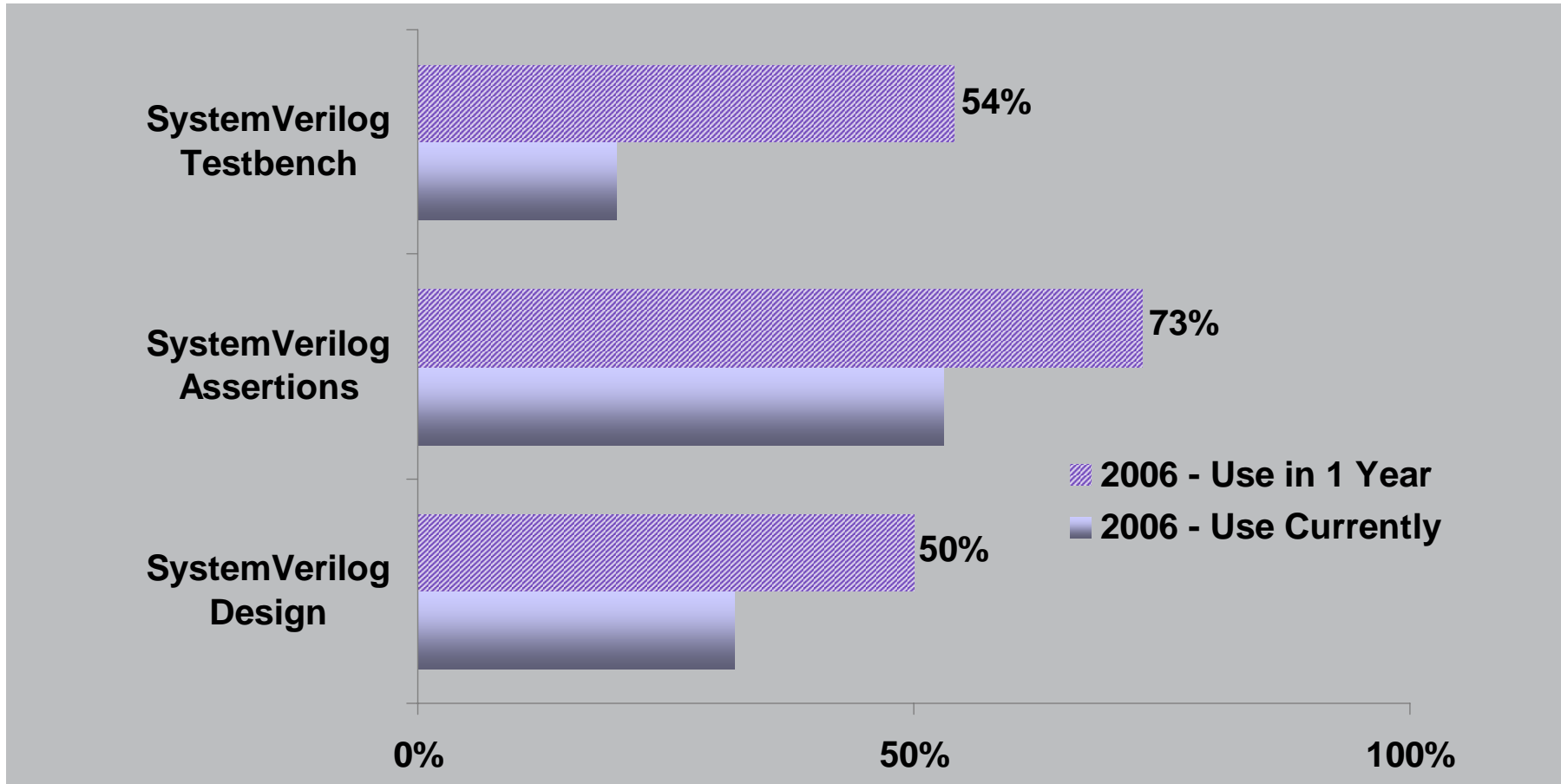
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First Complete SV Design & Verif. Flow

| Tool/Component | 2003.12 | 2004.12 | 2005.06 | Today |
|---------------------------------|---------|---------|---------|-------|
| VCS® RTL Design & Testbench | ✓ | ✓ | ✓ | ✓ |
| Pioneer-NTB Testbench Au | ✓ | ✓ | ✓ | ✓ |
| VCS Verification Library Verif. | ✓ | ✓ | ✓ | ✓ |
| Leda® Formal Equivalence | ✓ | ✓ | ✓ | ✓ |
| Magellan™ Formal Equivalence | ✓ | ✓ | ✓ | ✓ |
| Design Compiler® RTL Synthes | ✓ | ✓ | ✓ | ✓ |
| Formality® Formal Equivalence | ✓ | ✓ | ✓ | ✓ |

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Wide Adoption of SystemVerilog to Increase in 2007



Source: 2006 Worldwide SNUG Surveys

VMM Methodology for SystemVerilog



ARM®  **SYNOPSYS®**

- **VMM defines best verification practices**
 - Harnesses full power of SystemVerilog for higher verification productivity
 - Assertion-based, coverage-driven, constrained-random verification
 - ARM, Synopsys and over 30 contributors
- **Why a standard methodology?**
 - Avoid “re-inventing the wheel”
 - Enables easy cross-site collaboration, re-use
 - Foundation for future innovations
- **Vibrant VMM ecosystem**
 - 3rd party books, libraries, consultants, training
 - Expanding VMM user base, talent-pool

VMM Methodology User Success

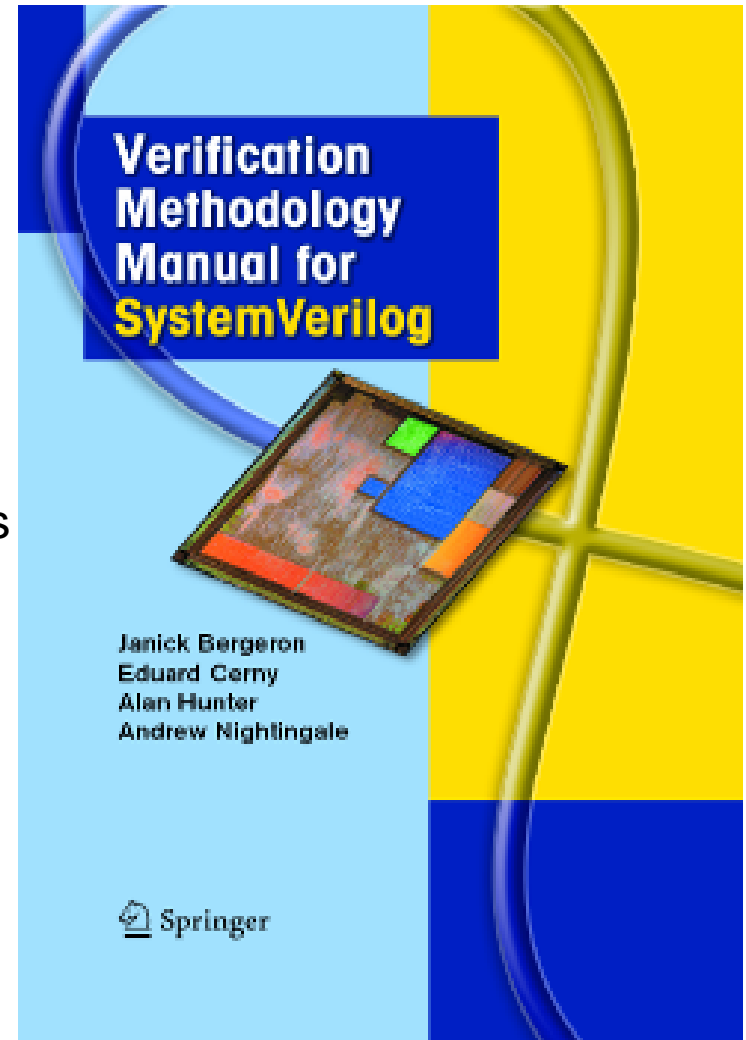


“Use of VMM and NTB saved four weeks on our project schedule.”

“Deciding to use the VMM was the best thing we could have done.”

VMM – An Open Approach

- **VMM Methodology**
 - Fully described in VMM book
 - Top-selling EDA book from Springer
- **VMM Standard Library**
 - Fully specified in VMM book
 - Speeds development of VMM testbenches
 - Implementation included with VCS
- **VMM Source Code Available**
 - For VCS customers & SystemVerilog Catalyst members
 - IEEE Std 1800-2005 compliant
 - Simple, no-charge license agreement



Google-Eye View of Methodology

November 8, 2006

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Standardizes on [Platform, Advanced ...](#)

converted their functional verification flow to SystemVerilog and AVM. This

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The methodology provides a common Universal Reuse Methodology (uRM) architecture that

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File Format: PDF/Adobe Acrobat

Used to model all transactors; built-in flow control for. starting, stopping and resetting transactors. • Fully documented in the SystemVerilog VMM ... [www.synopsys.com/partners/tapin/forumpres/oct2004/svf/04_Synopsys_SystemVerilogForum.pdf - Similar pages](#)

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http://www.synopsys.com/SystemVerilog/home.html

SystemVerilog Synopsys: The SystemVerilog Leader

TESTIMONIALS NEWS RESOURCES BOOKS

VERIFICATION
DESIGN

First Complete SystemVerilog Design and Verification Flow

ARCHITECTURE

VERIFICATION

- TRANSACTION-LEVEL MODELING & SIMULATION: VCS
- TESTBENCH AUTOMATION: VCS, PIONEER-NTB
- FUNCTIONAL COVERAGE: VCS, PIONEER-NTB
- VERIFICATION IP: VCS VERIFICATION LIBRARY
- DYNAMIC ASSERTION ANALYSIS: VCS, PIONEER-NTB
- RTL CHECKING: LEDA
- FORMAL AND HYBRID ASSERTION ANALYSIS: MAGELLAN
- RTL MODELING & SIMULATION: VCS

DESIGN

- DESIGN CHECKING: LEDA
- RTL SYNTHESIS: DESIGN COMPILER
- EQUIVALENCE CHECKING: FORMALITY

PLACE & ROUTE

Synopsys Complete SystemVerilog Flow

Complete SystemVerilog Flow
IEEE Std 1800™-2005 SystemVerilog is the industry's first unified hardware description and verification language (HDL/VL) standard. SystemVerilog is a major extension of the established Verilog language, and dramatically improves productivity in the development of large-gate-count, IP-based, bus-intensive chips. SystemVerilog is targeted primarily at the chip implementation and verification flow, with powerful links to the system-level design flow. SystemVerilog has been adopted by 100s of semiconductor design companies and supported by more than 75 EDA, IP and training solutions worldwide. Synopsys provides comprehensive support for SystemVerilog throughout its design and verification tool flow.

WHAT PEOPLE ARE SAYING

"After a detailed evaluation of available verification solutions, we chose to adopt Synopsys' VCS solution with its comprehensive support for industry-standard SystemVerilog testbench automation"
Hugues Deneux
General Manager
AMCC France

MORE TESTIMONIALS >

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www.synopsys.com/systemverilog

VMM Methodology

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http://www.vmm-sv.org/

Verification Methodology Manual for SystemVerilog

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What's Hot

- 2006
- 07/27 DAC SystemVerilog Testbench and VMM Workshop
- 05/01 SystemVerilog reference verification methodology: RTL
- 03/27 SystemVerilog reference verification methodology: Introduction
- 01/25 Leading Japanese Semiconductor Companies Endorse ARM-Synopsys VMM for SystemVerilog
- 2005
- 09/21 Springer Publishes the VMM
- 09/21 Source Code License for SystemVerilog

The VMM for SystemVerilog is our recommended reference book to architect SystemVerilog verification environments. It defines the state-of-the-art for advanced, coverage-driven functional verification that engineers can use to increase chip development productivity and quality, and will complement the IP Functional Verification Guide being developed by the STARC IP Reuse Engineering Group.

Yoshiharu Furui,
senior manager, IP Reuse Engineering Group STARC,
Japan

What People Are Saying >

Verification Methodology Manual for SystemVerilog

The *Verification Methodology Manual for SystemVerilog* is a blueprint for system-on-chip (SoC) verification success. The book documents advanced functional verification techniques used by industry experts to validate complex SoCs. It describes how to use the industry-standard SystemVerilog language to create comprehensive verification environments using coverage-driven, constrained-random and assertion-based techniques, and specifies verification library building blocks for interoperable verification components.

www.vmm-sv.org

SYNOPSIS
Predictable Success