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The SPIRIT Consortium: selections from a presentation to the Si2 Open Access Conference

Dr. Gary Delp, LSI Logic
10 November 2006

25
YEARS

Overview of The SPIRIT Consortium

Gary Delp, Technical Director
The SPIRIT Consortium





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Overview of The SPIRIT Consortium

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Presentation Structure

- Overview of The Consortium
- Technical Working Group Structure
- Roadmap and Futures
- IEEE Standardization Process
- Conclusions and Q&A

The SPIRIT Consortium Vision (2003)

- The SPIRIT Consortium was announced at DAC 2003
- The original vision upon which The Consortium was formed:

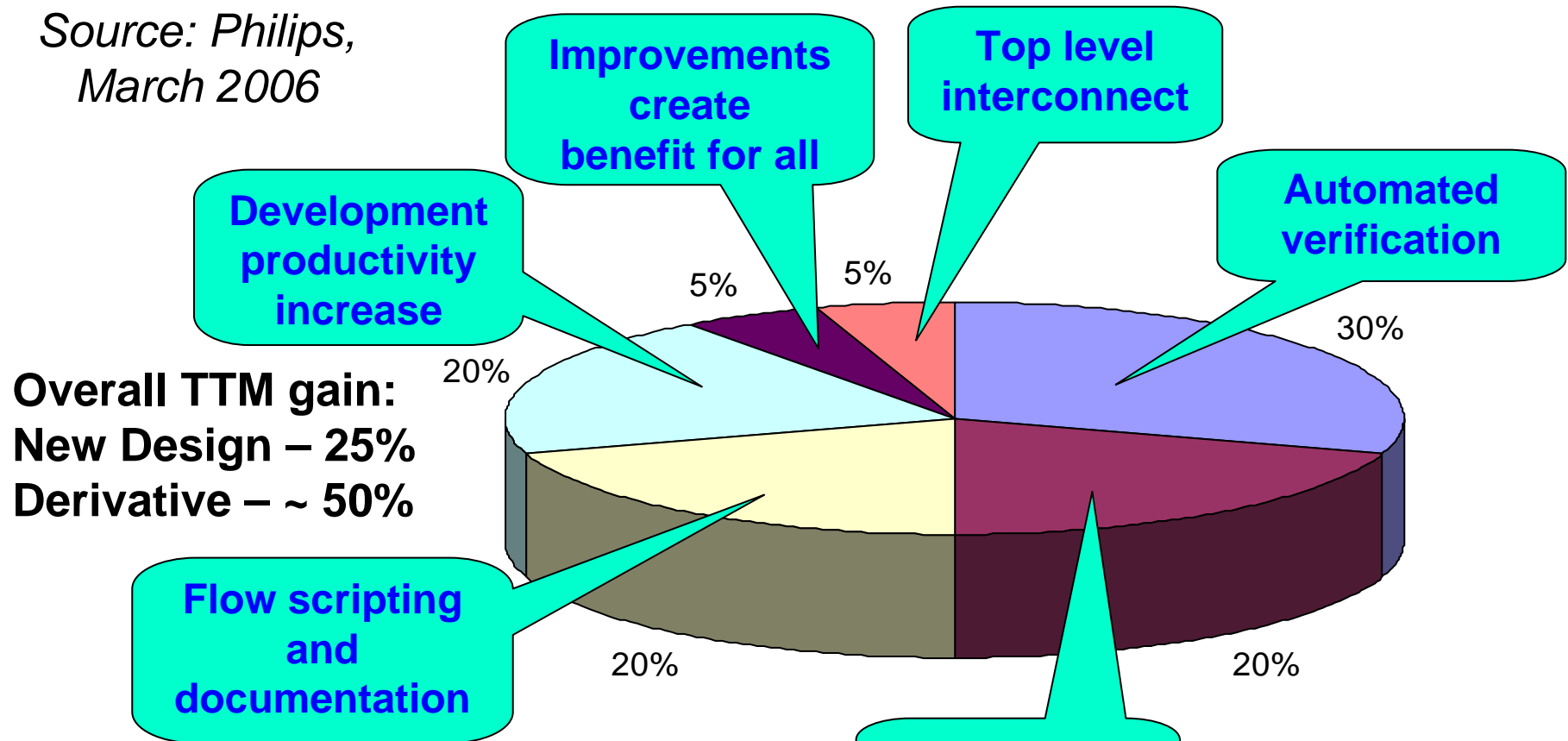
Achieve an open standard for a development framework upon which an SoC development flow, from components to chip, can be built allowing distribution and use of IP from varied sources as well as the free choice of tools used in the SoC development

Completing to Our Vision

- **3 specifications publicly released**
 - RTL support baseline : v1.0 Dec 2004
 - + Timing Constraints: v1.1 June 2005
 - + Hierarchy, Verification: v1.2 April 2006
- **Design-chain support started with v1.0**
 - Multi-vendor validation of principles
 - Multi-vendor demonstrations with each release
- **Formal standardization of deliverables started**
 - IEEE 1685 Working Group taking v1.2 (IP-XACT) specification
- **Gaining industry recognition**
 - Well over 2000 downloads, hundreds of companies
 - Membership grown to 57 members!
 - Representing US, Japan and the EU

IP-XACT Benefits Today (v1.2)

Source: Philips,
March 2006



Overall TTM gain:
New Design – 25%
Derivative – ~ 50%

IP-XACT  **Enabled**

The **SPIRIT** Consortium 

57 members strong, and growing!

Board of Directors



Contributing Members



Reviewing Members



Associate Members



Building The Consortium for the Future

- **Industry sees a strong role for The Consortium**
 - Proven body for multi-vendor IP and flow integration
- **The Consortium is structuring for long term sustainability**
 - Became a California non-profit corporation (March 30th 2006)
 - Increase transparency on operational processes
 - Expand international operations
 - Formalize relations with other standards organizations
- **And carrying forward our key values**
 - Clear technical focus and industry contribution
 - Membership differentiation based on engineering dedication
 - Keeping low-cost approach
 - Able to cooperate with other organizations



New Vision for The Consortium

- **To establish a set of IP and tool integration standards enabling proliferation of IP reuse through design automation**
- **Built on our membership experience**
 - Clear technology vision that lowers design risk
 - Removing barriers to market through IP automation standards
 - Enabling best core technology and tools to support it
 - Fueling SoC innovation through design integration
 - Enabling fastest path to market for embedded systems design
- **Deliverables driven through to standardization**
 - All specifications will be pushed in batches through IEEE

With New Brands and Room for Growth

- **IP-XACT: The Meta-Data Specifications**

- IP-XACT is the name for the meta-data specifications delivered by The Consortium



- The Consortium may consider new specification families that promote our vision

- **The SPIRIT Consortium: The Organization**

- The Consortium has a new logo!

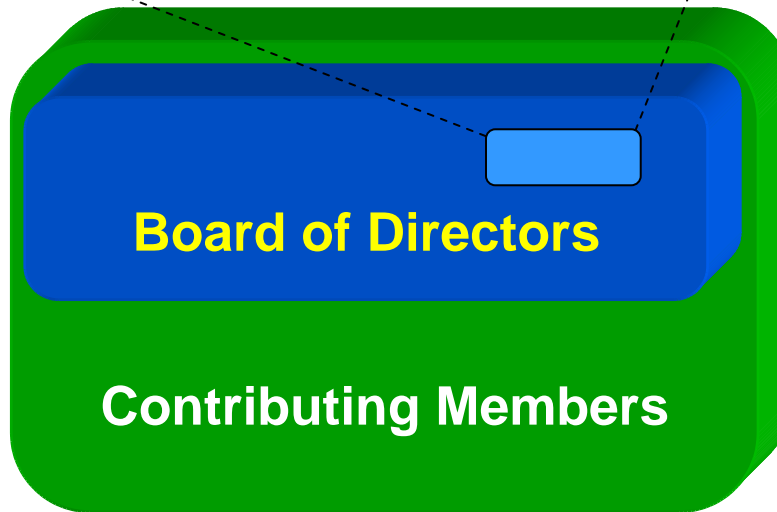


The Consortium Membership Structure

**Officers Elected
by BoD**

President
Vice-President
Technical Director
Marketing Director
Treasurer
Secretary

**BoD elected from
Contributing Members
Currently set at 9 companies
Number set by BoD Approval**



**Requires Engagement
Contribution & BoD
Approval
Are candidates for BoD
position**

**Non-Profit Organizations and
Institutes by BoD Approval**

Associate Members

**Free Membership
Only Companies**

Reviewing Members

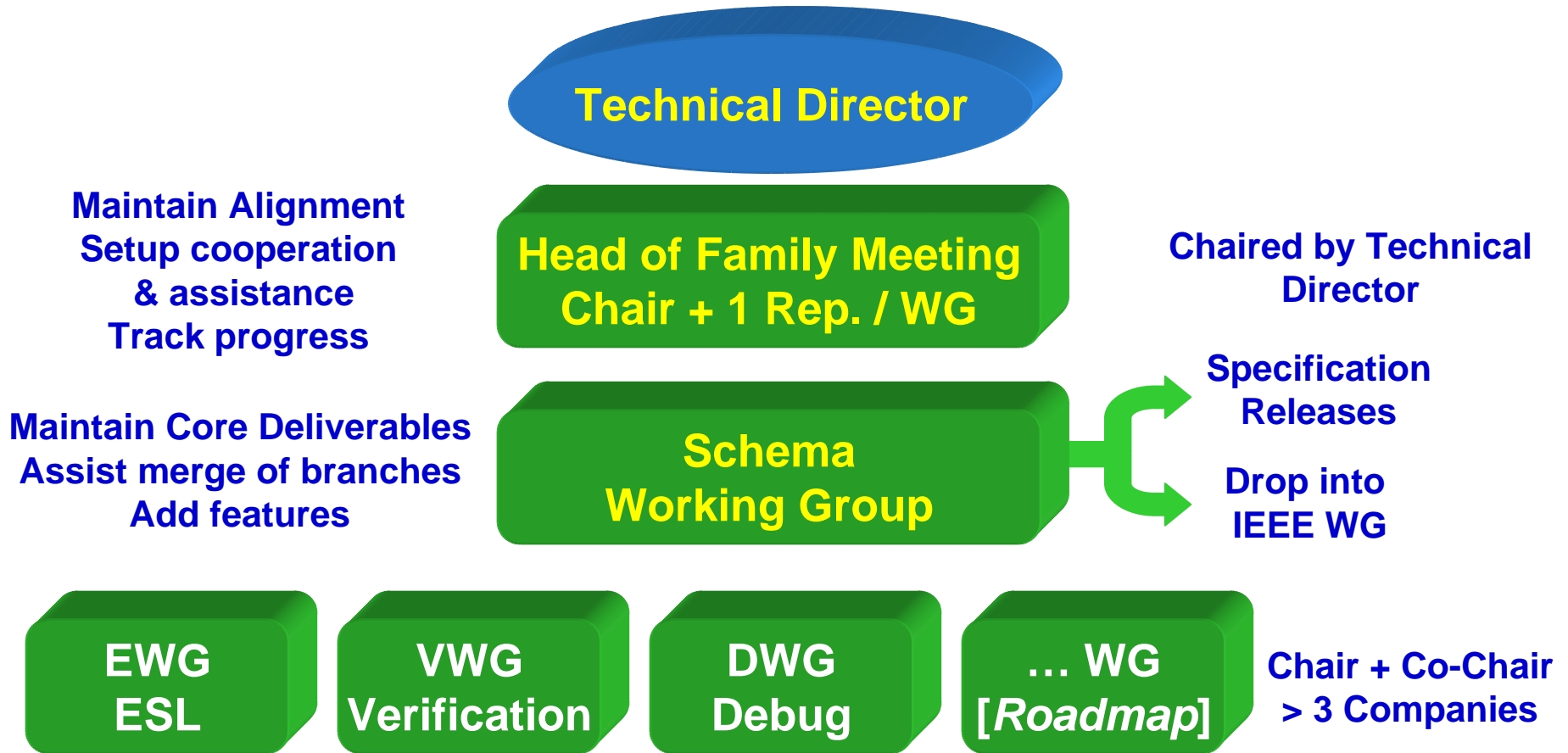
The Consortium Officers & BoD

President	Ralph von Vignau	NXP
Vice-President	Christopher Lennard	ARM
Treasurer	Pierre Bricaud	Synopsys
Technical Director	Gary Delp	LSI Logic
Marketing Director	Christopher Lennard	ARM
Secretary	Victor Berman	Cadence
Director (& Board Chair)	John Goodenough	ARM
Director	Victor Berman	Cadence
Director	Jean Bou-Farhat	LSI Logic
Director	Bill Chown	Mentor Graphics
Director	Bart De Loore	NXP
Director	Frank Ghenassia	STMicroelectronics
Director	Pierre Bricaud	Synopsys
Director	OPEN	
Director	OPEN	

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Technical Working Group Organization



Working Groups develop topic-specific technical updates
Constant cooperation with S-WG
Merge with S-WG main stream following BETA validation
1 vote / company

The SPIRIT Consortium Technical Goals

– Principles of operation

- Language neutral
- Progress by contribution
- Open source examples
- 2 working implementations for public release
- Alpha, beta, release, IEEE

– Build on existing standards

- XML (W3C)
- Synchronize with IEEE, Eclipse, OSCI, Si2, VSIA...

– Standardize one IP meta-data description

- One way to describe IP to enable configuration and integration

– Standardize one API for generator integration

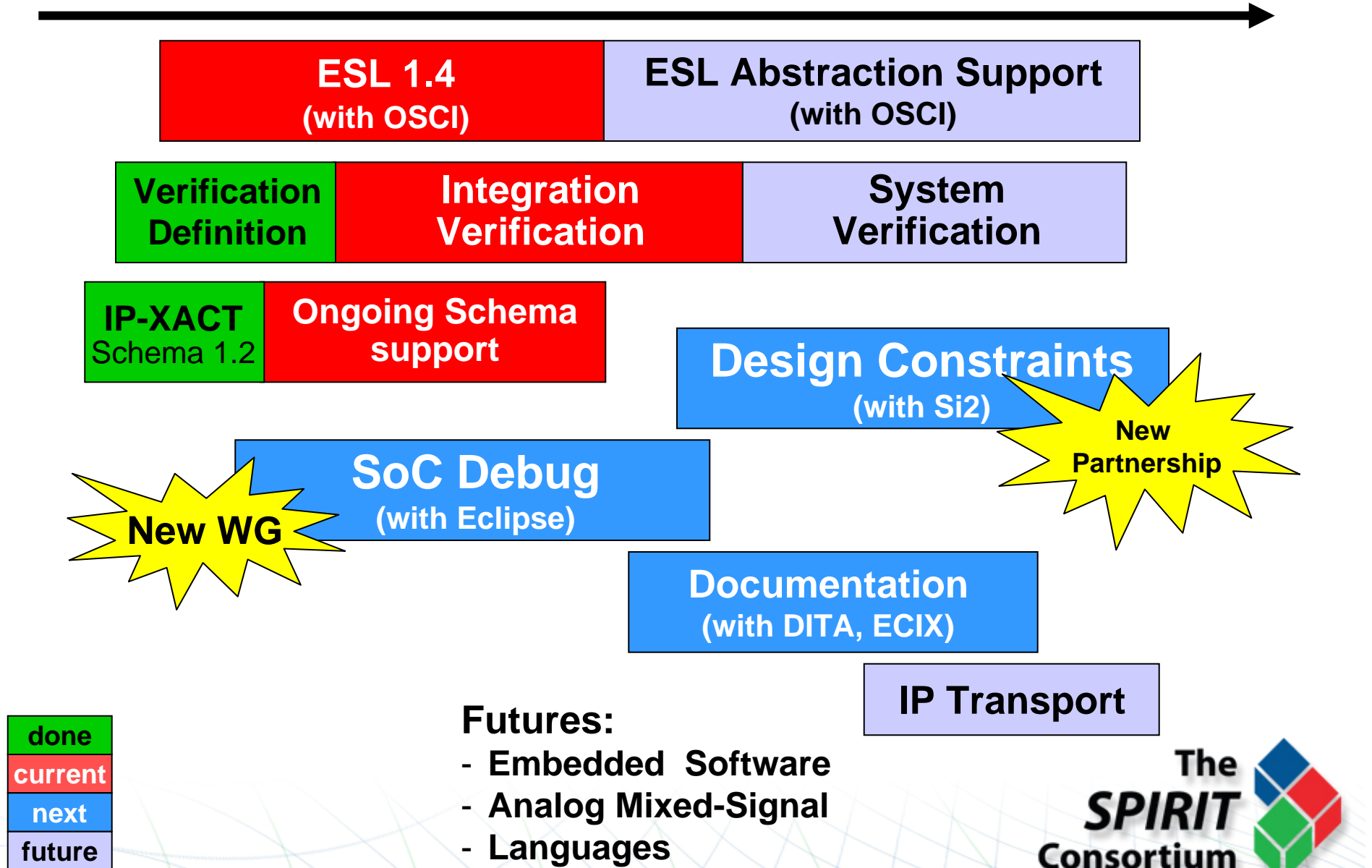
- Enable efficient and cost-effective integration of multi-sourced IP and tools



Elements of IP-XACT Deliverables

- **Validated and consistent release package**
 - Specification, Schema, XSLT converter, Open Source Examples
- **Schema includes**
 - Component schema for cores, peripherals, buses, components
 - Design schema for systems, component instancing, connectivity
- **Bus definitions**
 - Re-usable definitions for bus interface, integration reqs, defaults
 - Comprehensive set for common buses (first release in IP-XACT, The SPIRIT Consortium specification v1.2)

Roadmap Topics



done
current
next
future

Schema Working Group

- **SWG Chair: Greg Ehmann, NXP**
- **Active member companies**
 - ARM, Cadence, CoWare, Infineon, LSI, Mentor Graphics, NXP, ST Microelectronics, Synopsys
- **SWG activity: Develop IP-XACT baseline schema and address the following**
 - Merging of all new additional feature sets
 - Ensuring consistency, extensibility & compatibility
 - Having sub-groups to address small scale additions
 - Main channel to IEEE

ESL Working Group

- **EWG Chair: Jean-Michel Fernandez, Cadence**
- **Active member companies**
 - ARM, Cadence, CoWare, Infineon, LSI, Mentor Graphics,
NXP Semiconductor, ST Microelectronics, Synopsys
- **EWG activity: Develop IP-XACT with ESL extensions, specification v1.4, to address the following**
 - Include all IP-XACT features
 - TGI – Tight Generator Interface
 - Model TLM component (SystemC, SystemVerilog... but not only)
 - Model mix TLM and RTL component (different abstraction levels)
 - Model transactors (to bridge between two abstraction

Verification W

Moving to Complex verification with New Charter:

VWG Chair:

- John Swanson, Synopsys

Active member companies

- ARM, Cadence, LSI, Mentor Graphics, NXP, ST, Synopsys

Completed VWG Activity:

- Made 1.2 schema enhancements needed for RTL Verification including
 - Assertions
 - Monitors
 - Passive interfaces
 - Verification file sets
 - Mixed language verification
 - Testbench generation (RTL)

- To identify, develop, validate and deliver extensions to the 1.4 version of the IP-XACT specification
- to support IP-based SoC verification at multiple / different levels of abstraction.
- All extensions to the IP-XACT specification must be independent of the tools and IP used in IP/SoC design
- Will be built on the existing foundation of IP-XACT v1.4

Scope of new VWG

- Information in the metadata to enable the automation of structural test cases in a verification environment
- Testbenches at multiple levels of abstraction for different target environments
- The reuse of tests from component level to system level where applicable
- Testbench assembly automation including mixed abstraction level verification environments

Consortium





Debug Working Group

DWG Chair: Anthony Berent, ARM

— Charter

- Engage debug product companies
- Create technical exchange with the Eclipse DSDP group
- Define requirements for describing HW targets to SW debuggers
- Identify IP-XACT debug extensions and semantic rules
- Demonstrate that IP-XACT can be generated by design tools and used by a variety of debug tools

— Scope

- Ensure use of IP-XACT to describe IP to debug tools
- Extension of IP-XACT technical capabilities to cover at least
 - Additional register / memory info needed for debug tools
 - Description of debugger access (e.g. JTAG)
 - Identification of processor architectures / versions



Proposed

Design Constraints WG

- **Value: Consistent constraints throughout design flow**
- **Group is in formation process**
 - Looking to resource this activity
 - Plans for collaboration with Si2
- **Scope: Domain-based properties**
 - Clocks, resets, power, frequency, security, simulation, etc
- **Scope: Parameterization of constraints**
 - Generic structure defined for Parameterization
- **Scope: Chip-level constraint inputs**
 - Interface timing
 - Extend the application of meta-data into front and back-end flows



Proposed

Documentation WG

- **Value: consistent, up-to-date documentation automatically**
- **Scope:**
 - Documentation that describes the status of the system accurately at any time should be able to be extracted
 - Types of automated documentation that would benefit are technical datasheets, integration manuals, user documents, functional descriptions ...
 - Requirements defining the types of content and their usage in documents - to be done in cooperation with current document standards groups, e.g. DITA, IEC 61360, OASIS, Si2 ...
 - Specification of the XML schema requirements and definition of the schema for support of automated documentation

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IEEE Standards Process (P1685)

- **SPIRIT Technical deliverables:**

- Initial technical drop is based on IP-XACT, v1.2 complete
- Final drop: IP-XACT w/ ESL Extensions

- **Chair:** **Victor Berman**, vberman@cadence.com

- **Vice-Chair:** **Kathy Werner**, kathy.werner@freescale.com

- **Secretary:** **Gary Delp**, gary.delp@lsil.com

- **Meeting Schedule:**

- First meeting, May 06
- Operational policies, PAR scope agreed
- Work started on v1.2 examination & requirements for ratification

IEEE P1685

– Organization

- Entity-based WG – one company one vote
- Self funded through member dues on sliding scale
 - > \$1B pay \$10K
 - > \$1M pay \$ 5K
 - < \$1M pay \$ 1K

– Current Membership

- ARM, Cadence, CoWare, Denali, Freescale, LSI, Mentor, NXP, Sonics, ST, Synopsys

– Current Web Site <http://www.eda.org/spirit-p1685/>

– Tracking to an expedited schedule

- Will use IEEE-funded services to expedite ballot and publication
- Will use professional technical editor for final documents
- Will provide hosting of XML schema for free use



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The SPIRIT Consortium: Conclusions

- **International standardization organization**
 - Formed June 2003, with CA non-profit status in 2006
- **Supported in products from multiple vendors today**
 - e.g., 9 companies publicly demonstrated support at DAC 06!
 - Many others known to be deploying
- **The Consortium deliverables**
 - IP-XACT for RTL design (v1.2): Current Release
 - IP-XACT IEEE standardization (P1685): May 06 start
 - Tight generator interface and ESL extensions: v1.4 plan
 - Beta versions available to Reviewing & Associate Members today



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Purpose and Outline

- To motivate a system level view of power expression
- To describe Aspect design principles
- To introduce the IP-XACT structures for capturing design intent

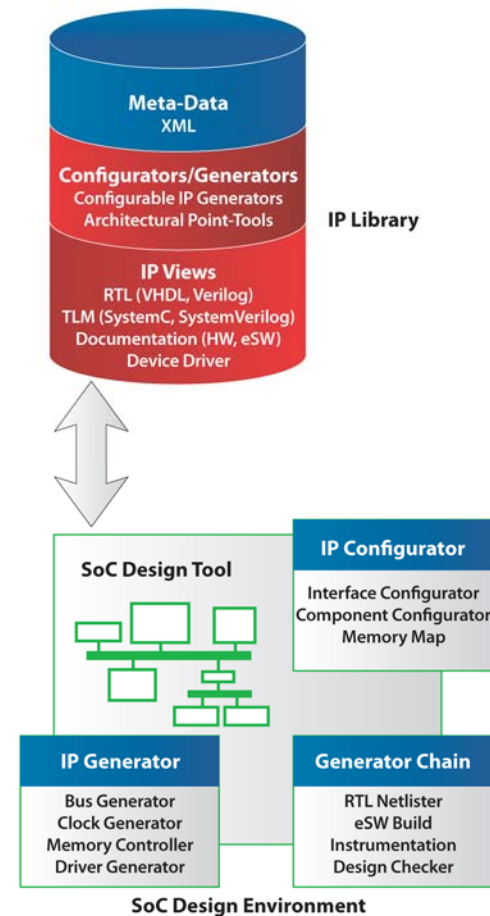
Outline

- Key Messages
- Hierarchical view of Energy Conservation
 - Progressive refinement
- System Aspects of Power
 - Driving structural requirements
 - Enabling Reuse
- IP-XACT – a method for capturing machine readable design and component descriptions
- Summary

Introduction to IP-XACT



- IP-XACT is the SPIRIT Consortium Standard for documenting IP.
 - It enables highly automated design creation and configuration
 - Tool independent
 - Machine readable
 - Base capability + standard “extension mechanisms”



The Spirit Vision for SoC Design

- IP shipped with machine readable IP-XACT 'data-book'
 - IP cataloged using IP-XACT meta-data
 - IP will be automatically configured and integrated into designs

- From IP-XACT, data for all design views is generated
 - Simulation models, docs, tool-config, embedded software, etc.
 - Soc configuration-data managed through project life-cycle
 - Consistency between design and verification views maintained

- IP-XACT-enabled specialist IP and Tools market emerges
 - Point tools operate in any IP-XACT enabled design environment
 - A rich 3rd-party IP generator market emerges



Low Power Design Needs

- Support Low Power Design Techniques thru the entire design flow using a single file format.
 - Design Representation
 - Accurately define and capture the low power design intent, modes and constraints.
 - Design Implementation
 - Floorplan and power grids.
 - Common constraints for all tools (Synthesis, APR, timing, DFT)
 - Design analysis tools with single power constraints.
 - Accurate power estimation and measurements
 - Design Verification
 - Voltage oriented simulators
 - Various static power technique modeling and simulations.
 - Silicon validation and correlation.

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- Bus definitions
 - **Re-usable definitions for bus interface, integration reqs, defaults**
 - **Comprehensive set for common buses**
 - first release in IP-XACT, The SPIRIT Consortium specification v1.2
 - Extensions to the capability in development
- Generator Interfaces
 - **Tight Generator Interface (first in IP-XACT with ESL Extensions, v1.4)**
 - Access IP-XACT data-bases directly
 - Supersedes LGI

IP-XACT Summary

- A vendor, tool, and process neutral way of documenting information about a component.
 - Built in extensibility enables new information domains to be added.
- Generators can be used process that information into useful design objects.
 - Perhaps, inserting level shifters into netlists where two components with incompatible voltage ranges are connected together.
- If IP-XACT looks like an interesting candidate for storing and processing power information, or structure
 - The SPIRIT Consortium would be very pleased to help and assist with a more detailed technical examination.



Thank you!

The
SPIRIT
Consortium

