



# Advancing the Analog Custom Design Interoperability

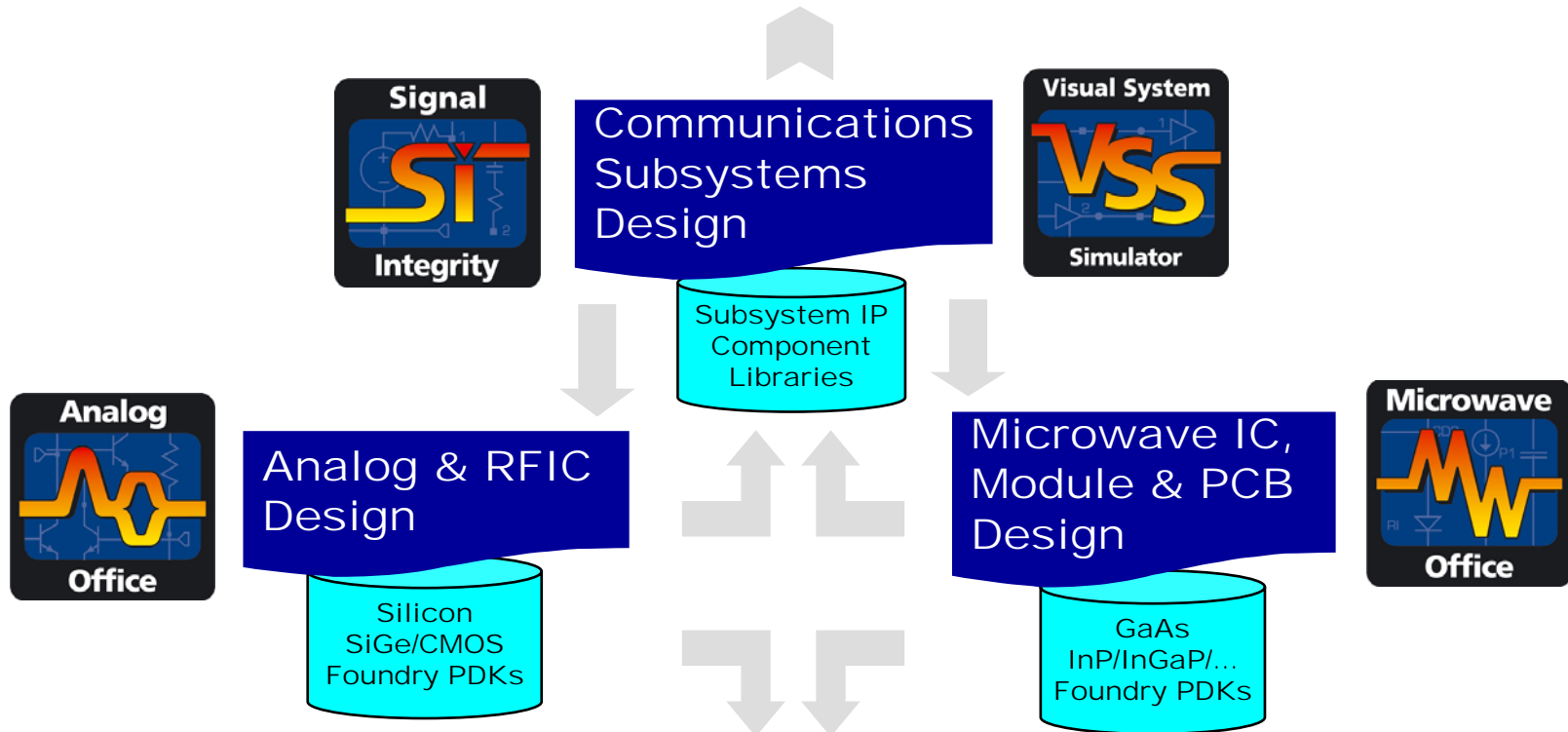
Tom Quan



# AWR Product Solutions

## System Components

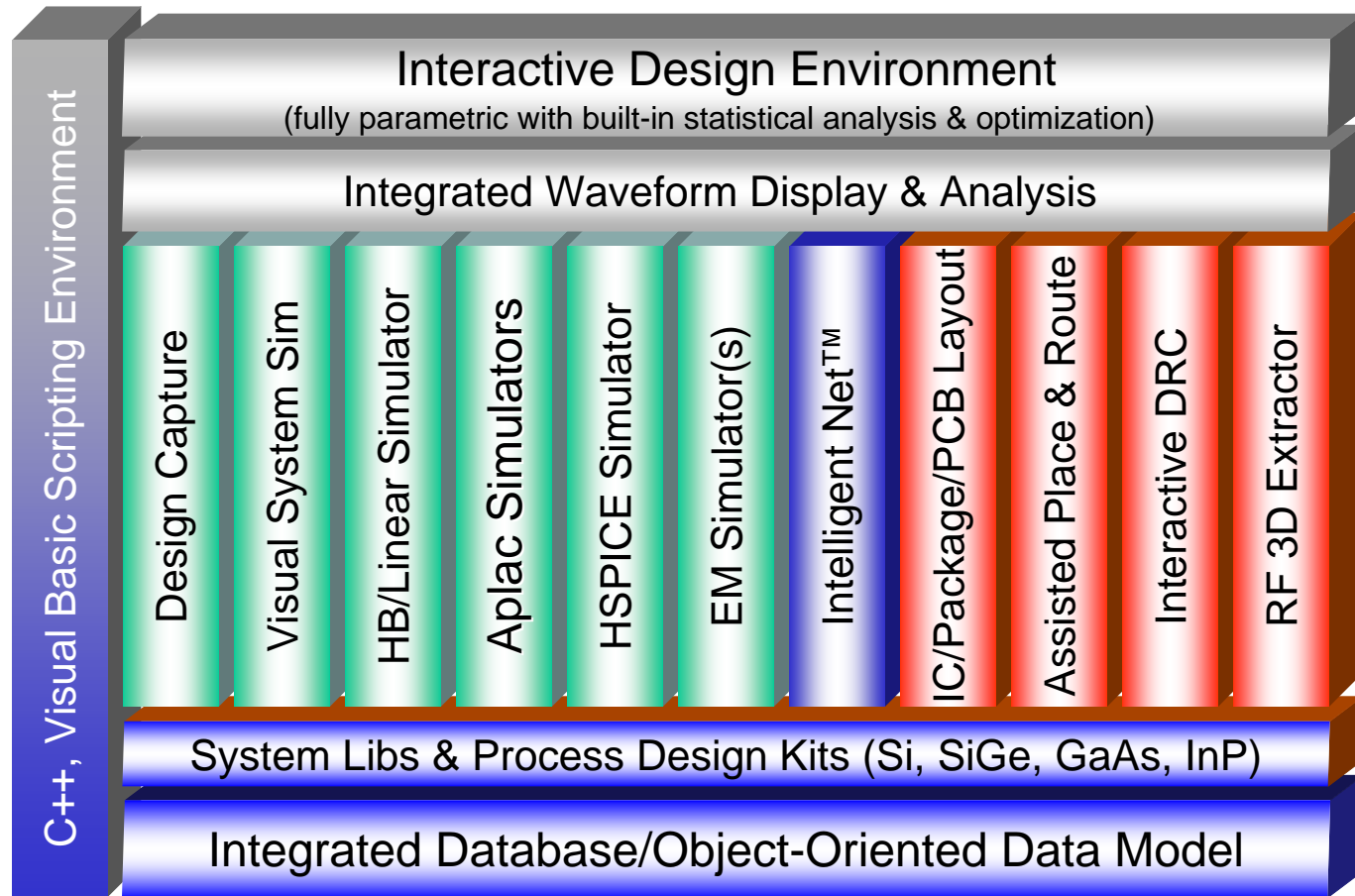
*Satellite 3G-Wireless WiMax UWB 802.11a,b,g.. Bluetooth xDSL Cable Optical*



## Circuit Components

*LNAs Mixers Amps Transceivers QAM QPSK Laser Drivers & PLLs Synthesizers Filters CDRs MUXs Detectors*

# AWR Solution Architecture



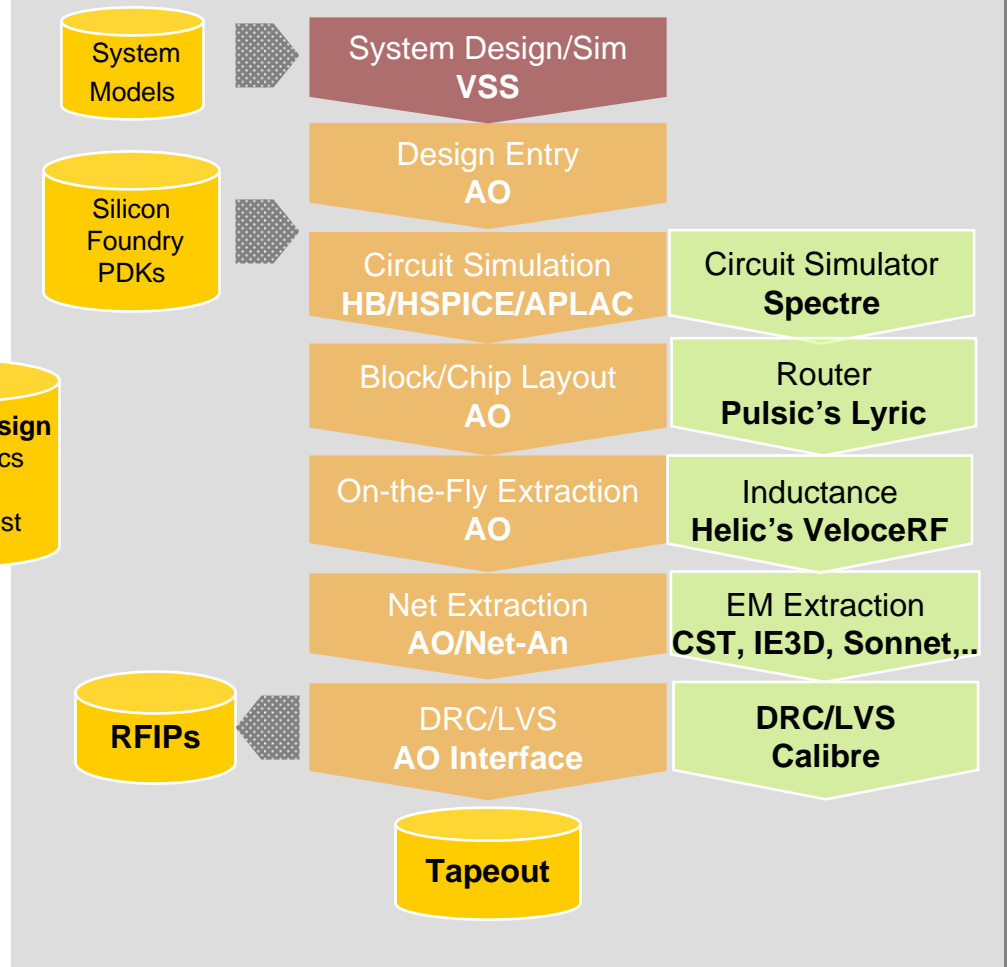
*Unified Data Model & UI for  
All Phases of Design*

# Data and Tool Interfaces

## Full Chip Integration With Digital Blocks



## Analog Office Design Flow

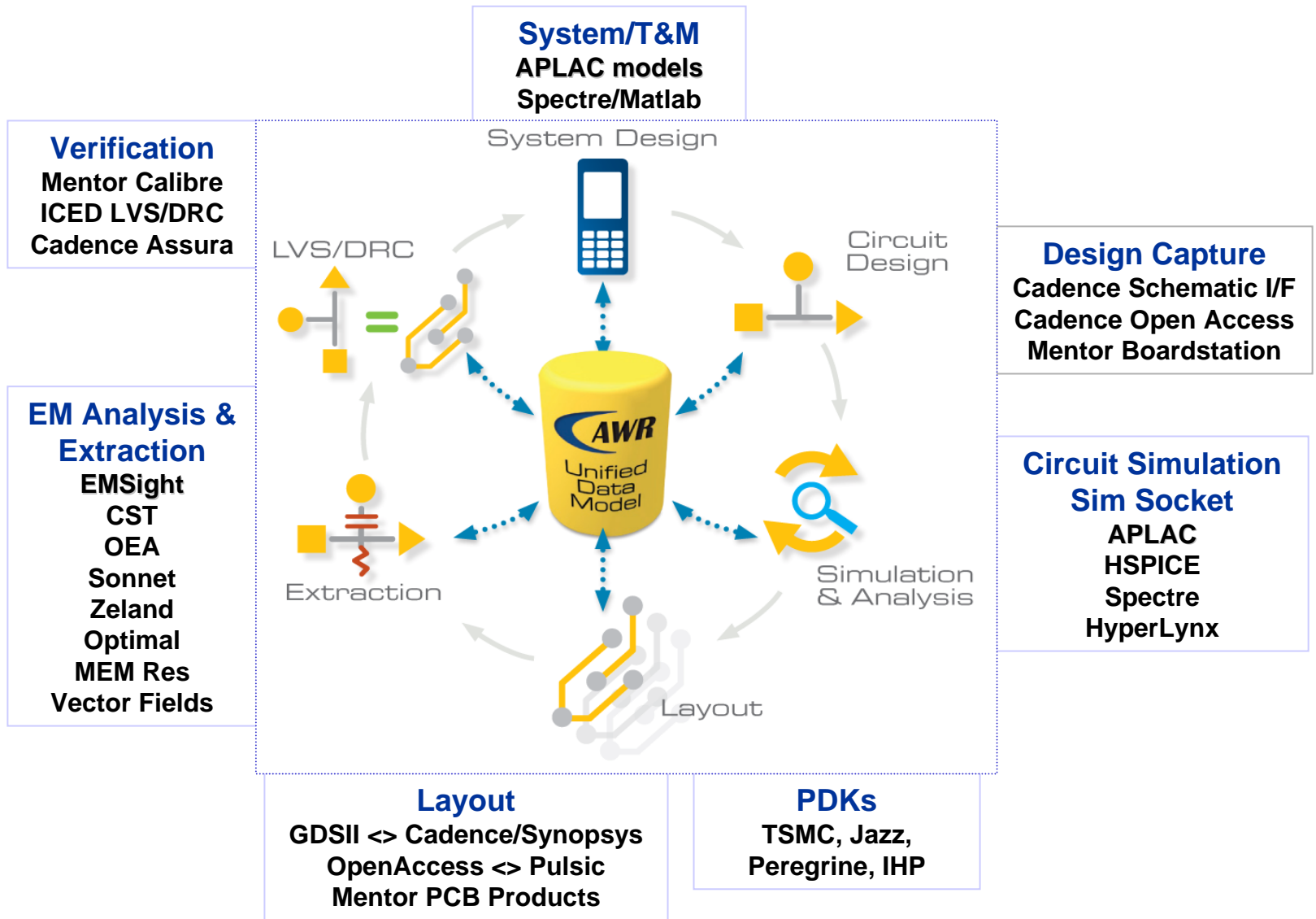


# AWR Open Design Platform

- Unified data model interoperable with OpenAccess
  - Support easy-to-use & highly interactive design environment
  - OA data model compliant
  - Clean interfaces with other OpenAccess compliant tools
- Open API/Open Sockets
  - EM simulation/extraction – 7 tools plugged in today
  - Circuit simulation – 4 simulators plugged in today
  - Physical design – layout editor, auto P&R, and layout compaction plugged today
  - Physical verification – 2 DRC/LVS tools today
- Open PDK
  - Standard Pcell development language – C++, Python, Tcl

*Open Platform ↔ Interoperability*

# AWR Interoperability



# RF Process Design Kit

- Configurable passive & active components
- Scalable active devices
- Accurate RF non-linear device models
- Symbols, models, layout generators, DRC/LVS rules
- Temperature variations, corners

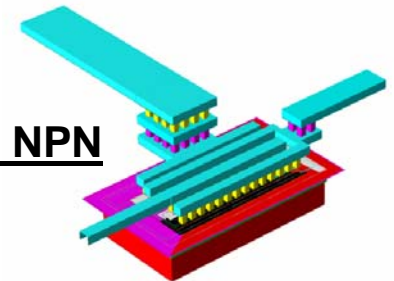
## • Active devices

- NPN transistors for digital/high performance/high breakdown
- RF and standard N- & P-channel MOSFETS
- Junction varactor
- MOS varactor
- N+ P-well diode/P+ N-well diode

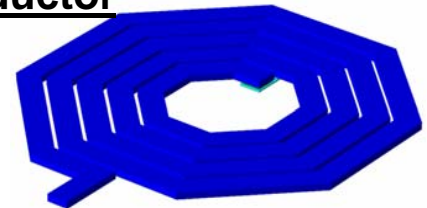
## • Passive devices

- Metal-insulator-metal capacitor
- Scalable octagonal inductor
- N-well resistor with multiplicity for series/parallel connection
- Polysilicon resistors with multiplicity for series connection
- Diffusion resistors with multiplicity for series connection

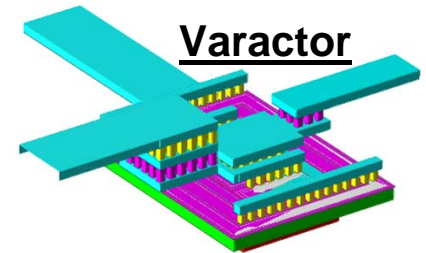
SiGe NPN



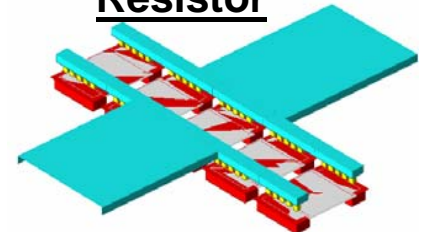
Inductor



Varactor



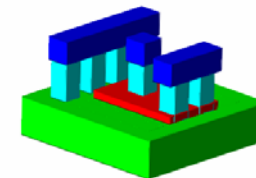
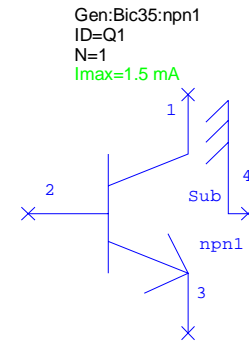
Resistor



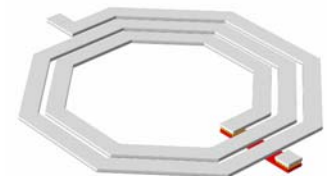
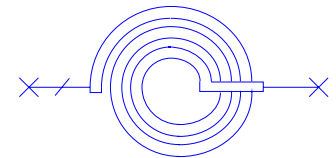
# PDK Interoperability Requirements

- Design constraints
  - Electrical
  - Physical
  - Manufacturing
- Simulation Models
  - HSPICE, Spectre, others
- Electrical
  - Schematic symbol
  - Naming conventions
  - Electrical/physical parameters
- Physical
  - Parameterized Cells (Pcells)
  - DRC/LVS/LPE/DFM rules (from foundry)
  - GDS layer map (from foundry)

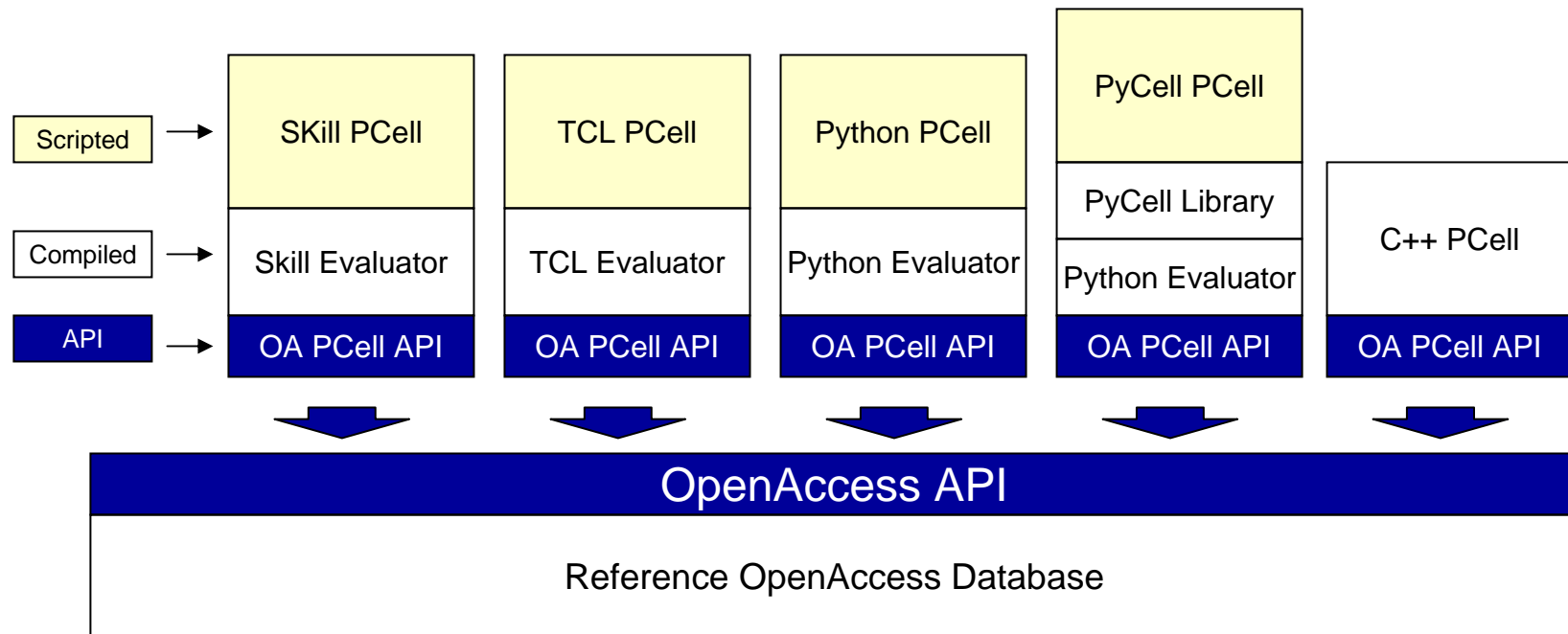
Symmetry  
Distance between inductive elements  
Placement of dummy elements  
Placement of pass capacitors  
P&R of guard band  
Common centroid  
Placement of parasitics  
Zig zag placement of Rs  
Enclosed R, C and MOS  
Isolation of N-region, Additional substrate for M



Gen:Bic35:SPIRAL  
ID=L1  
NTURNS=2.5  
W=5 um  
S=2 um  
IDia=50 um



# PCell on OpenAccess



- Which approach used does not matter that much
- Pcells created using any of the approaches could be ported to any OA system
  - Compiled PCells will require compilation on each supported platform
  - Scripted PCells will only require the supporting plug-in to be compiled on each platform

# Steps to Ensure PDK Interoperability

1. Validating **several** sets of generic Pcells written in Python, C++ and Tcl on **one** OA-compliant design platform (AWR)
2. Validating **one** set of generic Pcells on **different** OA-compliant design platforms
3. Defining a **common** format for electrical and physical parameters
4. Defining a **common** format for design constraints
5. Validating a generic PDK on **different** OA-compliant design platforms





The industry's most open high frequency design platform

Thank You!

Tom Quan ([tomq@appwave.com](mailto:tomq@appwave.com))

