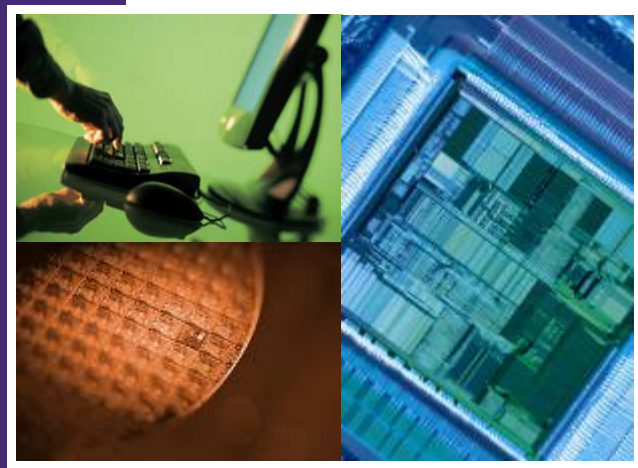
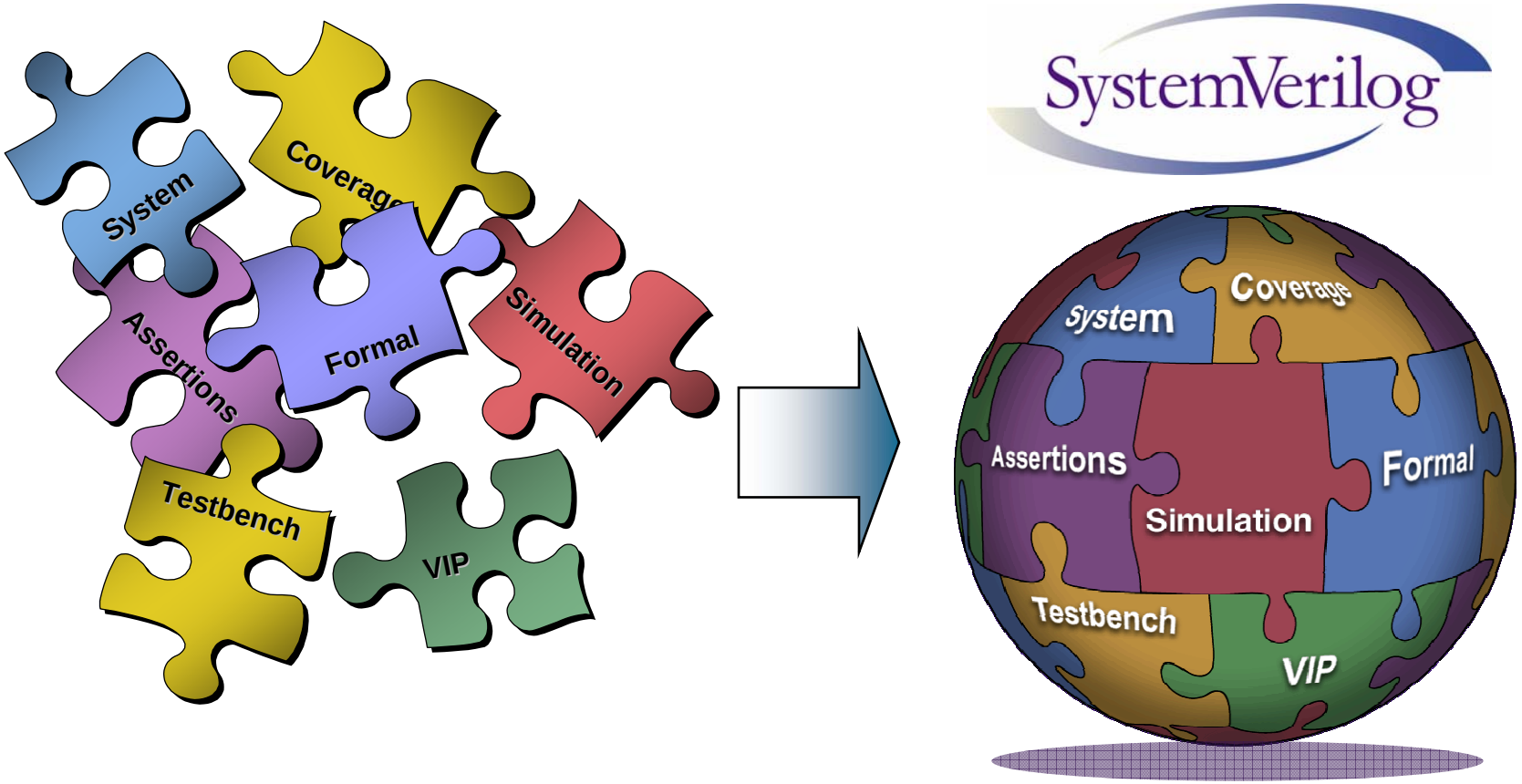
Synopsys SystemVerilog Update

Steve Smith
Senior Director, Platform Marketing
Synopsys Verification Group



SYNOPSYS®
Predictable Success

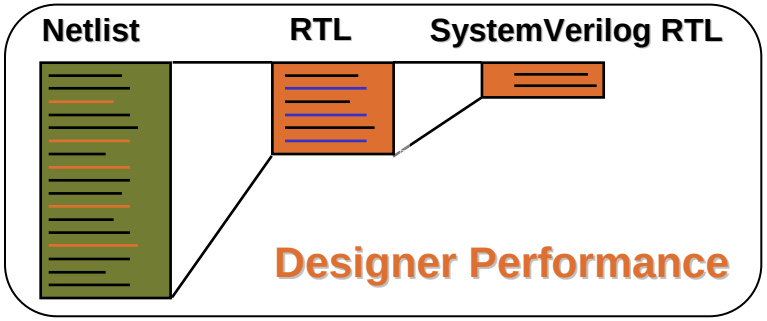
SystemVerilog: Unifying Design and Verification



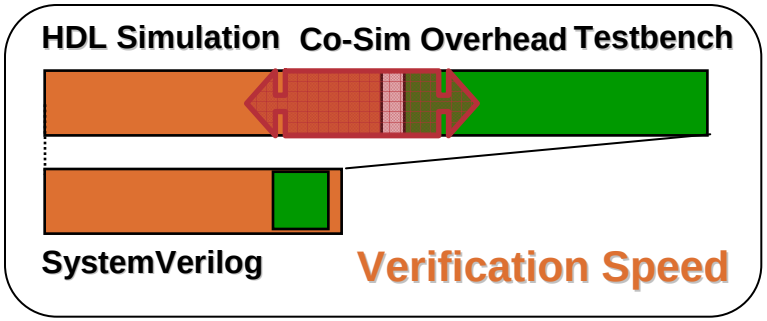
Fragmented Verification

Single, Unified Language

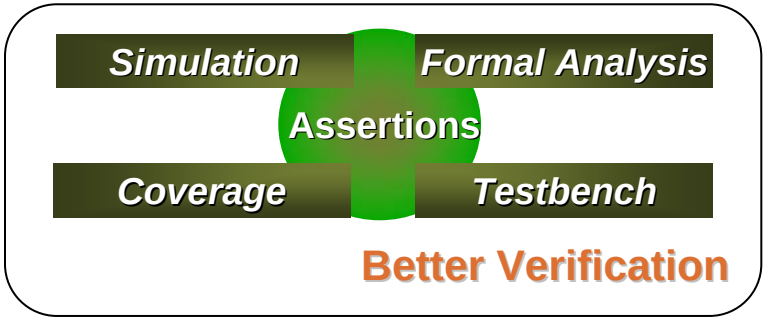
SystemVerilog Increases Productivity



- Extends Verilog to Higher Abstraction
- 2-5x less code
- No change in synthesis flow



- Full native testbench
- 2-5X faster verification



- Built-in assertions
- Capture intent in RTL code
- Pinpoint design errors quickly

SystemVerilog is an IEEE Standard

IEEE APPROVES SYSTEMVERILOG® and VERILOG® STANDARDS FOR ELECTRONIC DESIGN

IEEE

PISCATAWAY, N.J., USA, 9 November 2005 The IEEE today announced that it has approved SystemVerilog, IEEE Std 1800(TM)-2005, as a new standard and has approved Verilog, IEEE Std 1364(TM)-2005, as a revision to the popular Verilog hardware description language (HDL). SystemVerilog extends the Verilog language, the predominant language used for chip design, to address' the growing complexity of electronic system and semiconductor designs. SystemVerilog is a unified language for hardware design, specification, and verification that was developed within the IEEE Standard Association's Corporate Program. The revisio
minor errors.

The broad IEEE SystemVerilog 1800 standa
validation, especially for large-gate-count, I
description and verification language (HDVL
advanced design modeling capabilities, test
language, and a richer coupling with other l
semiconductor and system design communit
verification work flows more efficient. It also
leverage existing designs and intellectual pr

"IEEE 1800 enhances the Verilog HDL to ke
SystemVerilog 1800 Working Group and Ver
design and verification language, allowing e
pipelines, greater logic functionality and a h
transfer level code."

accellera

ACCELLERA APPLAUDS IEEE 1800™ SYSTEMVERILOG STANDARD APPROVAL

Electronic Design Industry Backs Standard for System-on-Chip Design and Verification

NAPA, California – November 9, 2005- Accellera, the electronics industry organization focusing on electronic design automation (EDA) standards, today welcomed the Institute of Electrical and Electronics Engineers' (IEEE) announcement that it has approved the SystemVerilog hardware description and verification language as IEEE Std.1800™-2005, "Standard for SystemVerilog Unified Hardware Design, Specification and Verification Language." The rapid approval by the IEEE through its Corporate Standards Program finalizes the accreditation process and provides design and verification engineers assurance that their SystemVerilog system-on-chip (SoC) designs are based on a single, stable standard.

70 SystemVerilog Catalyst Program Members

XtremeEDA
bluespec
ESTEREL Technologies
LOA Technology
SYNAPTICAD
WHDL
CONTROLNET INDIA
NOVAS
Verification Technology
DOULOS
eve
ARM
ALATEK
SiConcepts

VhdlCohen Training
PRODUCTIVITY DESIGN TOOLS
Blue Pearl Software
nSys
JEDA Technologies
Real Intent
Verific
Posedge Software
J. van der Schoot Consulting
Sunburst Design
cadence
TRANSEDA
CBE
interra systems
eNd-to-eNd Solutions
KACPER
SUTHERLAND HDL
OKI
chipvision
SUMMIT
veriEZ
The Verification Tools Company
eInfochips
ACEVERIFICATION
www.aceverification.com
ALDEC
The Design Verification Company
INTRINSIX
Tharas Systems
hdLab
denali
Project VeriPage
Silicon Interfaces
a software and vlsi design center
CALYPTO
Veritools
SPIKE Technologies
JASPER design automation
IBEX
ingot
SEQUENCE
Enabling Power-Aware SoC Design
ADVEDA
TenisonEDA
tNi-VALIOSYS
PARADIGM WORKS
verilab
WSFDB Consulting
Aptix
SILICOMOTIVE SOLUTIONS
VGVP
Logic Research
Beach Solutions
Perftrends
avery design systems
PERFECTUS
The Verification Platform Company
GDA Technologies
ATRENTA
TERA SYSTEMS
The New Frontend

Growing SystemVerilog Ecosystem

SYNOPSYS®
Predictable Success

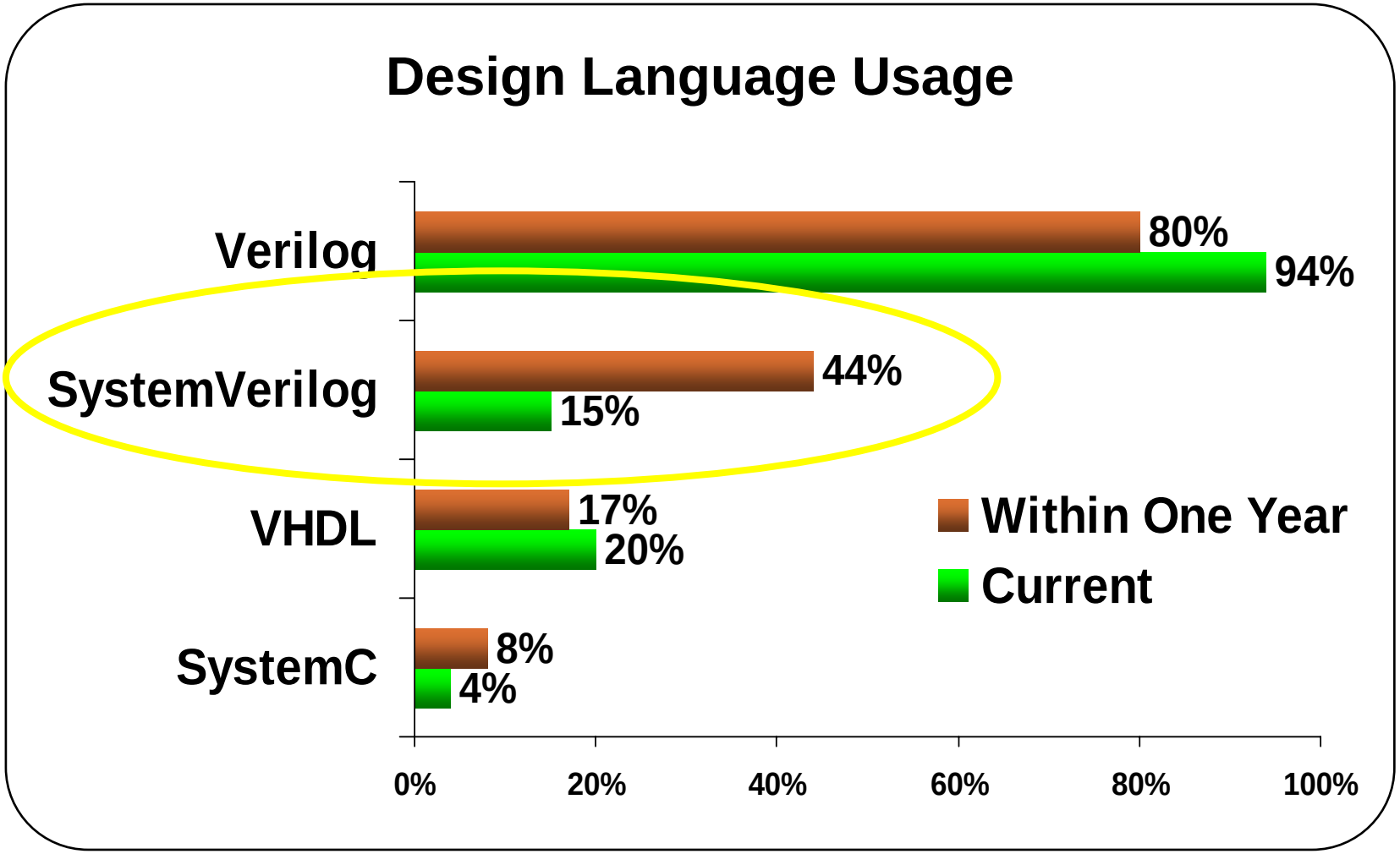
Industry's First Verification Library with Support for SystemVerilog and VMM

AMBA 3 AXI
AMBA 2 AHB/APB
Serial ATA I & II
PCI Express
USB On-the-Go
USB 1.1 / 2.0
PCI / PCI-X / PCI-X 2.0
10/100/1G/10G Ethernet
Serial I/O
I^2C
> 10,000 Memory Models

VCS Verification Library

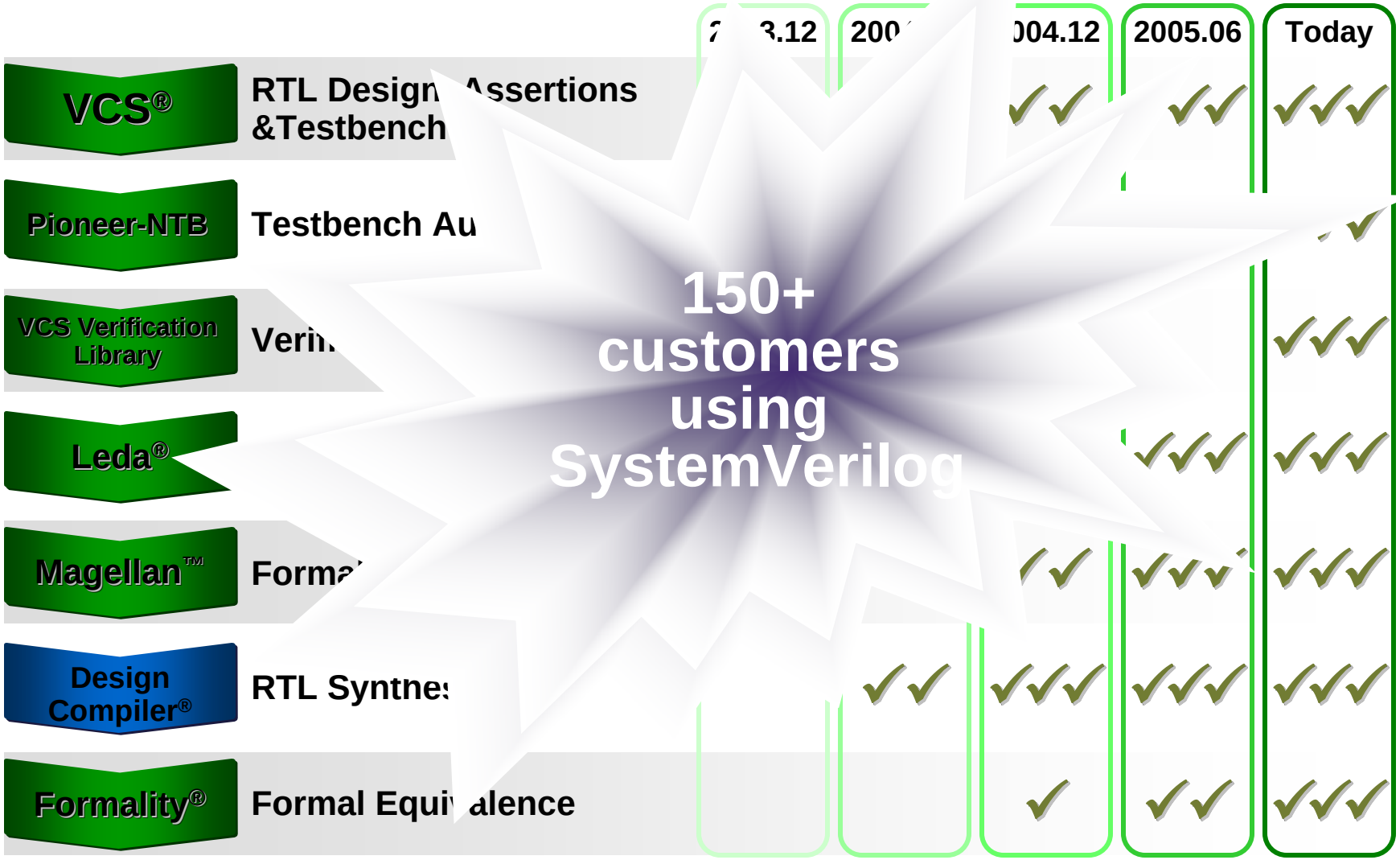
- 5X higher verification performance with VCS and Pioneer-NTB
- Supports industry's popular bus standards
- VMM-compliant Reference Verification Methodology

Rapid Growth in SystemVerilog Use



Source: Synopsys User Group (Boston) Survey September 2005

First Complete SV Design & Verif. Flow



SYNOPSYS®
Predictable Success

Learn More

www.synopsys.com/systemverilog

SYNOPSYS®
Predictable Success