IEEE P1800 Status Report

Synopsys EDA Interoperability Developers' Forum

Presenter: *Karen Pieper, Synopsys,*

Technical Chair IEEE 1800 SystemVerilog

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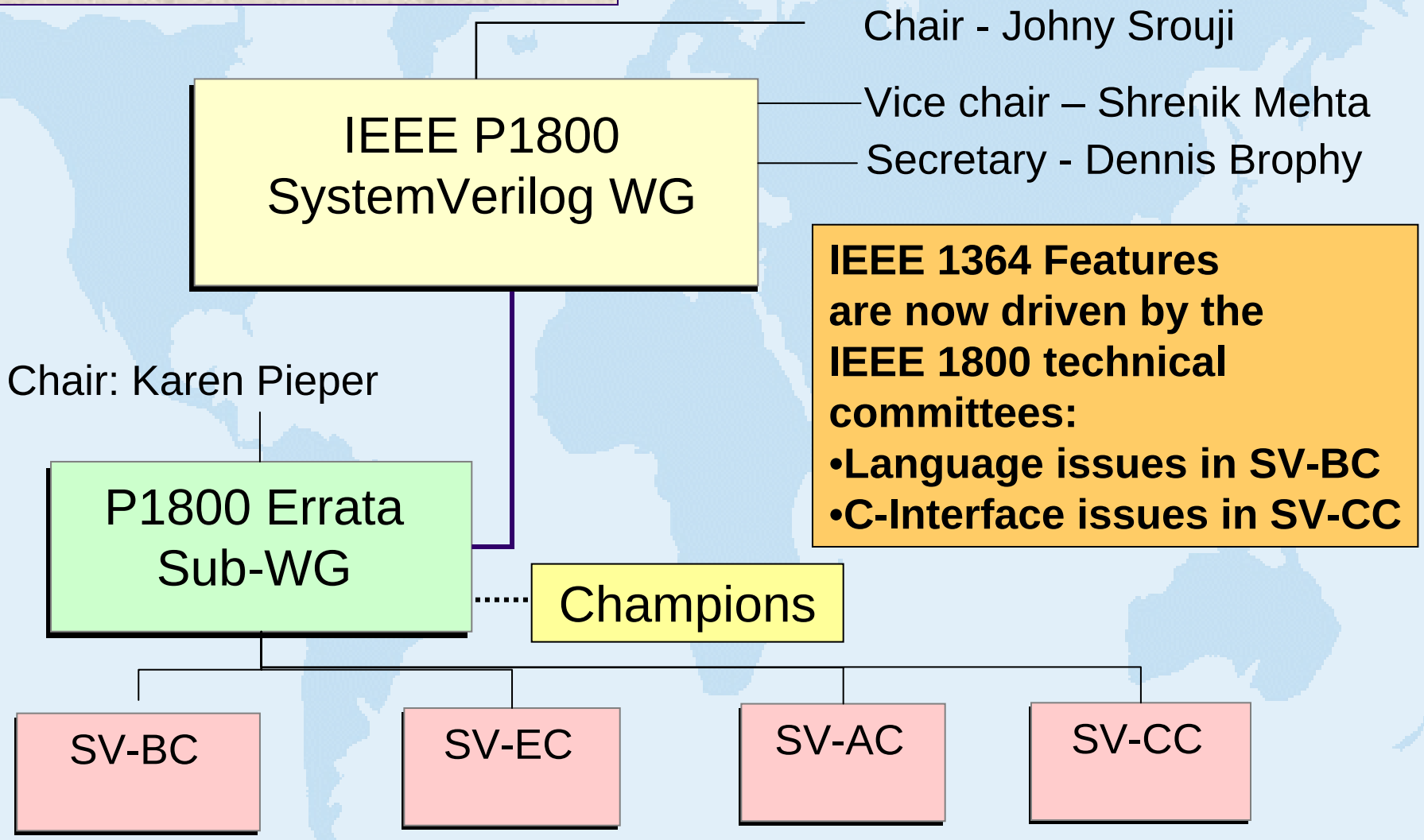
Agenda

- Organization & Structure
- Status of IEEE 1364 Verilog
- IEEE 1800 Goals Going Forward
- Current Status of Technical Committees
- How can you participate?
- Contacts

Organization

- Over 50 members on ieee1800 reflector
- 11 active members from Users' and EDA entities
- Elected Officers:
  - Chair: Johny Srouji, IBM corporation
  - Secretary: Dennis Brophy, Mentor Graphics
  - Vice-chair: Shrenik Mehta, SUN corporation

IEEE P1800 Structure



2005 Revisions Status Update

- IEEE 1364-2005 Standard for Verilog Hardware Description released
  - Can be purchased from

    http://shop.ieee.org/ieeestore/
- Pricing Information:
  - **IEEE Product No.:** SS95395
  - **List Price:** $120.00
  - **IEEE Member Price:** $95.00
  - **Product Size:** 8.5 X 11
  - **ISBN:** 0-7381-4851-2
  - **IEEE Standard No.:** 1364-2005

IEEE 1800-2005 SystemVerilog

- IEEE 1800-2005 Standard for SystemVerilog : Unified Hardware Design, Specification and Verification Language
  - Can be purchased from

    http://shop.ieee.org/ieeestore/
- Pricing Information:
  - **IEEE Product No.:** SS95376
  - **List Price:** $55.00
  - **IEEE Member Price:** $45.00
  - **ISBN:** 0-7381-4811-3
  - **IEEE Standard No.:** 1800-2005

P1800 Goals - The Big Picture

- Develop, Approve and Publish an IEEE standard of SystemVerilog 1800 and Verilog 1364
- PAR (Project Authorization Request) being worked on
  - Next revision targeted for submission to the IEEE in December of 2008
    - Add clarifications and correct errata
    - Local enhancements to ensure successful use
    - Enhancements to SVA
    - Enable interoperability with other standards
      - VHDL, AMS, SystemC, etc
    - Merge IEEE 1364 Verilog standard into P1800 SV Standard
  - Plan to maintain a “live” version of the LRM

Status

- Investigation of funding for merging the LRMs is underway
- Technical Committees are addressing errata and prioritizing issues
  - SV-BC Design subset of SV, and Verilog language
  - SV-EC Testbench subset
  - SV-AC Assertion subset
  - SV-CC External language interfaces: PLI, DPI, etc

SV-BC (Design) Status

- All 1364 & SV-BC issues being reviewed & prioritized.
- Current focus: ‘Major’ severity issues
  - If not addressed will lead to visibly different implementations
  - Preference to those that do not complicate merging of the LRMs or require edits to both specs.
  - Clarify intent even if no formal resolution
- Issue Groupings under investigation
  - First Round: Namespaces, Enumerated Types, I/O Errata/Clarification, Compiler Directives
  - Second Round: Configurations, Scheduling

SV-EC (Testbench) Status

- Errata categorization from issues database
  - Coverage related (8)
  - Randomization/Constraint related (8)
  - Miscellaneous: classes, queues, arrays, (35)
  - Scheduling/clocking/program block (15)
- Some areas of clarifications
  - Coverage
  - Arrays/Queues
  - Abstract class clarifications
- Priorities going forward
  - Focusing on errata items with clear/concise proposals
  - 1. Coverage related issues have taken time, since least known
  - 2. Randomization and constraint
  - 3. Classes/data types clarifications and corrections
  - 4. Scheduling semantics and clocking/program block

SV-AC (Assertions) Status

- Minor corrections and clarifications:
- Important corrections and local changes:
  - Proper definition of vacuous successes and provide finer control on when action blocks should execute
  - Arguments to recursive properties
  - Arguments to $isunbounded
- More profound refinements of the semantics of SVA
  - Annex E does not cover all clocked derived forms
  - Semantics of "calling subroutines on match of a sequence" is not well defined.
- Combined P1800 + 1364 LRM:
  - Incorporate by reference Accellera PSL

SV-CC (Interfaces) Status

- Resolve errata and clarifications
- Continue to enhance VPI to fully support all of the SystemVerilog constructs
- Merge the 1364 and 1800 LRMs
  - Improve the organization of the VPI sections
- Enhance the interfaces as needed to support new features added by the other committees

Contacts & Participation

- IEEE meetings are open to the public
  - Everyone is welcome to attend meetings and voice their opinions
- Voting membership / balloting
  - By company, requires IEEE-SA membership
- Working Group:
  - Web site: http://www.eda.org/sv-ieee1800/

Email addresses

  - Chair: Srouji at location US.IBM.com
  - Vice Chair: Shrenik.Mehta at location sun.com