

Esterel Technologies Talks SPIRIT

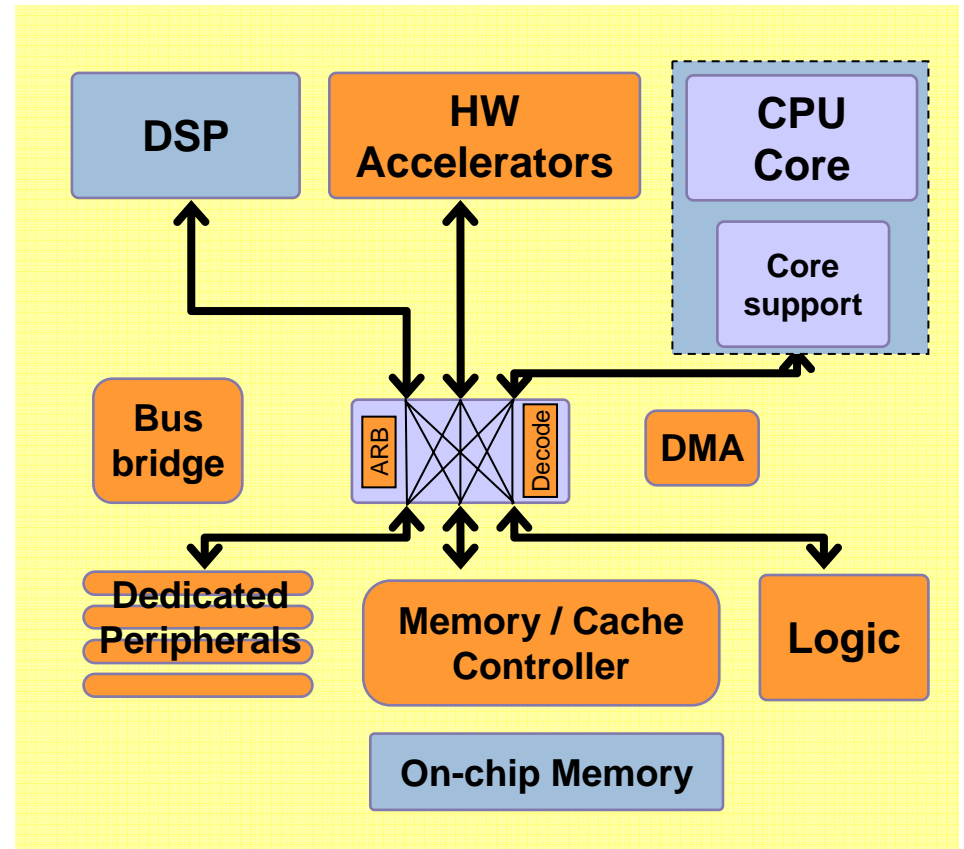


Esterel Studio IP export into SPIRIT flow

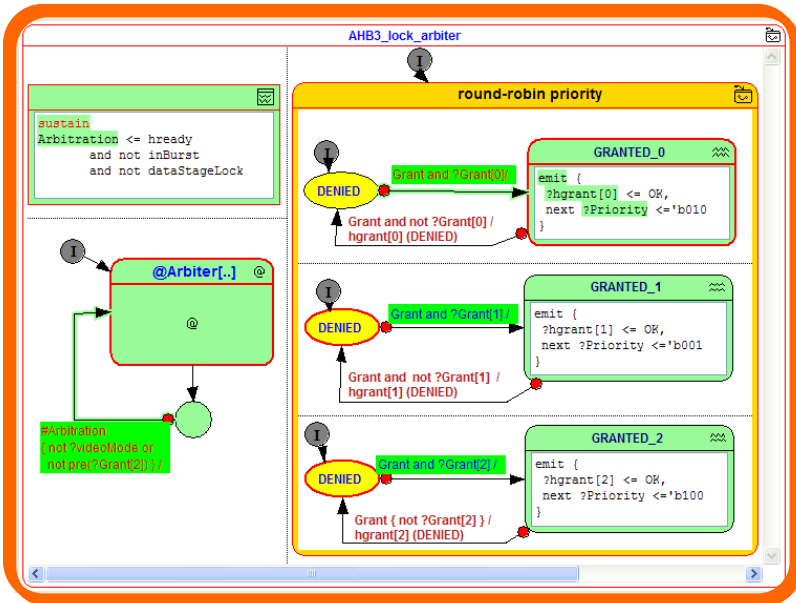
- **Esterel Studio is** a toolset to create and verify IP executable specifications
- **Esterel Studio SPIRIT export** will enable SoC Architects and Designers to:
 - **Export Esterel IP** to the SPIRIT meta-data format for use by other SPIRIT compliant tools
 - **Release configured RTL or SystemC IP** from Esterel Studio highly configurable source
 - **Export debug and verification instrumentation** used when validating Esterel Studio IP to other SoC debug tools

Esterel is an IP specification and design tool

- Esterel Studio suited to IP specification and design for
 - Bus interfaces and peripheral controllers
 - Processor core peripherals
 - Communication IPs
- Esterel Studio Generates
 - Synthesizable VHDL/Verilog RTL
 - SystemC

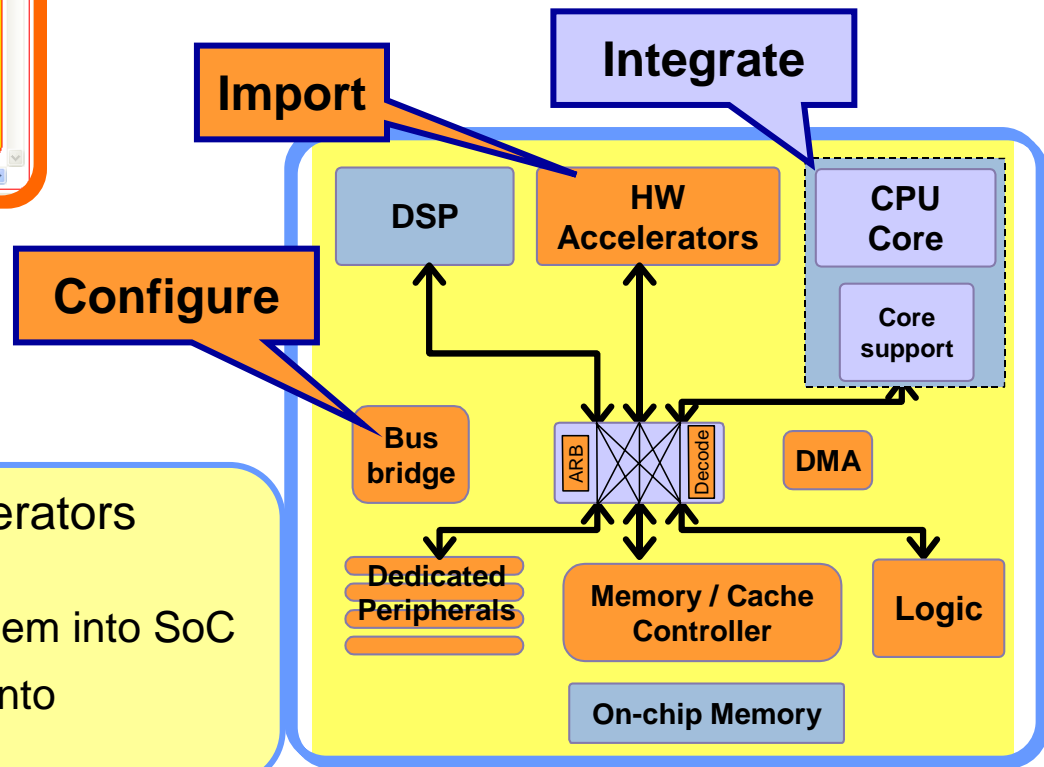


Esterel Studio and SPIRIT complementary features for SoC design



Esterel Studio supports

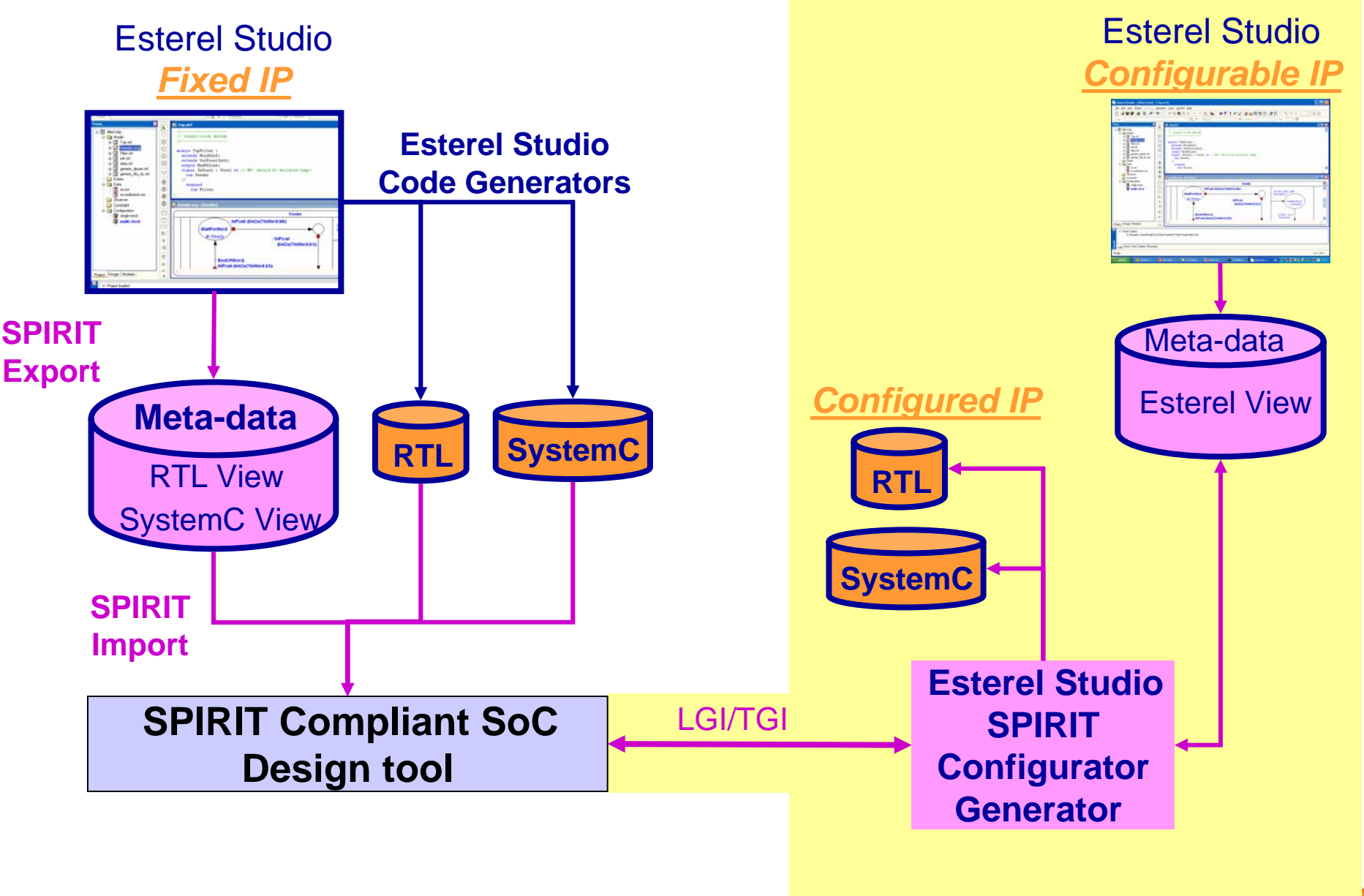
- Formal IP specification
- Complex FSM design and debug
- Configurable and parametric design
- Powerful debug environment (assertion, testbench)



SPIRIT meta data and generators enables customers to

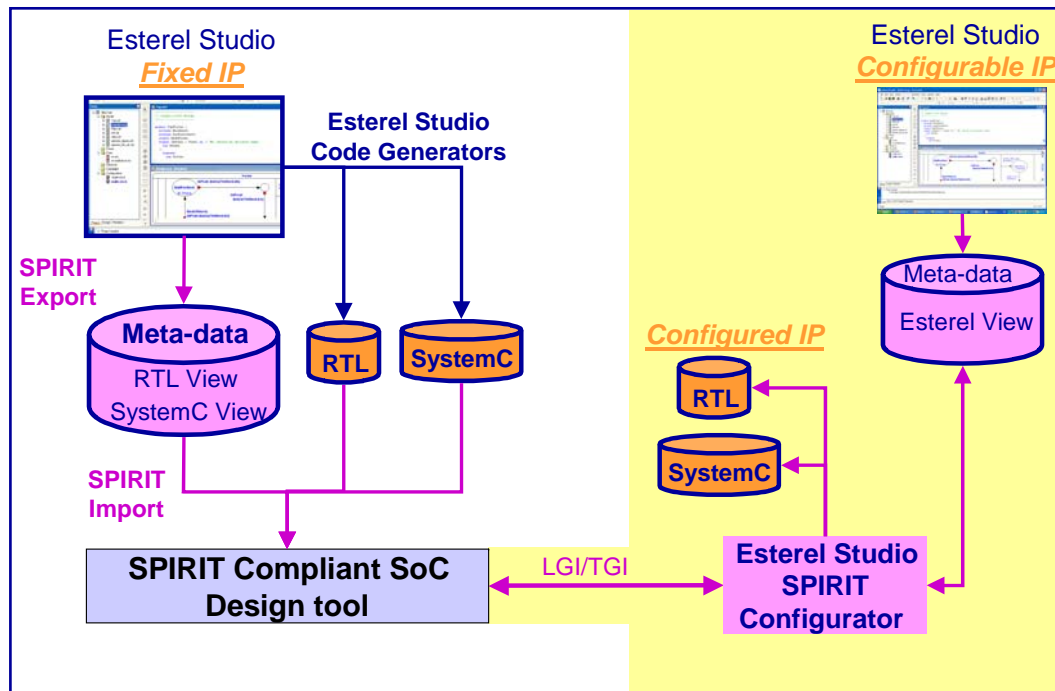
- Configure IP and integrate them into SoC
- Import SPIRIT-compliant IP into SoC design and debug tools

Esterel Studio - SPIRIT flow



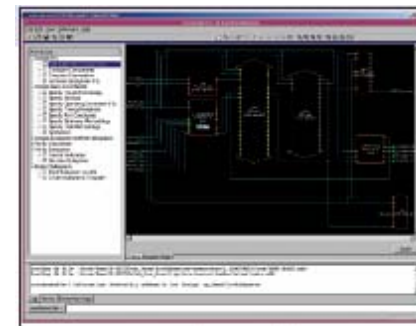
Esterel Studio - SPIRIT interoperability demonstrator

- ▶ Show that Esterel IP integrates into SystemC architecture exploration tool as well as RTL synthesis and layout tool, ...
- ... with guaranteed same behavior



ESL - performance evaluation

IP validation/implementation
SoC integration



coreAssembler

SYNOPSYS®



Esterel - SPIRIT flow roadmap

- First SPIRIT interoperability demonstrator (June '06)
 - SPIRIT 1.2 support
 - RTL Flow
 - Interoperability with EDA partners
 - ARM SOC Designer
 - Synopsys CoreAssembler
 - Candidate demo for DAC'06 (after review by ARM/Synopsys/ET for DAC'06)
- Customer demos and feed-back
- SPIRIT export integration in Esterel Studio 5.4 (2'H06)
 - Need to work on Esterel IP packaging
 - Verification instrumentation (assertions, simulation testbench), and documentation is in the scope
- Support of SPIRIT 2.0 and SystemC export (including Esterel Transactional models) is the next goal