

CCS Technology

Synopsys Interoperability Forum
November 9, 2005

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Vice President of Engineering
Synopsys, Inc.



Composite Current Source (CCS)

Timing

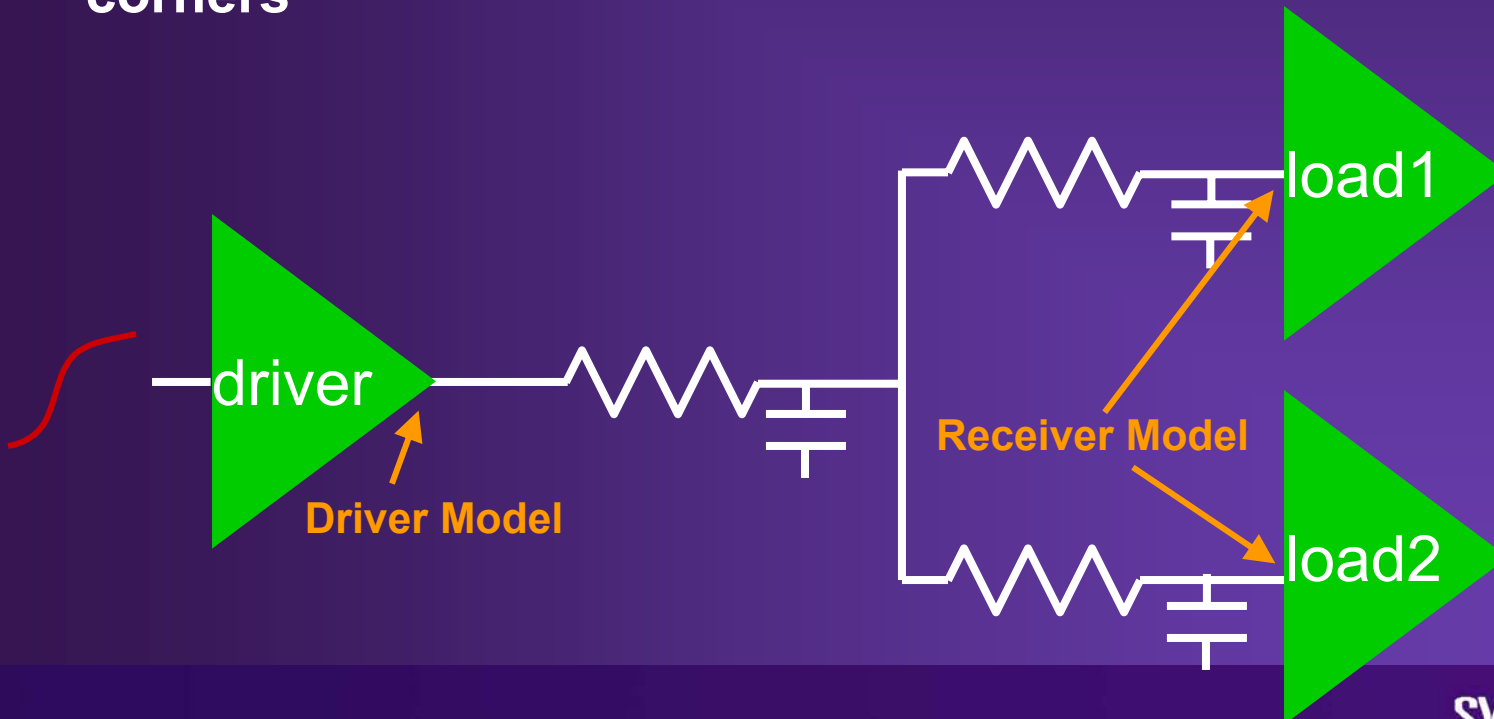
Timing

Noise

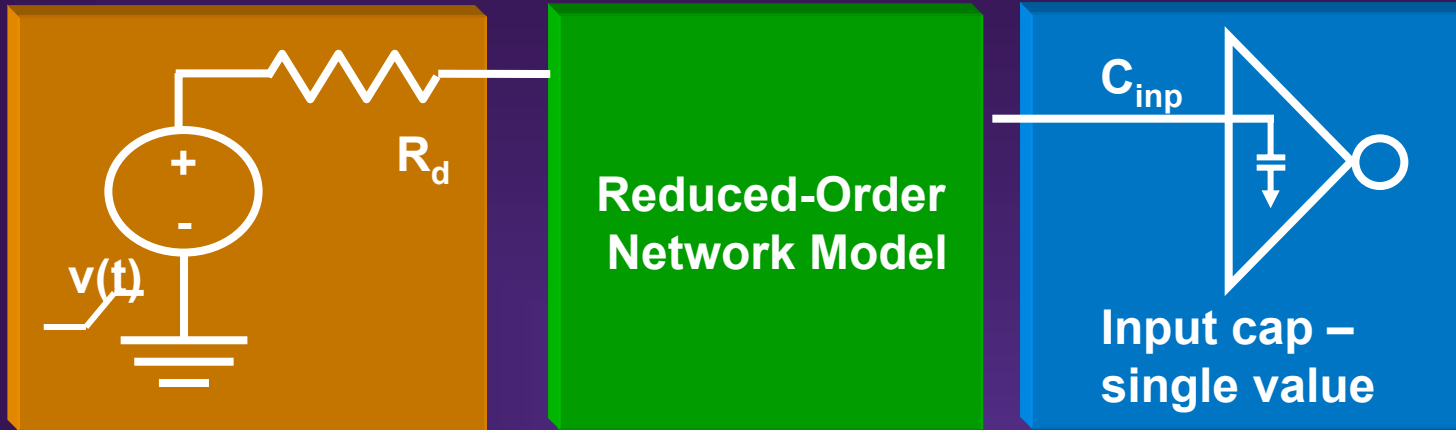
Power

Delay Calculation Requirements

- Driver Model: drive arbitrary interconnect, including high-impedance nets
- Receiver model: complex input capacitance
- Efficient characterization
- V_{dd} & Temperature scaling for IR drop, multi- V_{dd} , DVFS, corners



NLDM Based Driver/Receiver Models



Driver Model

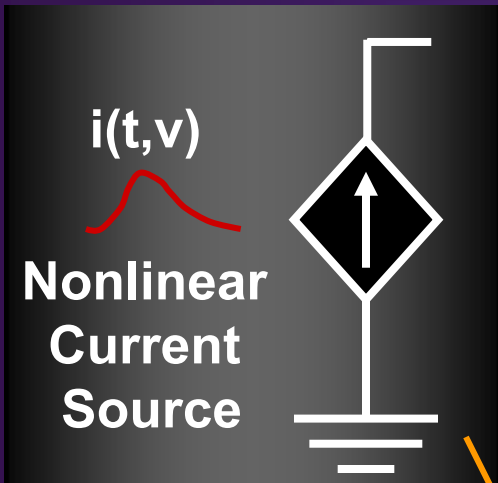
- Ramp voltage source, fixed drive resistance
- Very fast – accurate for most nets
- Limited accuracy for high impedance networks with large drivers (RC-009)

Receiver Model

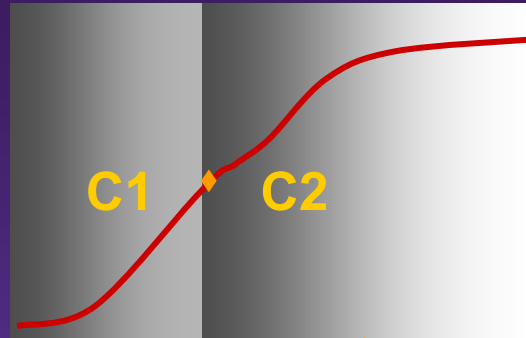
- min/max rise/fall input caps
- Doesn't model capacitance variation during transition

Basics of CCS Timing

Driver model

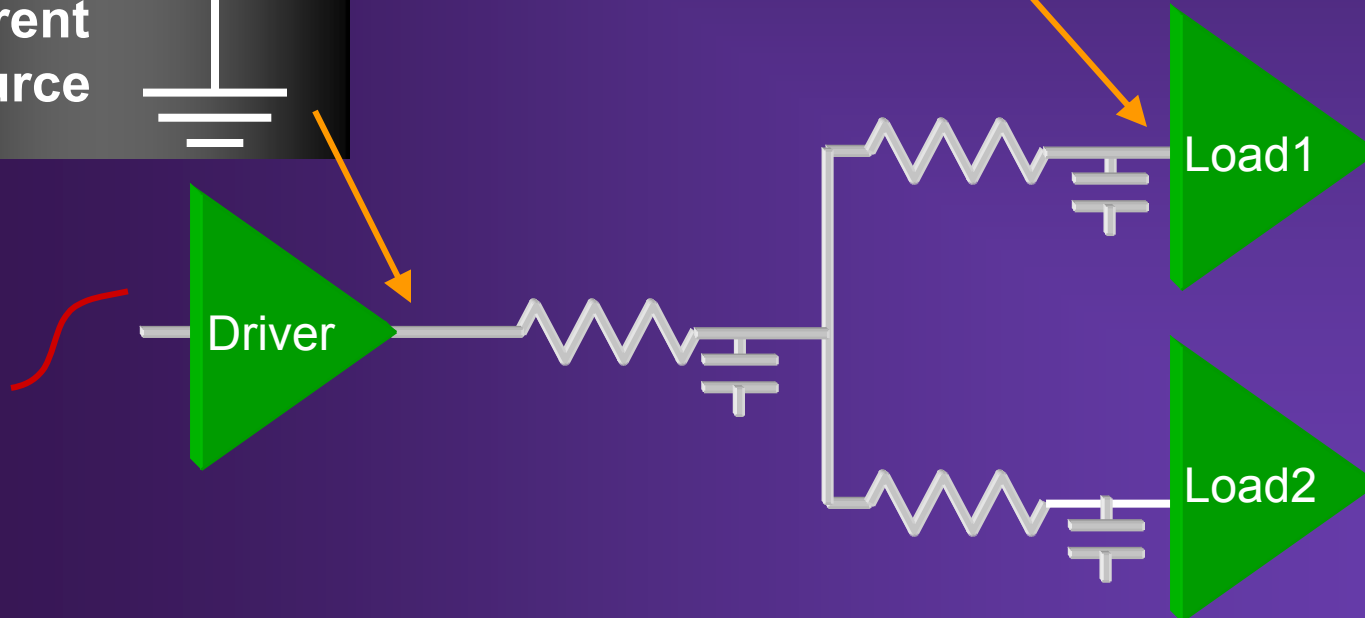


Receiver model



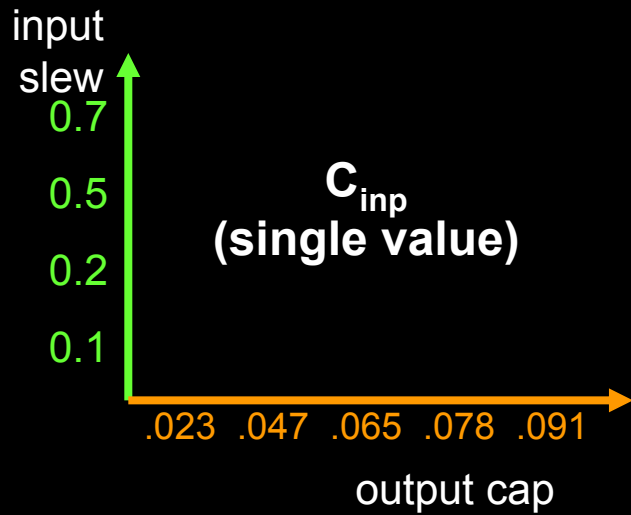
C1, C2 vary with

- ✓ Input slew
- ✓ Output load
- ✓ Rise vs. fall
- ✓ State of cell

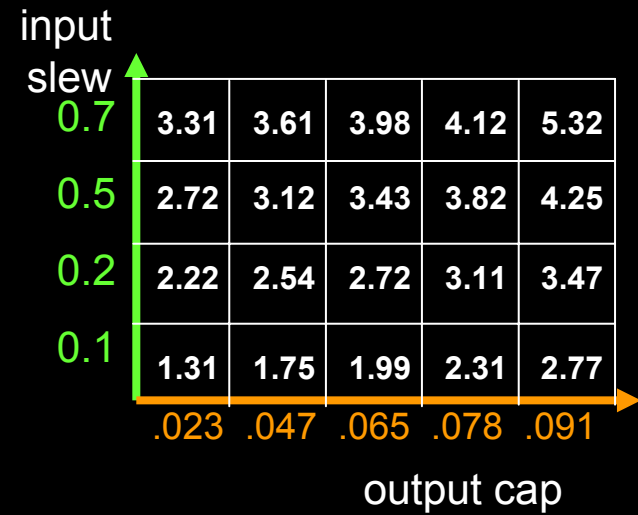


Characterization for NLDM

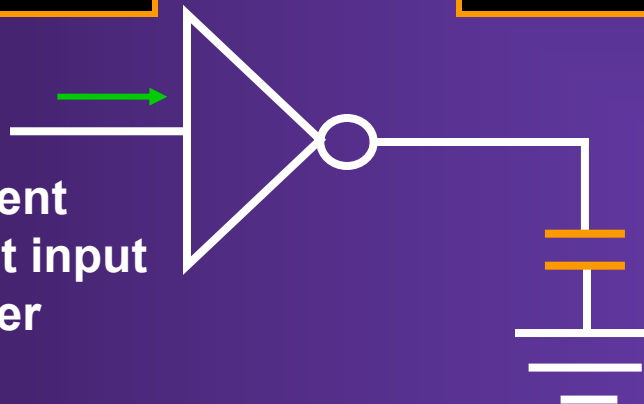
Pin Capacitance



Cell Delay / Slew Tables

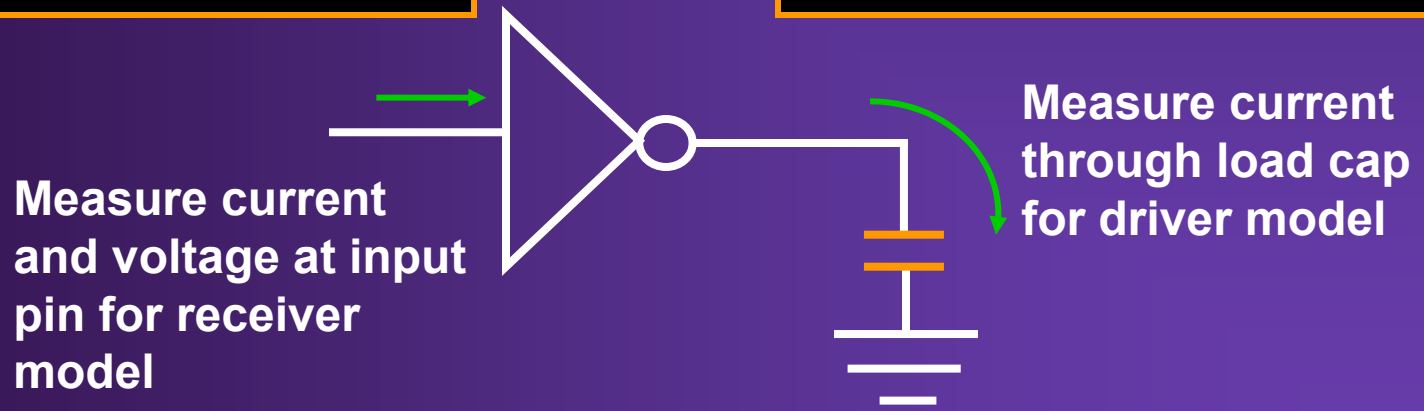
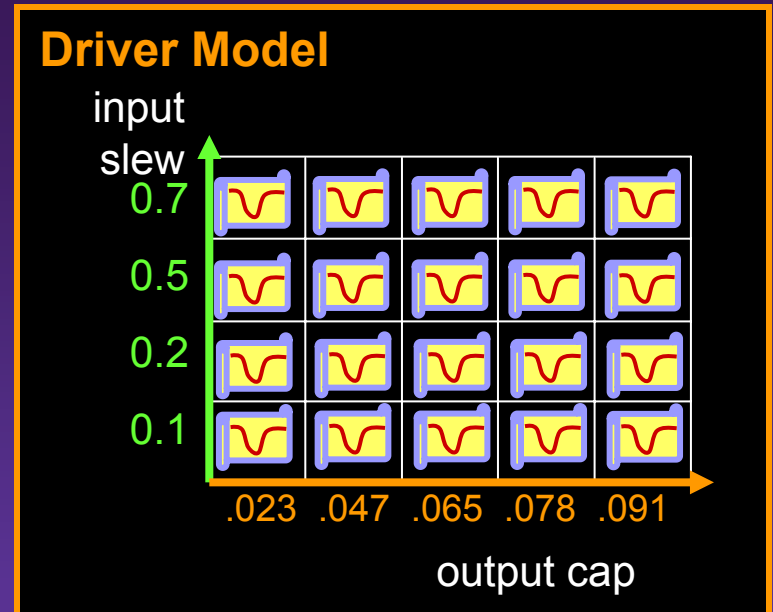
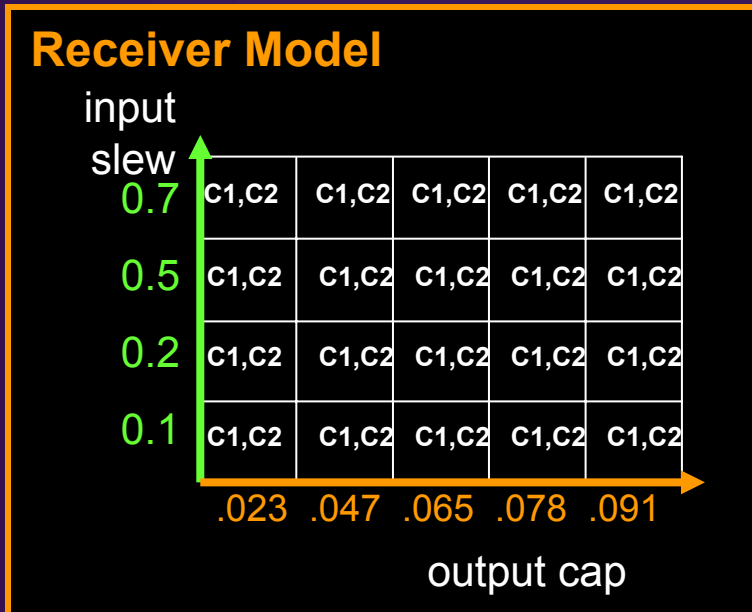


Measure current and voltage at input pin for receiver model

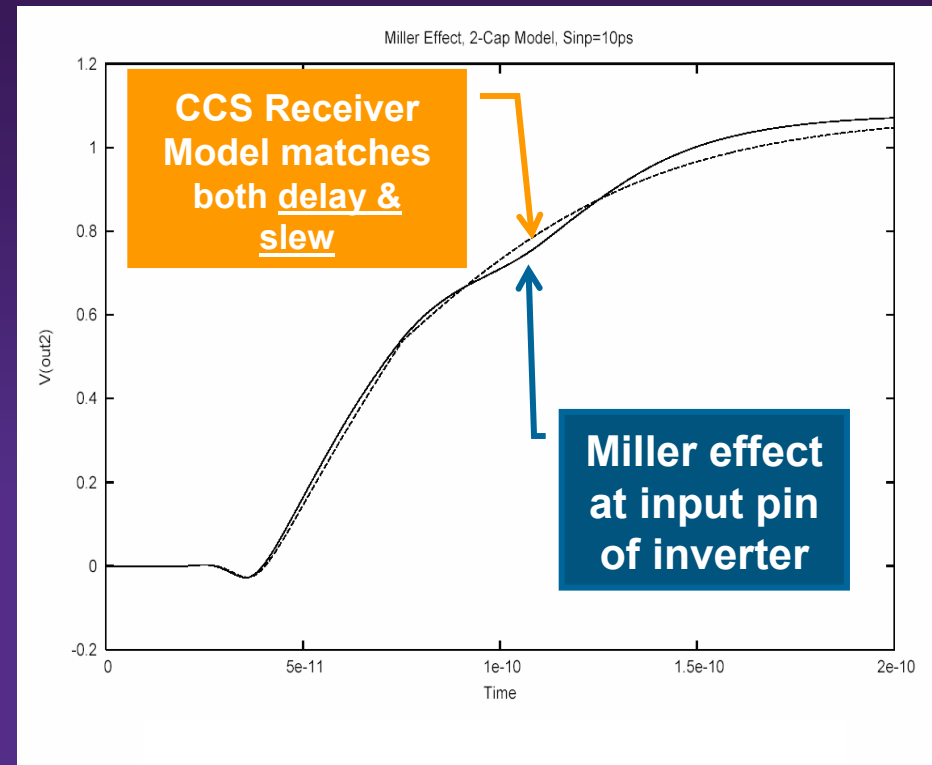
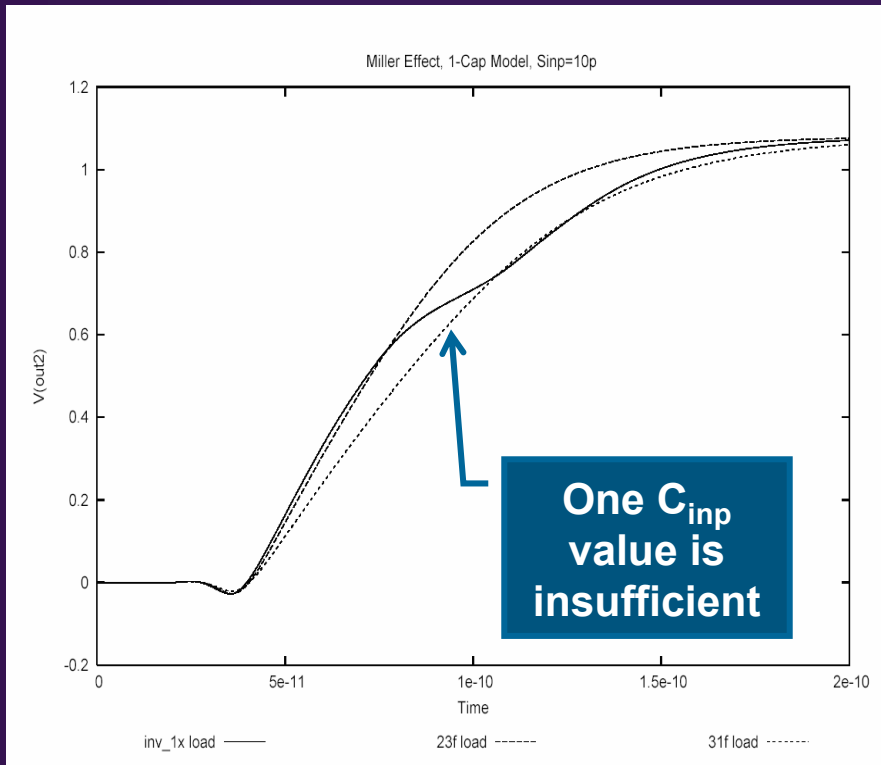


Measure cell delay and output slew

Characterization for CCS Timing

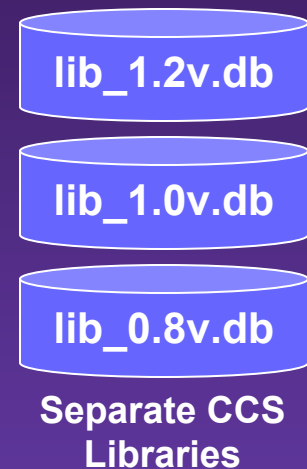


CCS Receiver Model Advantage



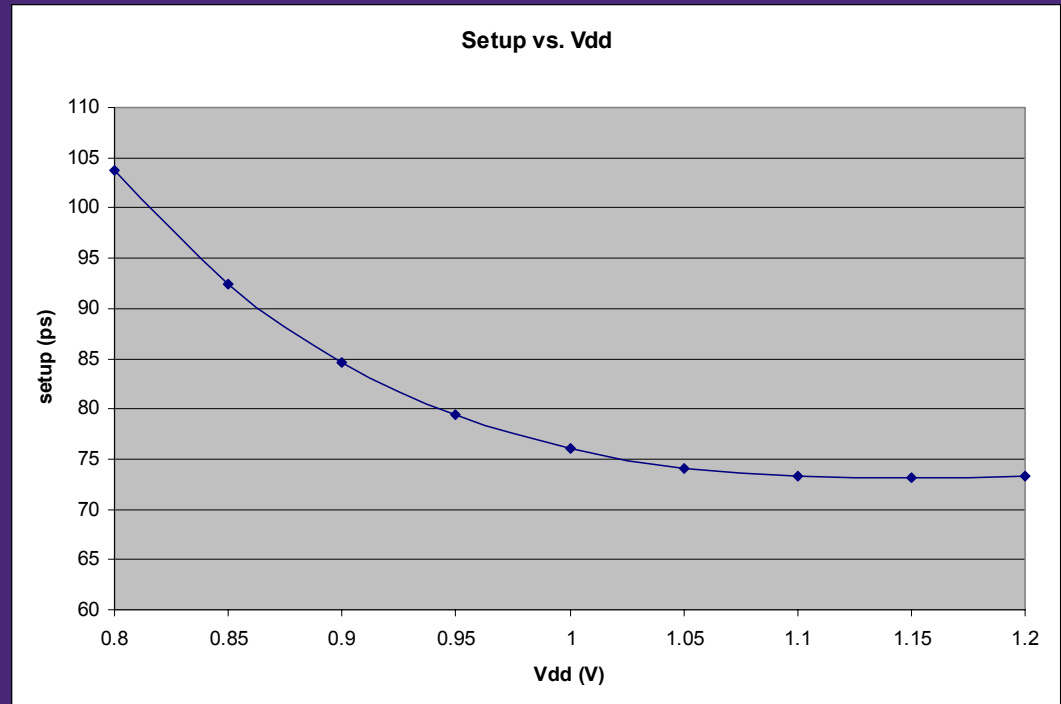
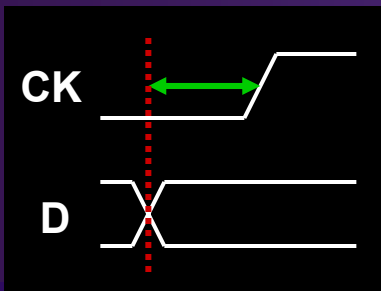
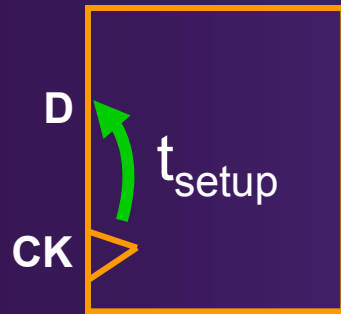
V_{dd} and Temperature

- CCS Timing enables high accuracy delay calculation for wide range of V_{dd} and Temperature
- For power-aware design styles:
 - Single V_{dd}
 - Multiple V_{dd}
 - Dynamic Voltage & Frequency Scaling (DVFS)
- Advanced analysis including IR Drop effects
- What is scaled:
 - Driver model
 - Receiver model
 - Timing constraints: setup, hold, recovery, removal, MPW
- Straightforward characterization



Constraint Arcs: V_{dd} & Temperature

- Constraint arc (timing check) values depend on V_{dd} and Temperature
- CCS Timing supports nonlinear scaling of constraint arcs

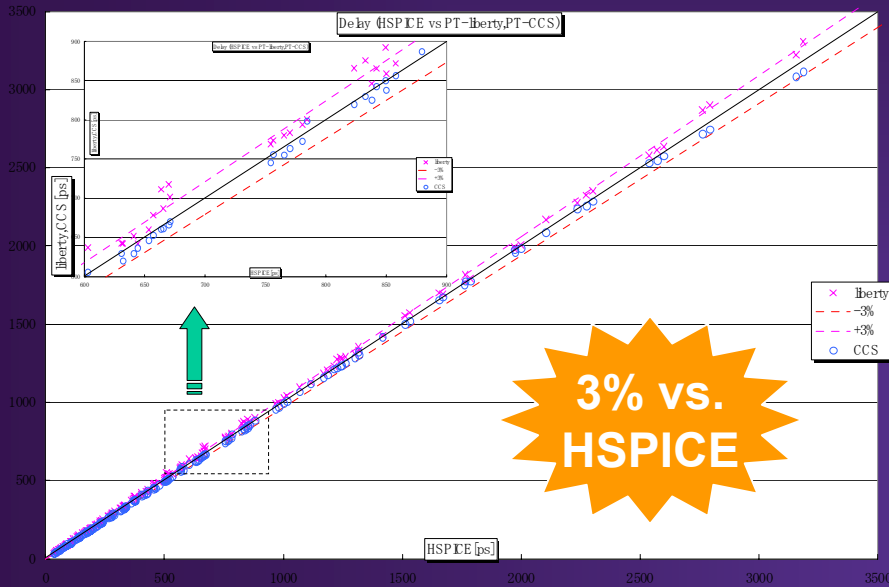


CCS Timing Results



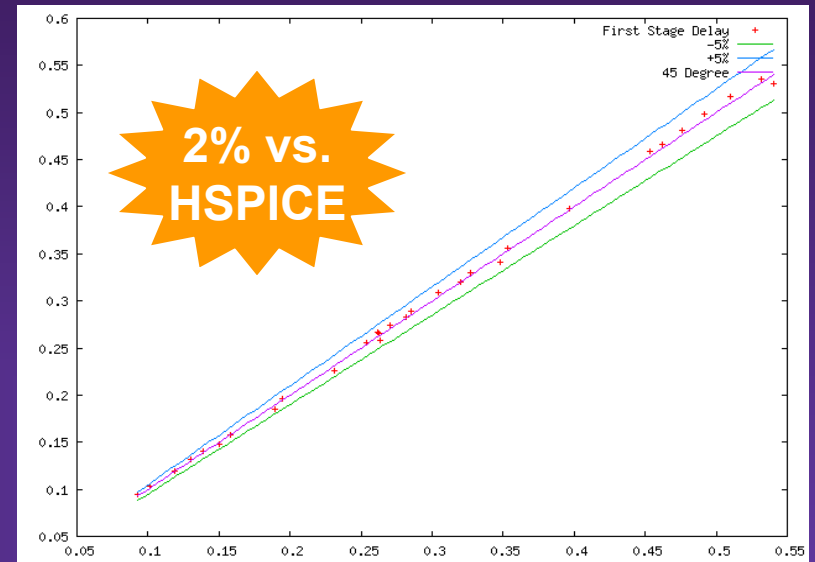
Results: STARC, TSMC

STARC



**PrimeTime2004.12 with STARC
90nm CCS liberty libraries
Error : < 3% vs. HSpice**

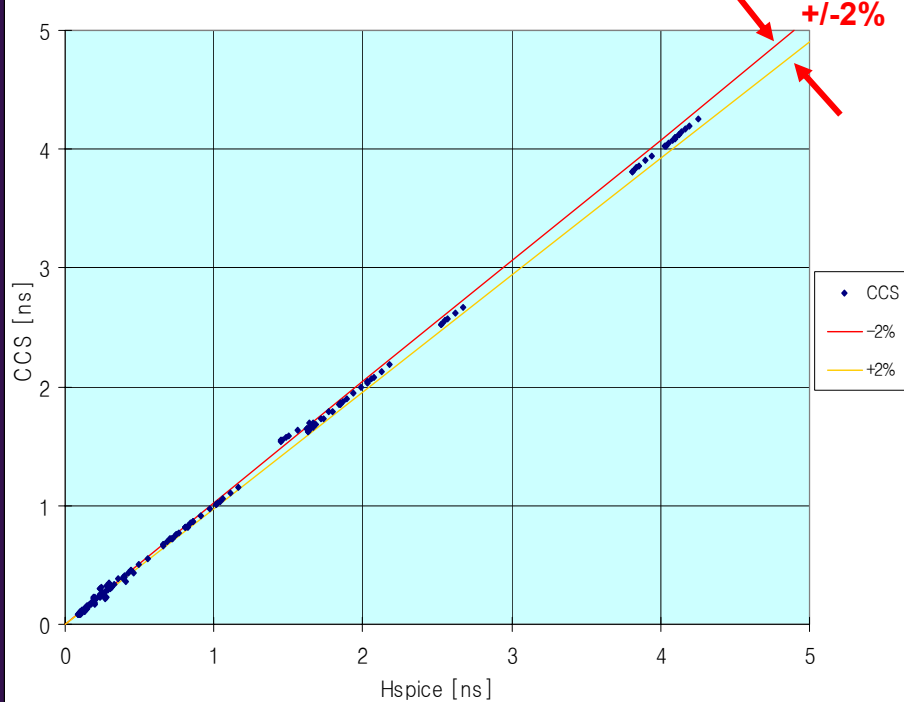
Major Foundry



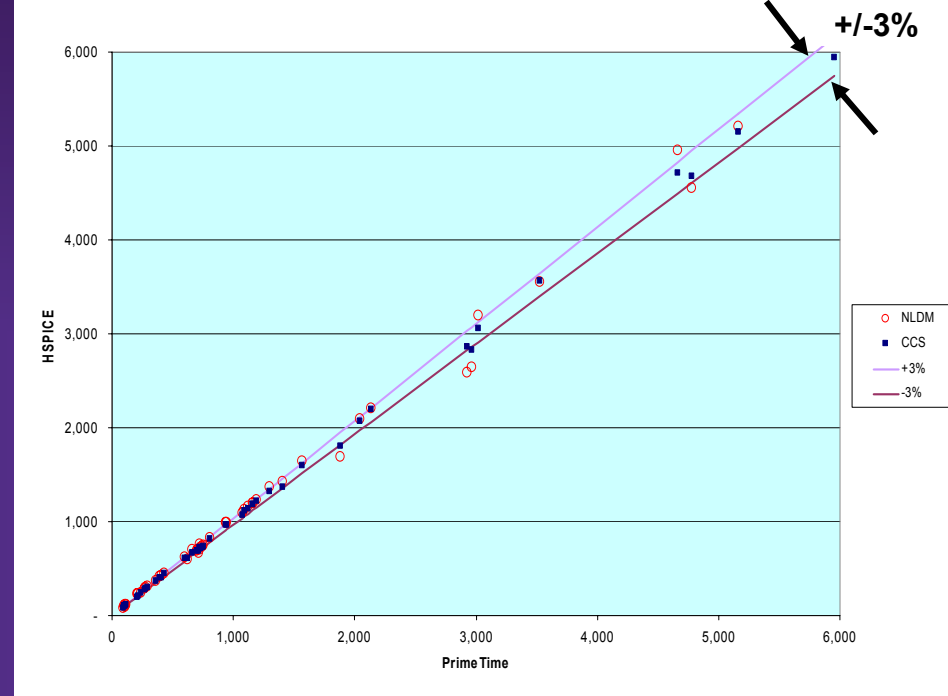
**PrimeTime2005.06 with 90nm
CCS liberty libraries
Error : < 2% vs. HSpice**

Customers Demonstrate CCS Accuracy

CCS Accuracy vs. HSPICE



CCS & NLDM vs. HSPICE



90nm Library
Major Electronics Firm in Asia

65nm Library
Leading Global IDM

CCS Timing Summary

- **High accuracy delay and slew calculation**
 - **Advanced driver and receiver modeling**
 - **Results within 2% of SPICE**
 - **Powerful scaling for Vdd and Temperature**
- **No impact on analysis runtime**
- **Easy and efficient characterization**
- **Industry Support**
 - **ARM, TSMC, Virage Logic, STARC, Library Technologies, Synopsys NanoChar**

Composite Current Source (CCS)

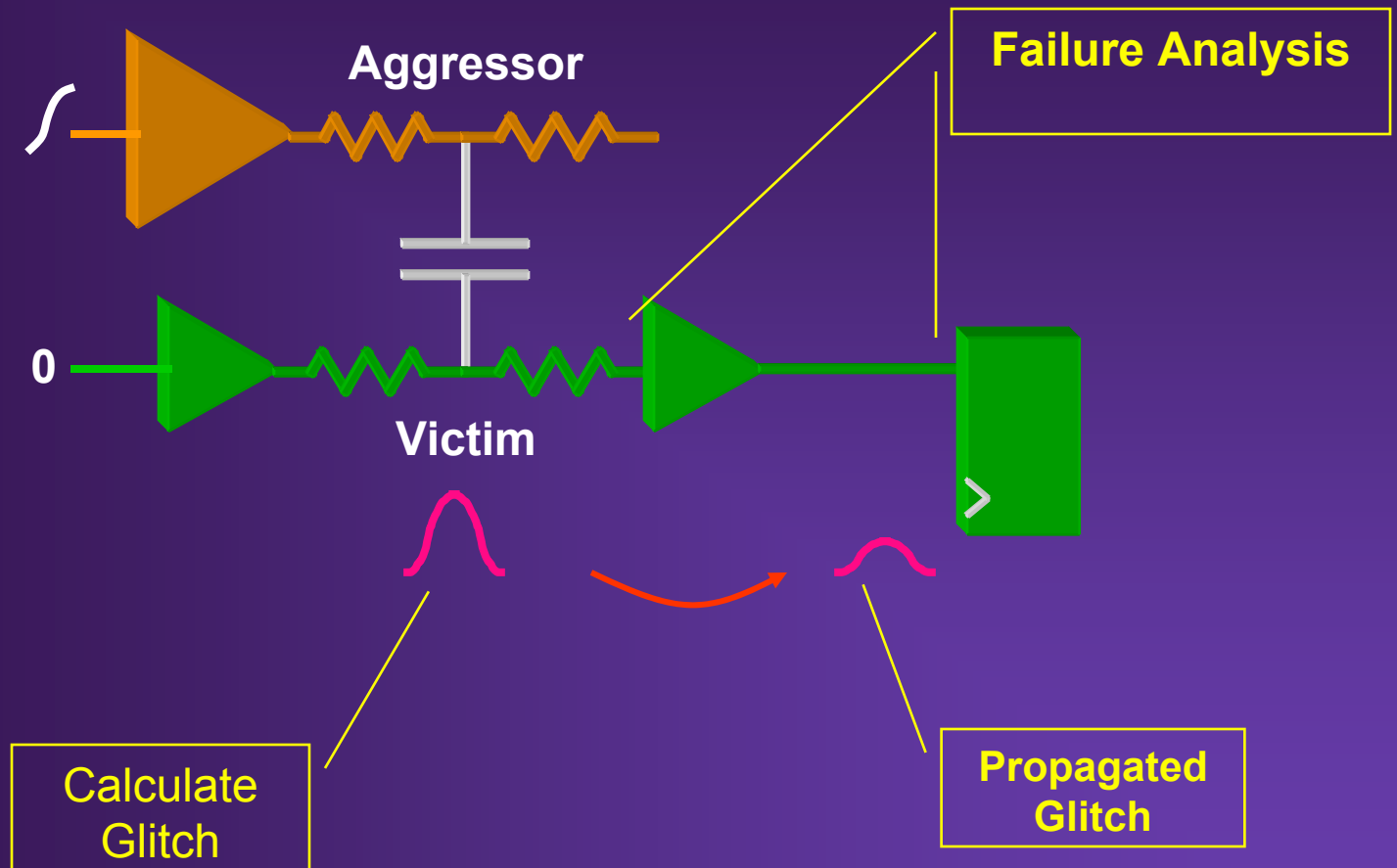
Noise

Timing

Noise

Power

Noise Analysis



Noise Modeling Requirements

- **Accurate model to support:**
 - **Noise bump calculation**
 - **Noise propagation**
 - **Driver weakening (combination of propagated and injected bumps)**
 - **Vdd and Temperature scaling**
- **Characterization should be fast and cover a broad set of cell types**
- **Model must enable efficient calculation in analysis and implementation tools**

NLDM Noise Modeling in Liberty

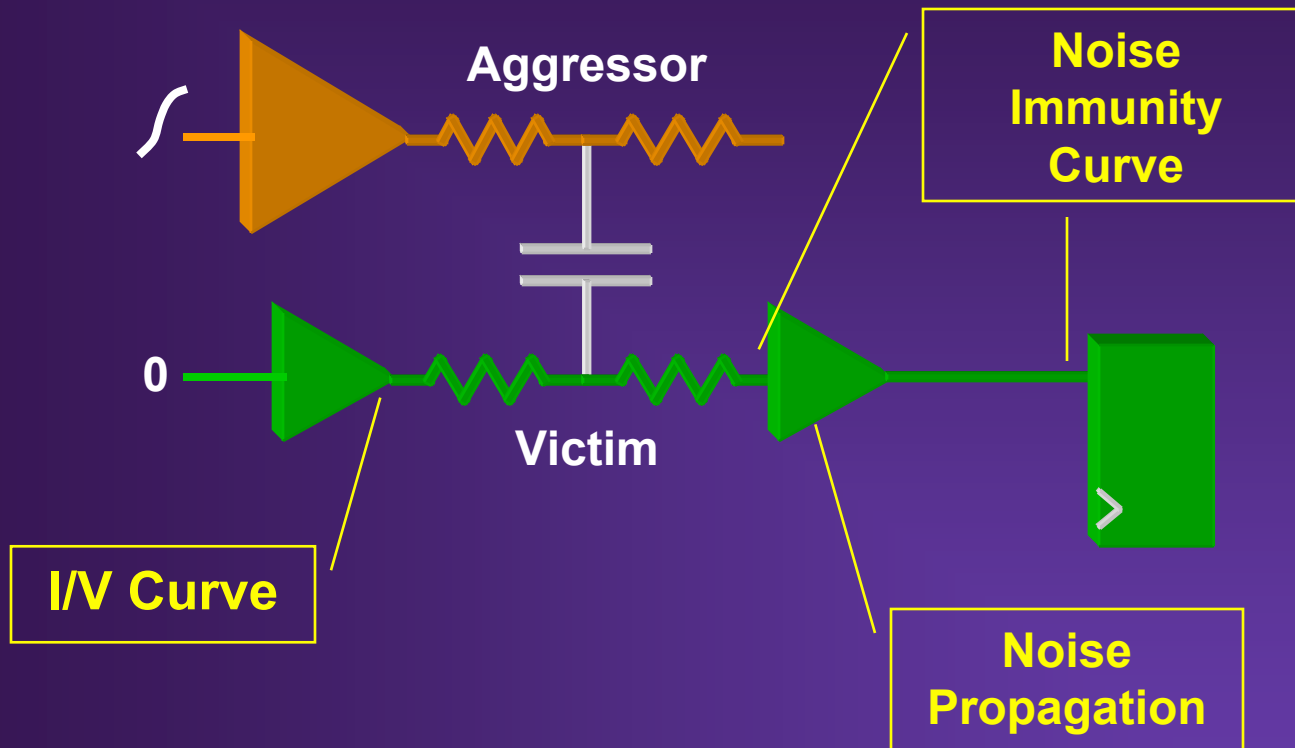
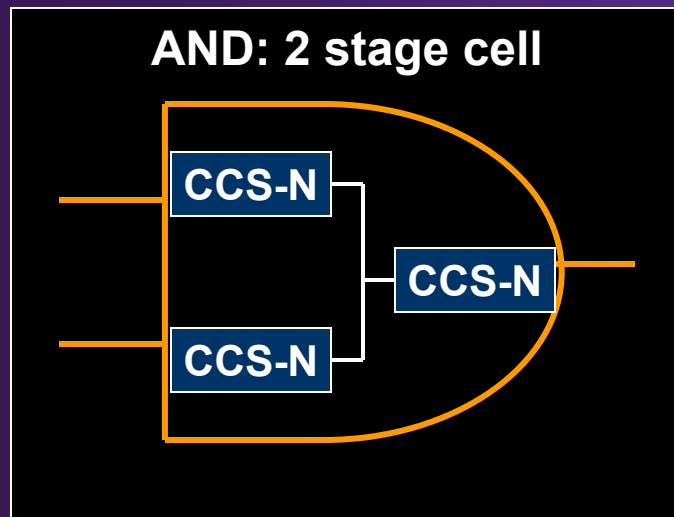
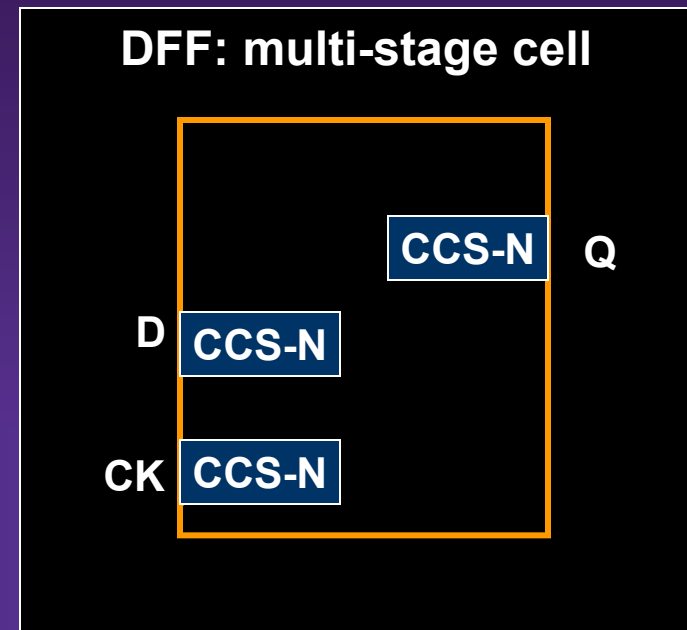
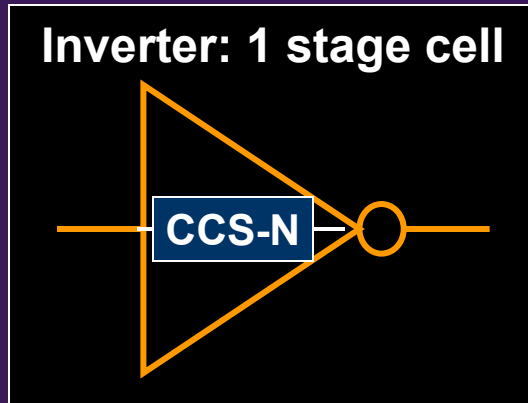


Table-based noise immunity and propagation characterization require extensive circuit simulation

Introducing CCS Noise

- **Faster Characterization:**
 - **100X faster characterization vs. NLDM Noise**
 - Much less circuit simulation is needed
 - **Typical 90nm library in under 4 hours on 10 cpus**
- **High Accuracy:**
 - **Accurately models noise propagation and driver weakening**
 - **Accurate voltage and temperature scaling using the same scaling mechanism as CCS Timing**
 - **Same accurate receiver modeling as CCS Timing**

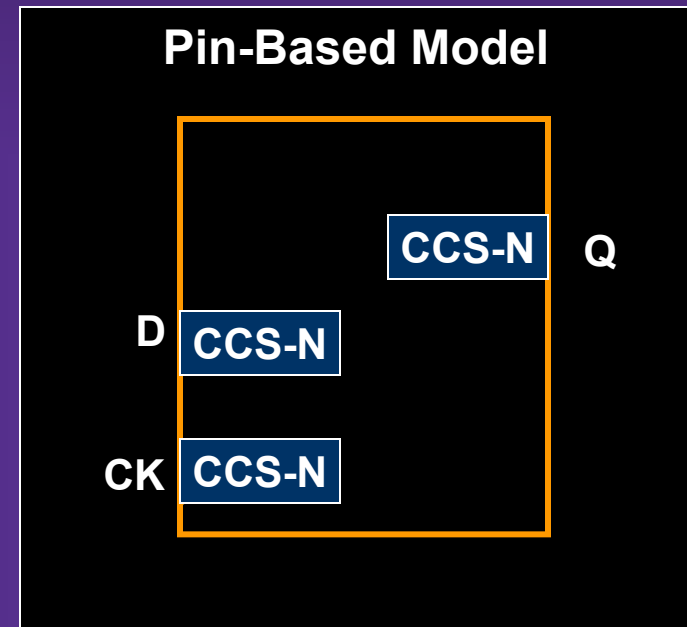
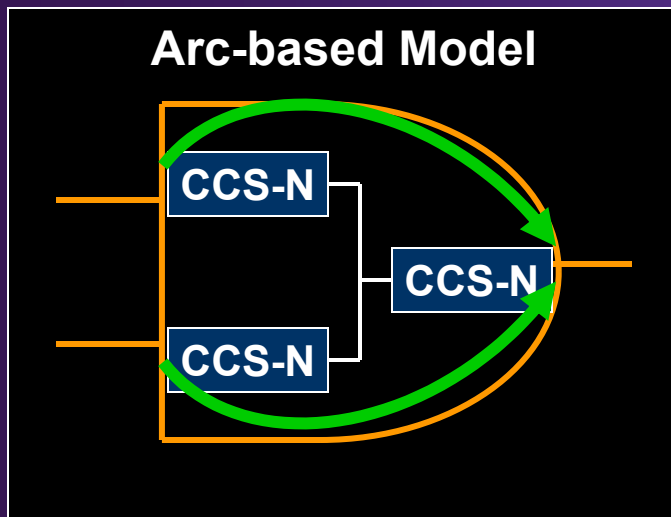
CCS Noise: Cell Model



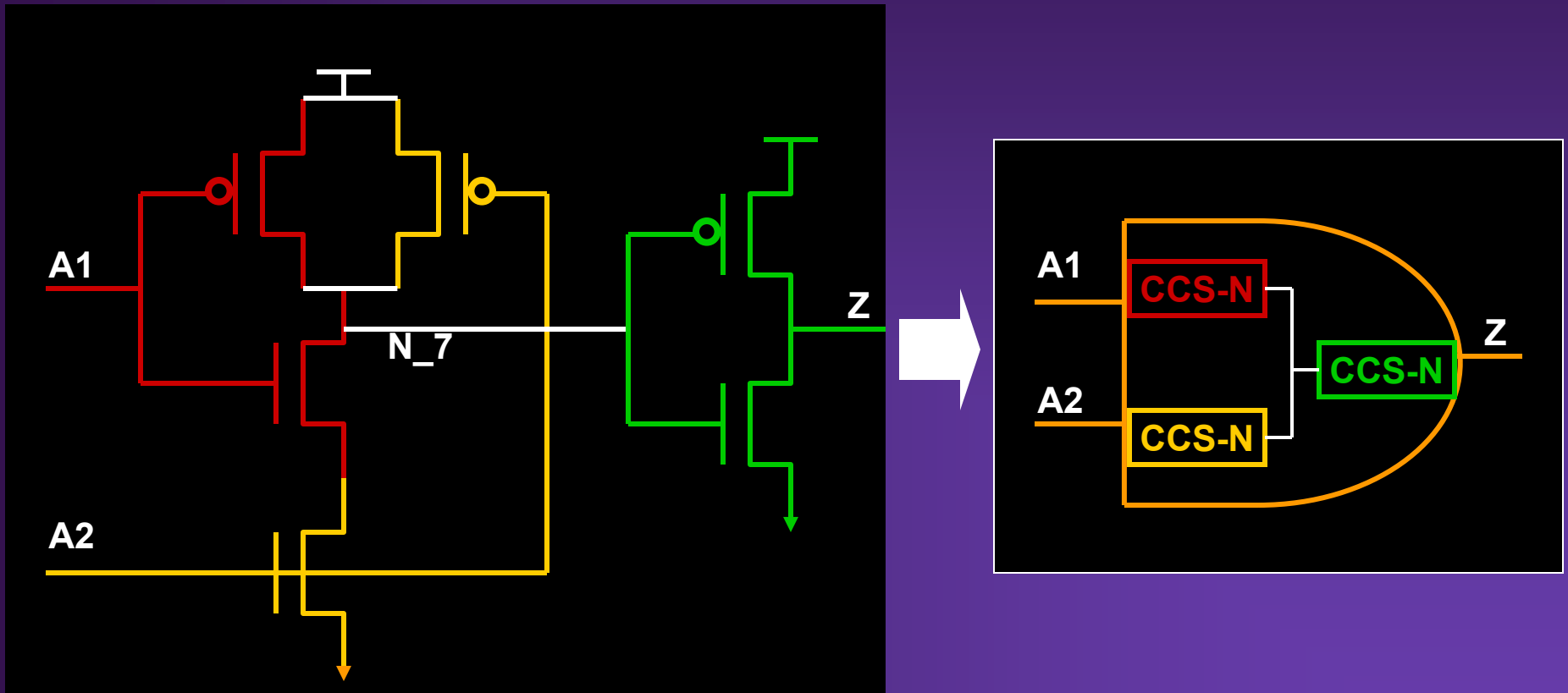
- **First and last transistor stages are modeled**

Arc and Pin CCS Noise Models

- Input stage: Noise immunity
- Output stage: Driving strength
- Arc: Immunity + Driving Strength + Noise Propagation
 - For paths of one or two stages



Arc-Based Example: AND2



AND2 – Liberty Syntax

```
pin(Z) {
  direction : output;
  ...
  timing() {
    related_pin      : "A1";
    ccsn_first_stage() { /* A1 to N_7 */
      ...
    }
    ccsn_last_stage() { /* N_7 to Z */
      ...
    }
  }
  timing() {
    related_pin      : "A2";
    ccsn_first_stage() { /* A2 to N_7 */
      ...
    }
    ccsn_last_stage() { /* N_7 to Z, copy of the above */
      ...
    }
  }
}
```

CCS Noise Stage Contents

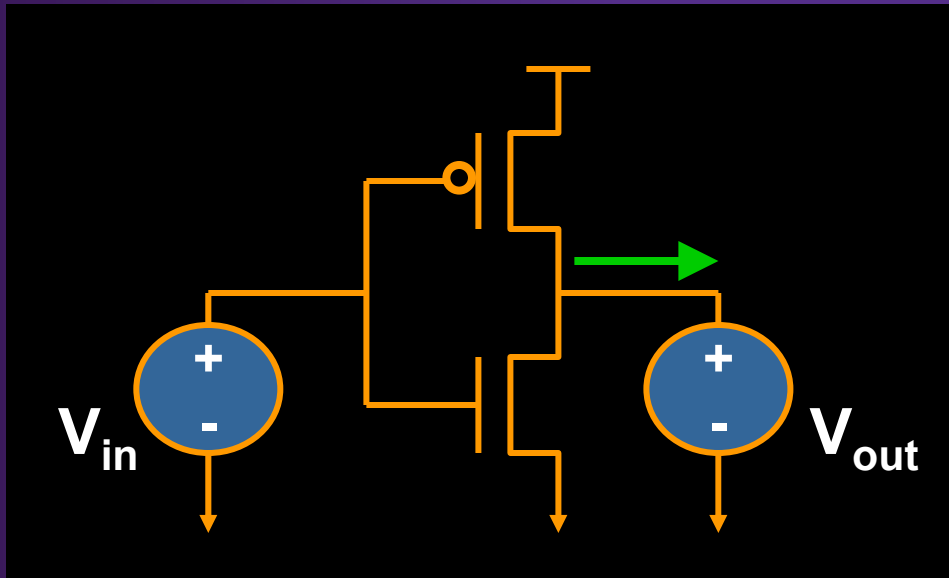
Each CCS Noise stage has three components:

CCS Noise stage

1. DC Current Table
2. Dynamic Behavior Information
3. Parameters

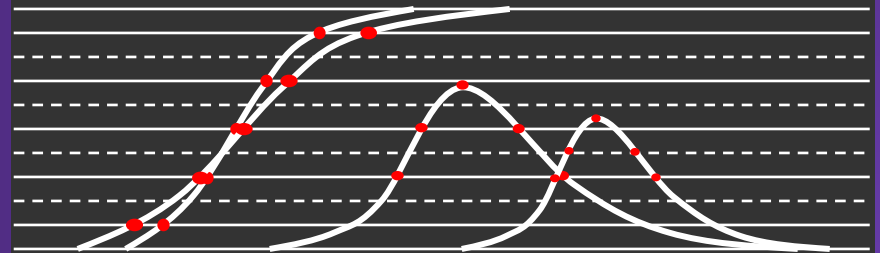
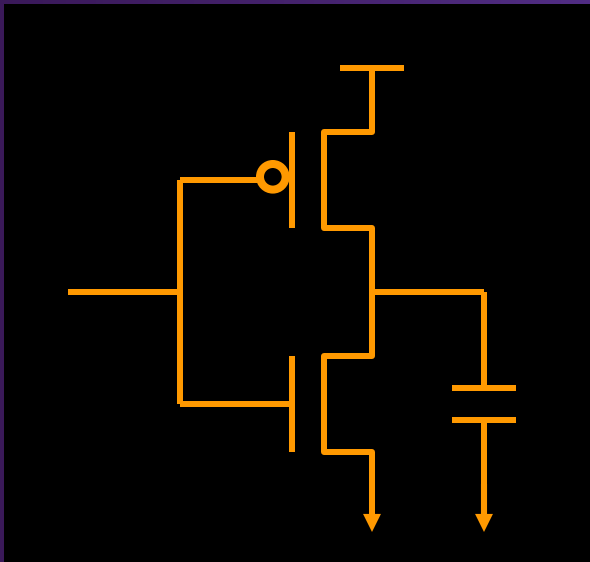
Characterization: DC Current Table

- DC Current table represents output current as a function of two variables
 - V_{in} : Input voltage
 - V_{out} : Output voltage
- A fast DC sweep simulation is used to capture data



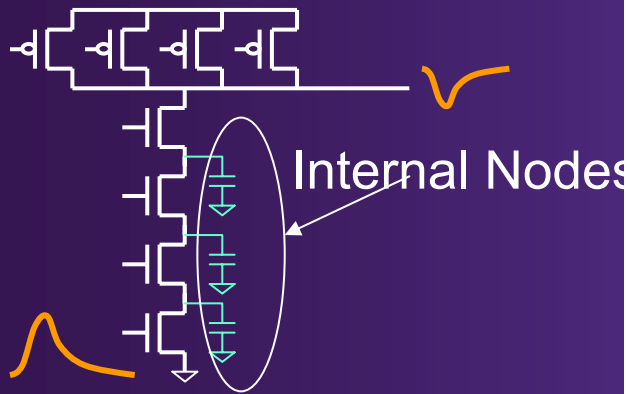
Characterization: Dynamic Behavior

- **Small number of transient simulation runs**
 - **Inputs: A few ramps and a few glitches**
 - **Output response is used to derive the dynamic behavior of the stage**

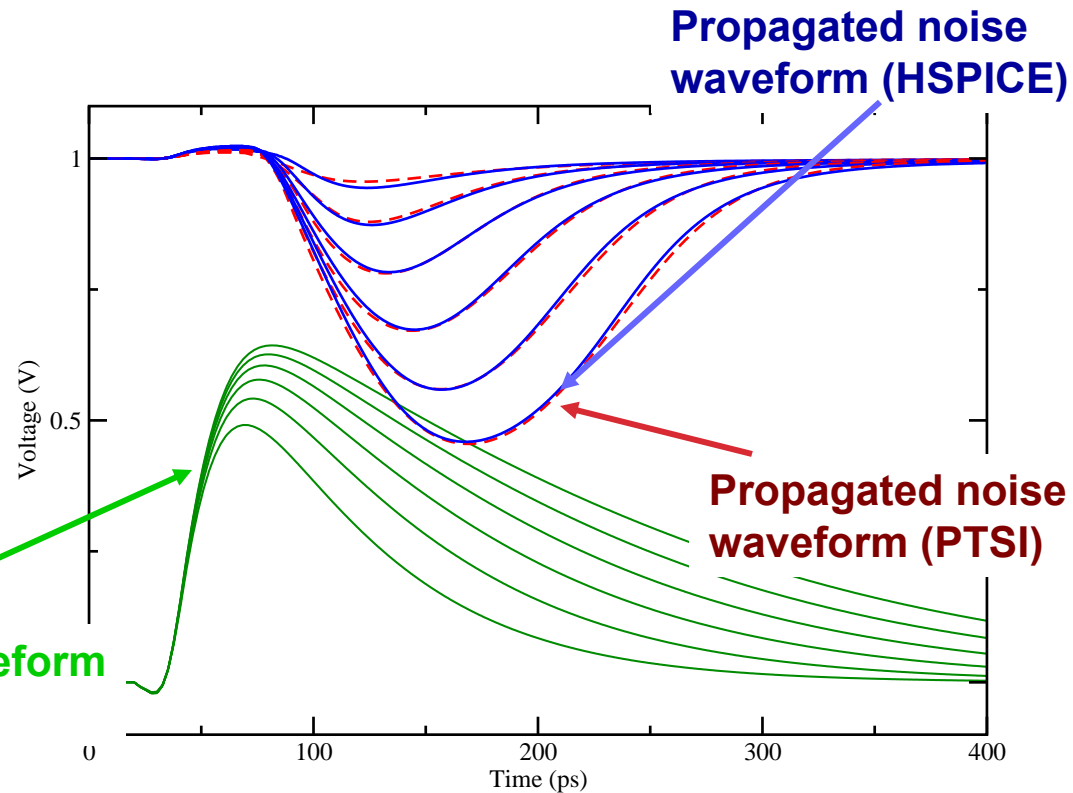


Noise Propagation Accuracy

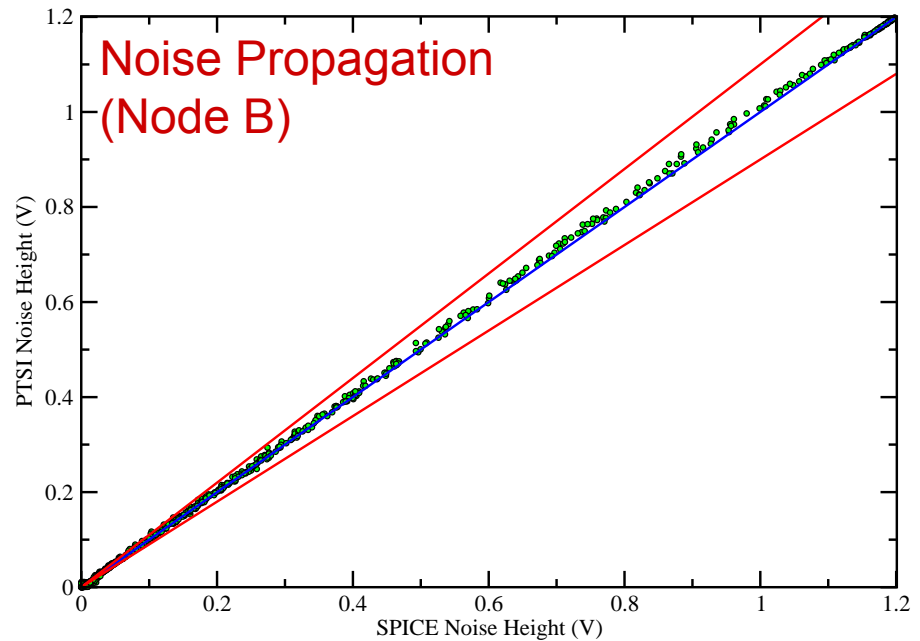
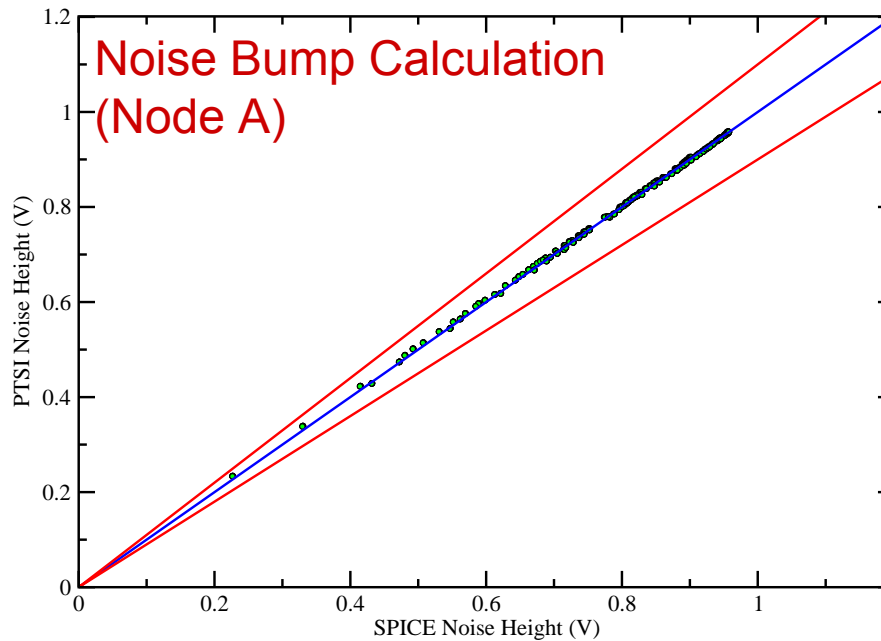
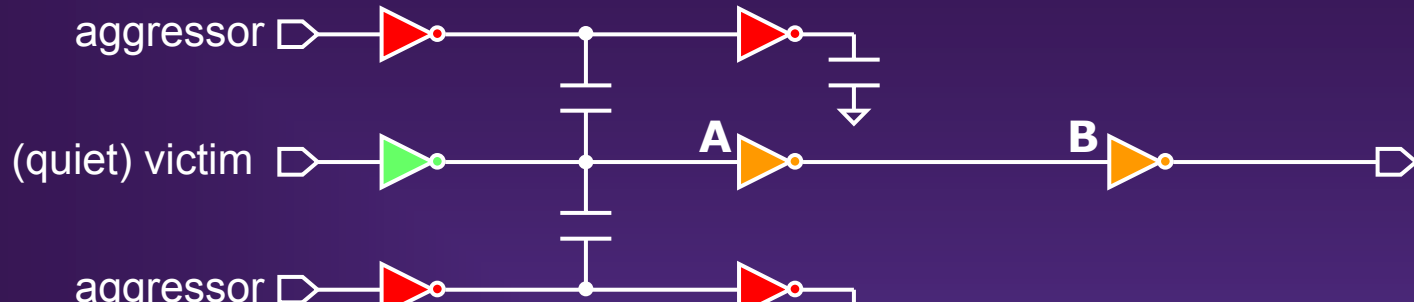
- CCS Noise accurately models dynamic effects such as the impact of charging/discharging of internal nodes



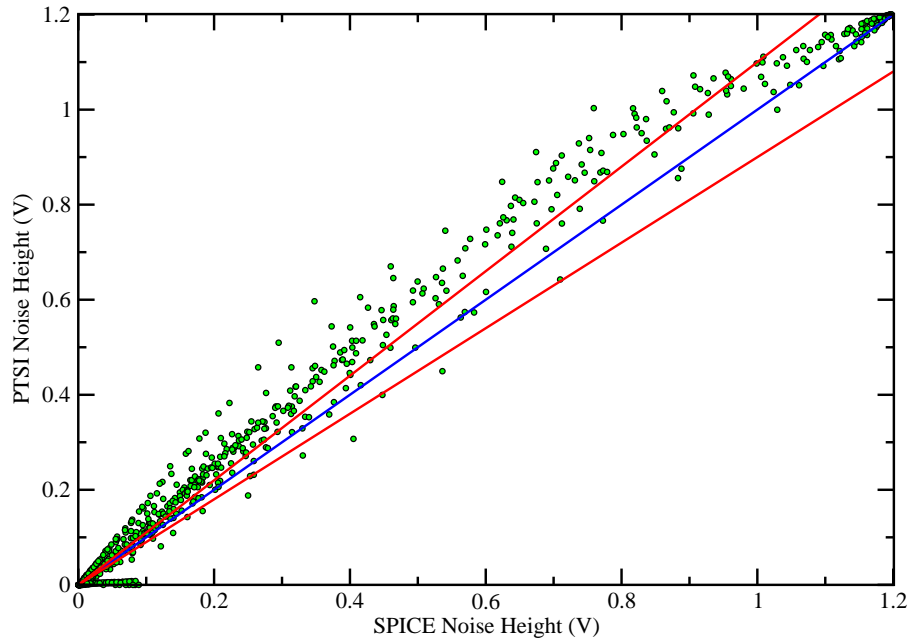
Input noise waveform (HSPICE)



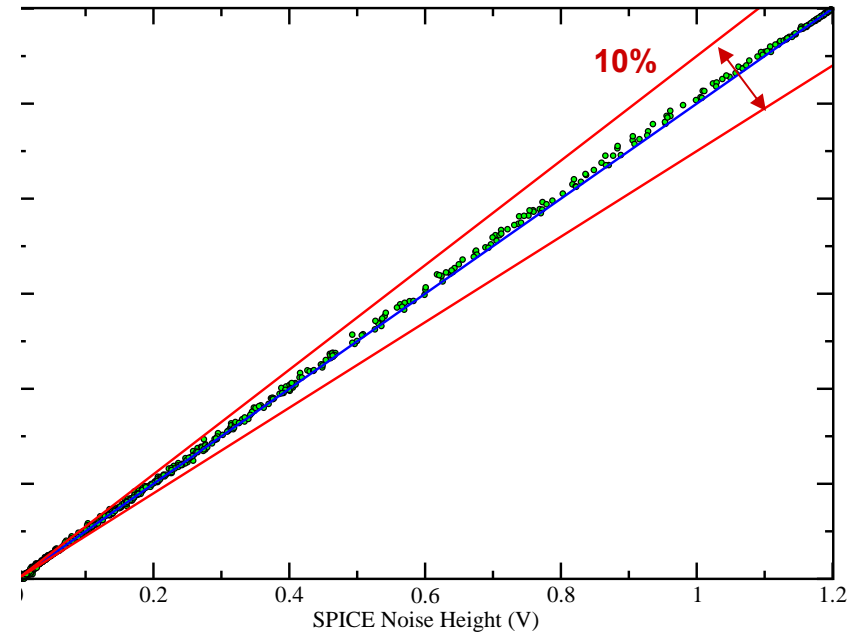
CCS Noise Bump Height Correlation



Noise Propagation Correlation



NLDM Noise



CCS Noise

CCS Noise – Fast Characterization

Library Technology	Number of cells	Characterization time on 10 CPUs
Lib1 90-nm	595	1.5 hrs
Lib2 90-nm	747	2 hrs
Lib3 90-nm	593	4 hrs
Lib4 90-nm	541	1 hr
Lib5 90-nm	1304	4 hrs
Lib6 65-nm	766	3 hrs

CCS Noise Summary

- **Very good customer beta test results**
- **Fast characterization**
 - **Typical library in under 4 hours on 10 cpus**
 - **For large blocks, only need to characterize boundary stages**
- **Fast calculation – no measurable overhead during noise analysis**
- **High Accuracy**
 - **Noise propagation and driver weakening**
 - **Voltage and temperature scaling**

Composite Current Source (CCS)

Power

Timing

Noise

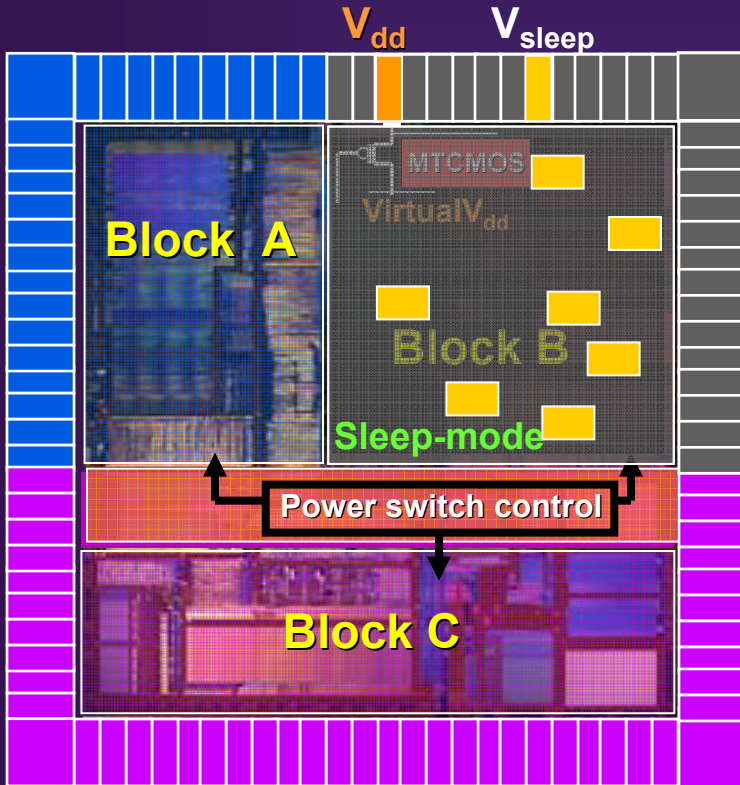
Power

Power Library Requirements

- **Address needs of Multi-Voltage designs**
 - **Multi-Rail cells (Vdd, Vss)**
 - **Non-zero ground rail**
 - **MTCMOS (power gating)**
- **Static and dynamic rail analysis**
 - **Support accurate voltage (IR) drop calculation**
- **Single library / model for all power related applications**
- **Fast and easy library characterization**

Power Gating (MTCMOS)

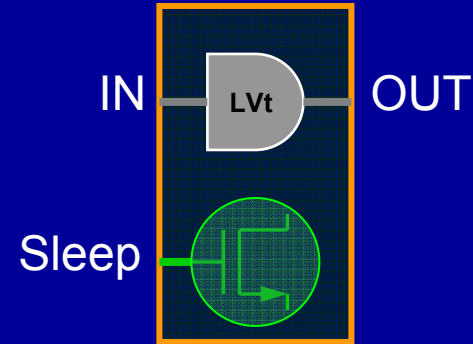
Reduce Leakage by turning block off



Challenge: Analyze “in-rush current” when block turns on

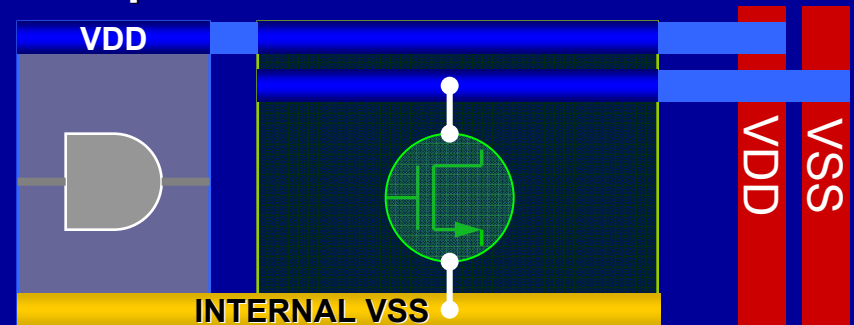
Fine Grain:

Sleep transistor within each cell



Coarse Grain:

Sleep transistor for entire block

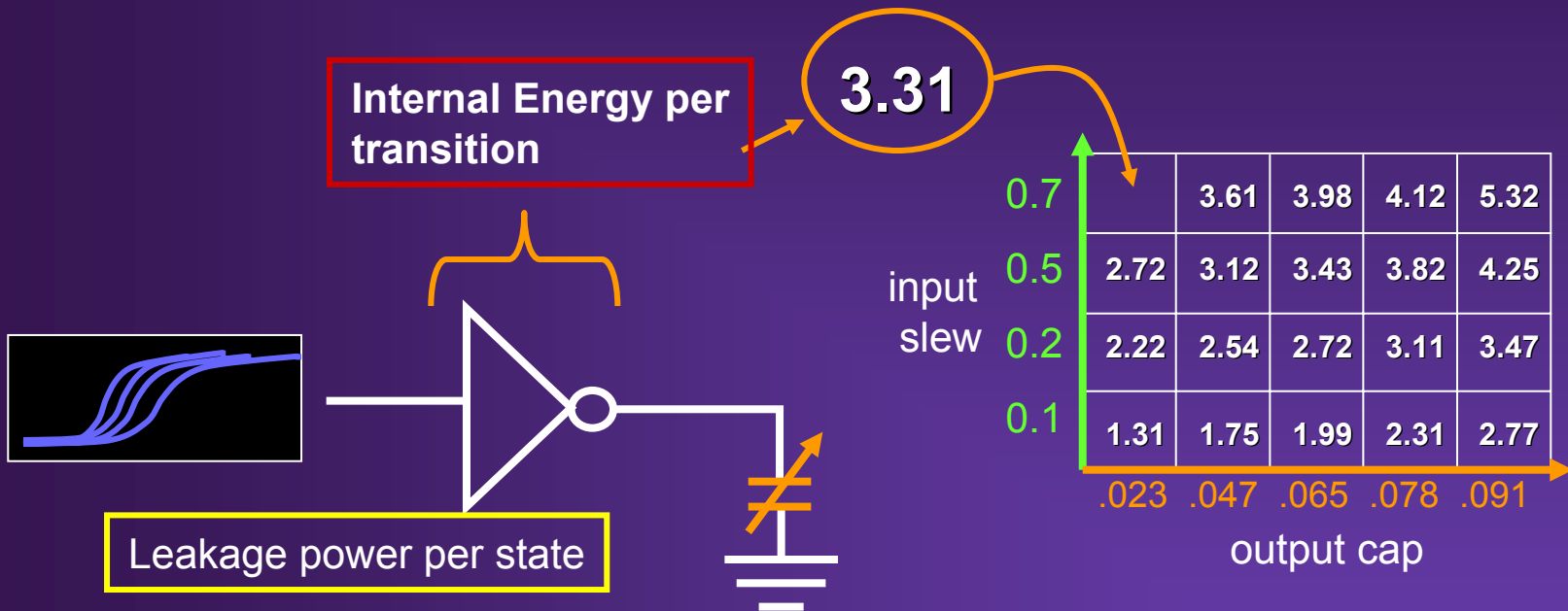


Introducing CCS Power

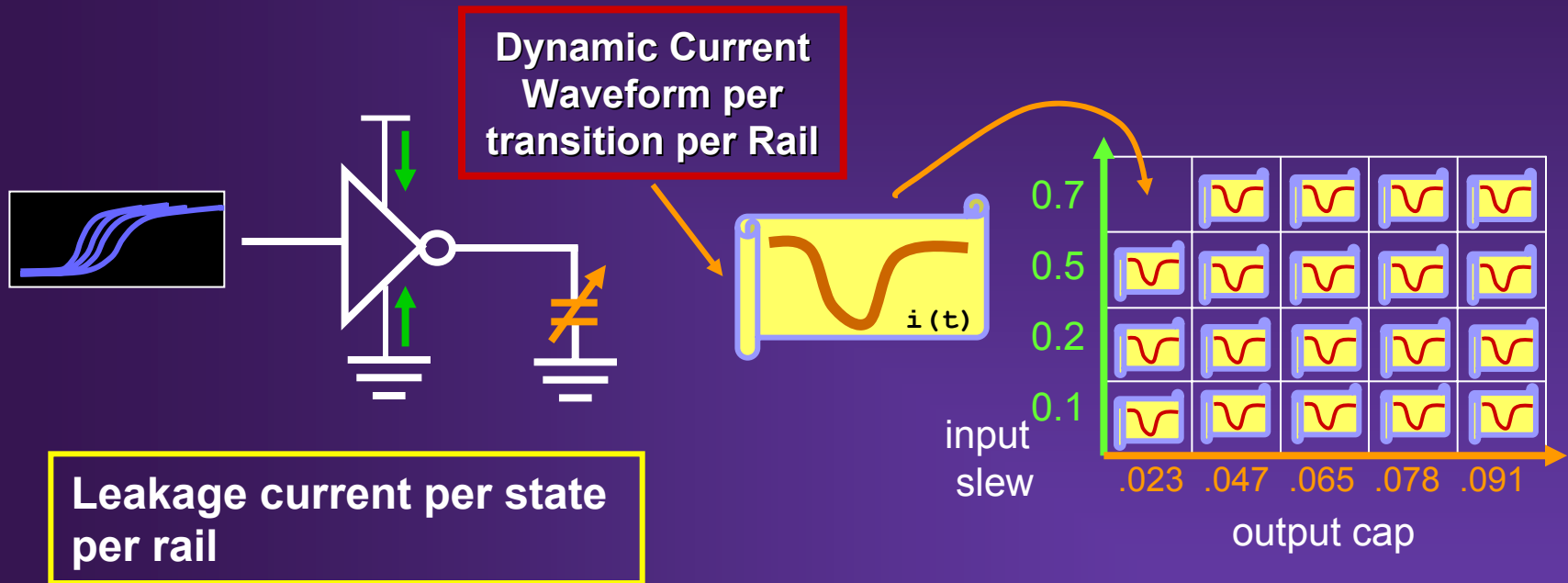
- **Switching current waveform for each power or ground pin**
 - **Finer time resolution**
 - **Full Multi-Voltage support**
- **Equivalent parasitics as seen from the power network**
 - **Allows fast yet accurate rail analysis**
- **Support for macro power modeling for memory and IP**
- **Unified library model for power optimization, power analysis, rail analysis**
 - **Fast and easy to characterize**

Characterization for NLPM

Liberty Non-Linear Power Model



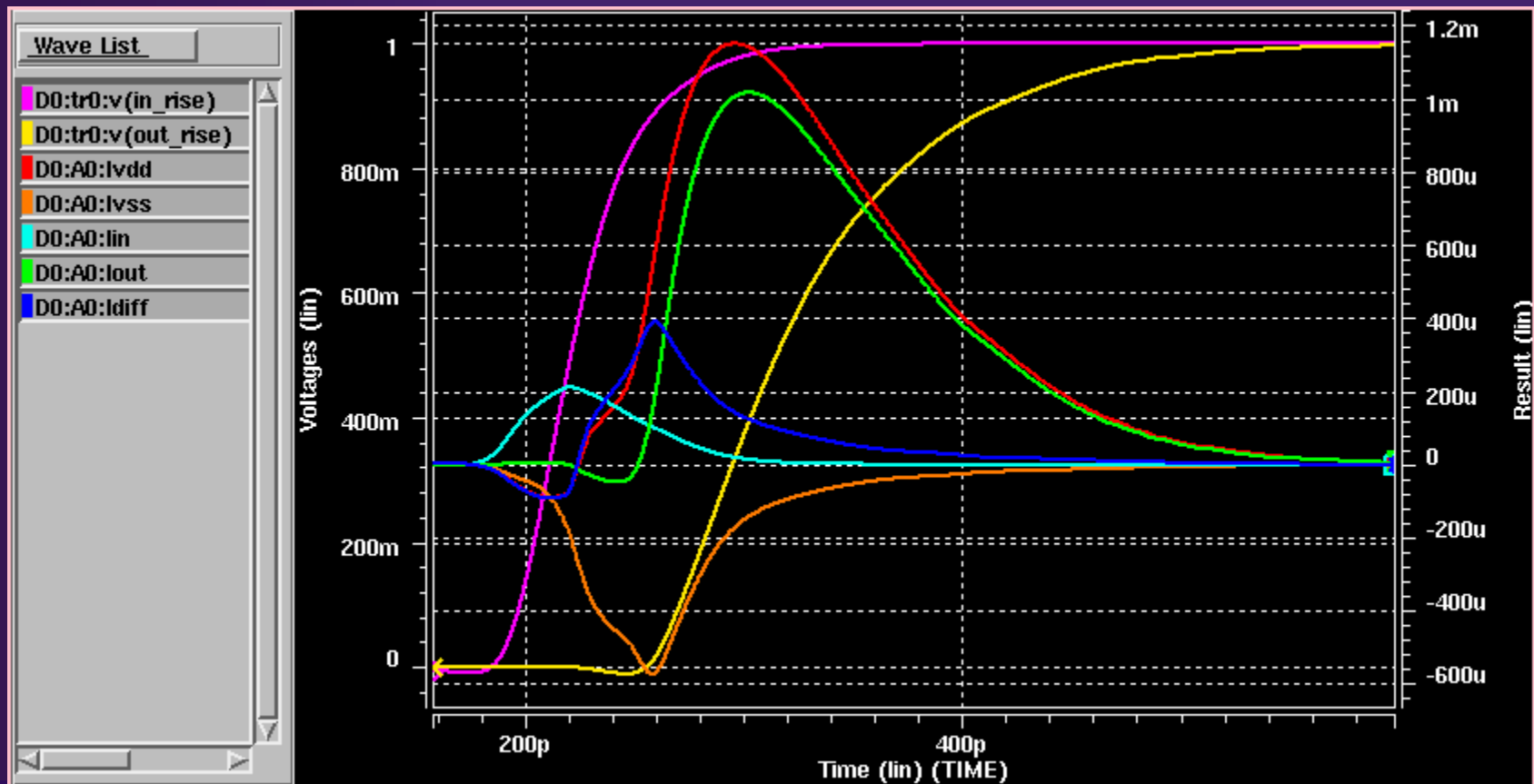
Characterization for CCS Power



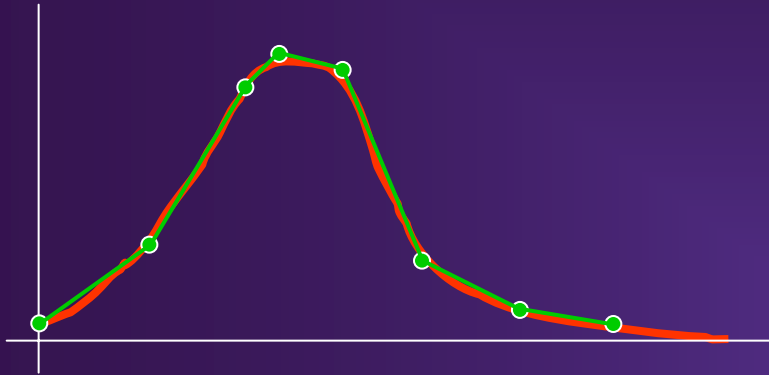
Can characterize CCS Power switching information concurrently with CCS Timing

CCS Power Characterization

- HSPICE Simulation: AND gate with rising input
 - Power pin (Vdd) current
 - Ground pin (Vss) current



Advantages: Time Resolution

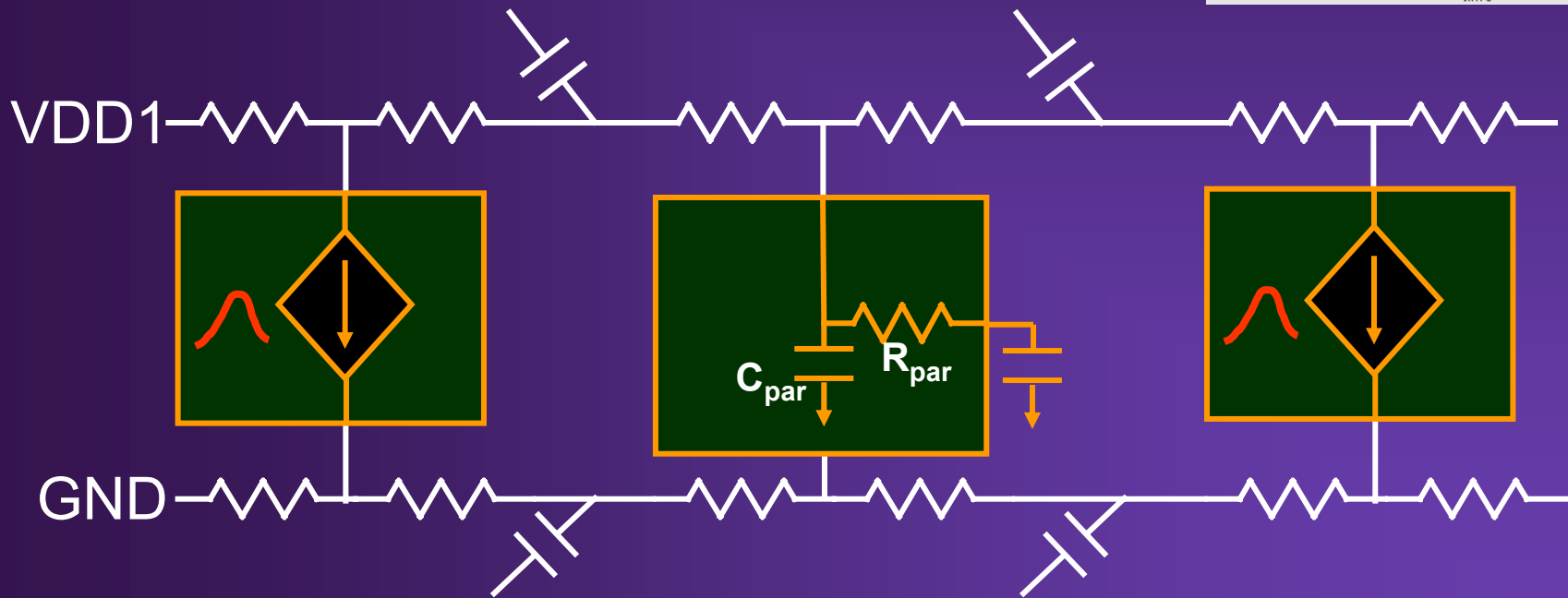
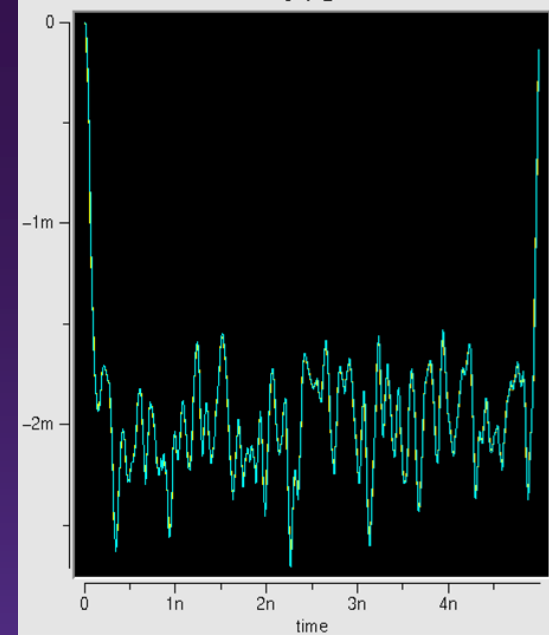


- Captures complete power and ground pin current waveforms
 - Charge/energy can be calculated by integrating current

$$\int_0^{+\infty} I dt \approx \sum_{i=1}^n \frac{I_i + I_{i-1}}{2} (t_i - t_{i-1}) + \frac{I_n (t_n - t_{n-1})}{\ln(I_{n-1}/I_n)}$$

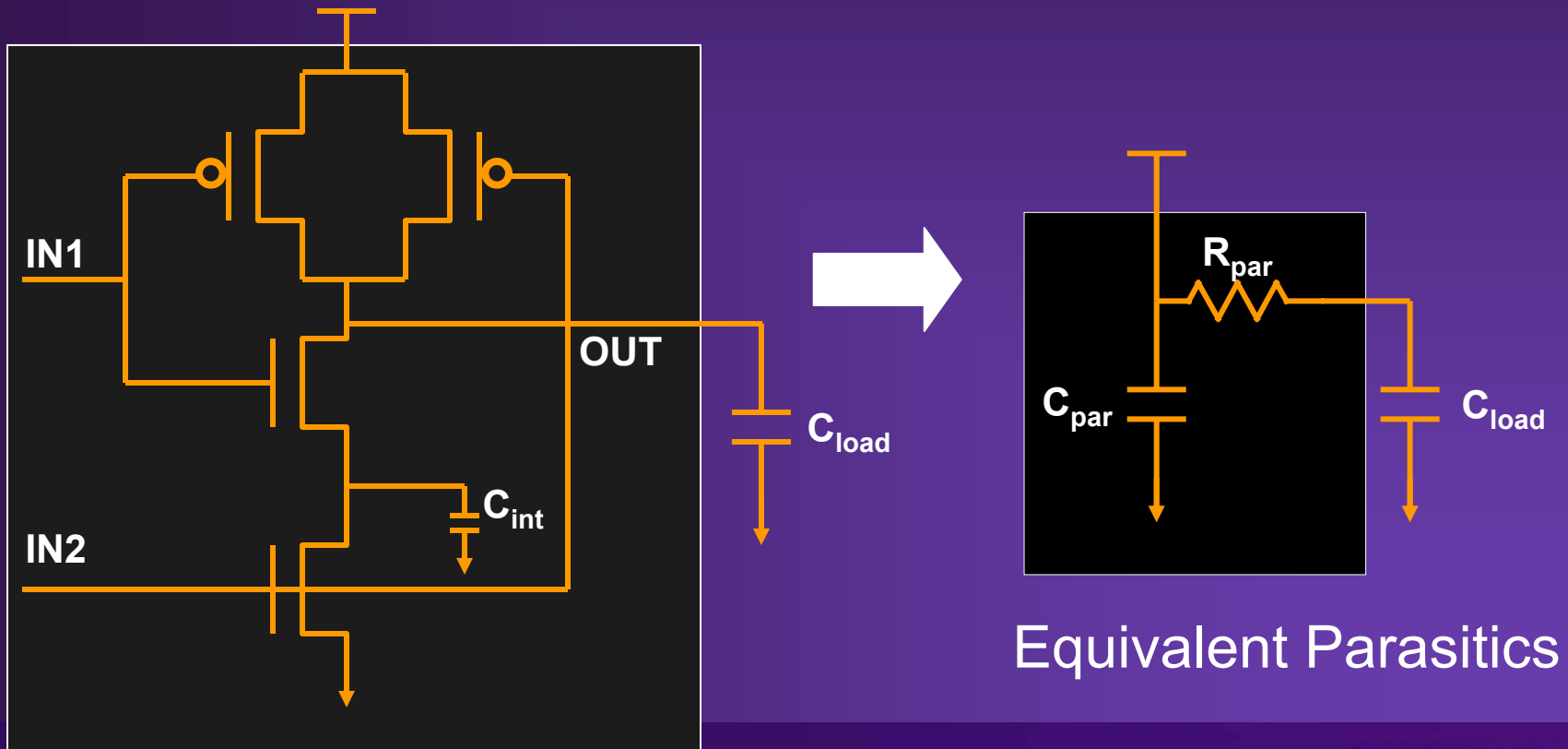
Dynamic Rail Analysis

- Compute instance-specific voltage drop at all power/ground pins
- Requires cell model for switching and non-switching cases



Equivalent Parasitics for Non-Switching Case

- Essential for accurate rail analysis – additional decoupling cap
- C_{par} per input state for each power or ground pin
- R_{par} per input state for each power or ground pin to each output



CCS Power Summary

- **Single Power Model For All Power Applications:**
 - **Power Optimization, Dynamic Rail Analysis, Power Analysis**
- **Accurately Models:**
 - **Transient current during switching**
 - **Equivalent parasitics for non-switching case**
 - **Leakage current**
 - **Multi-Voltage designs**
 - **Multi-rail cells**
 - **Non-zero ground rail**
 - **MTCMOS: fine-grain or coarse-grain**
- **Characterized concurrently with CCS Timing**

CCS Summary

Continuing With A Tradition Of Innovation

- **CCS - Next Generation Modeling Technology**
 - **Open Source**
 - **Unified Model For Timing, Noise and Power**
 - **Higher Accuracy as Needed By 90nm and Below**
- **Easy and Efficient Library Characterization**
- **Complete Ecosystem: Models, Format, Characterization**

Timing

Noise

Power

Technical Collateral Material

- Technical collateral material for CCS is available on:
www.synopsys.com/products/solutions/galaxy/ccs/cc_source.html

- It includes:
 - CCS Backgrounder
 - White Papers
 - Format Specification
 - FAQ

The screenshot shows the Synopsys website page for the Composite Current Source (CCS) modeling technology. The page is titled "Composite Current Source" and is part of the "Galaxy Design Platform". The navigation bar includes "PRODUCTS & SOLUTIONS", "PROFESSIONAL SERVICES", "EDUCATION & SUPPORT", "CORPORATE", and "PARTNERS". The main content area is divided into several sections: "Products", "Press Releases", "White Papers", and "Articles". The "Products" section lists the Composite Current Source (CCS) Modeling Technology, CCS Timing Format Specification, CCS Noise Format Specification, and CCS Power Format Specification. The "Press Releases" section lists several releases, including "Synopsys Galaxy Design Platform Now Supports Composite Current Source Modeling Technology" and "Synopsys Leads Industry with New Nanometer Modeling Tech". The "White Papers" section lists "CCS Timing White Paper", "CCS Noise White Paper", and "CCS Power White Paper". The "Articles" section lists "EE Times: Synopsys spins new physical model, preps statistical timer" and "EE Times: Synopsys claims first unified modeling for timing, noise". The "Composite Current Source" section includes an "Overview" and "Modeling Challenges". The "Overview" section states that accurate cell library models are essential for IC design implementation and sign-off tools. The "Modeling Challenges" section lists several challenges, including high impedance interconnect, Miller effect, dynamic IR-drop, multi-voltage, dynamic voltage and frequency scaling (DVFS), driver weakening, temperature inversion, and increasing variations.

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Galaxy Design Platform

Composite Current Source

Industry's First Open-Source, Current-Based Cell Library Model for Timing, Noise and Power

Overview

Accurate cell library models are essential for IC design implementation and sign-off tools. To ensure high accuracy at technology nodes of 90-nm and below, library models must accurately capture the complex transistor behavior of cells.

The Composite Current Source (CCS) modeling technology is the first in the industry to deliver a complete open-source current-based modeling solution for timing, noise and power. Along with the available parsers, characterization/validation tools, and guidelines, this open-source Liberty™ modeling format enables efficient characterization for cell library creators. For IC designers, the CCS modeling technology enables comprehensive nanometer design analysis and optimization for the first time. Designers can reduce design margins and speed design closure by eliminating iterations.

Modeling Challenges

- At process geometries of 90-nm and below, many new effects and design styles need to be supported during design implementation and sign-off. Some of these modeling challenges include:
 - High impedance interconnect
 - Miller effect
 - Dynamic IR-drop
 - Multi-voltage
 - Dynamic Voltage and Frequency Scaling (DVFS)
 - Driver weakening
 - Temperature inversion
 - Increasing variations