



16th EDA Interoperability Developer's Forum
Developing a SystemVerilog EcoSystem

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SystemVerilog Productivity is VeriEZ



A New Language



Do we need another language? I can do the same thing by downloading C++ libraries, spending hours looking for free tools and hiring a temporary summer intern!!

A New Language





A Complete Language

The power to create and destroy.

□ Very powerful syntax

❖ Design

➤ Don't get carried away

❖ Assertions

➤ Don't kill the simulation

❖ Testbench

➤ Don't use to write basic directed tests only

Users come from varied backgrounds!



Verification Efficiency

Automate Automate Automate

Verification-ready constructs

Tools

❖ Analysis

❖ Module Creation and Reuse

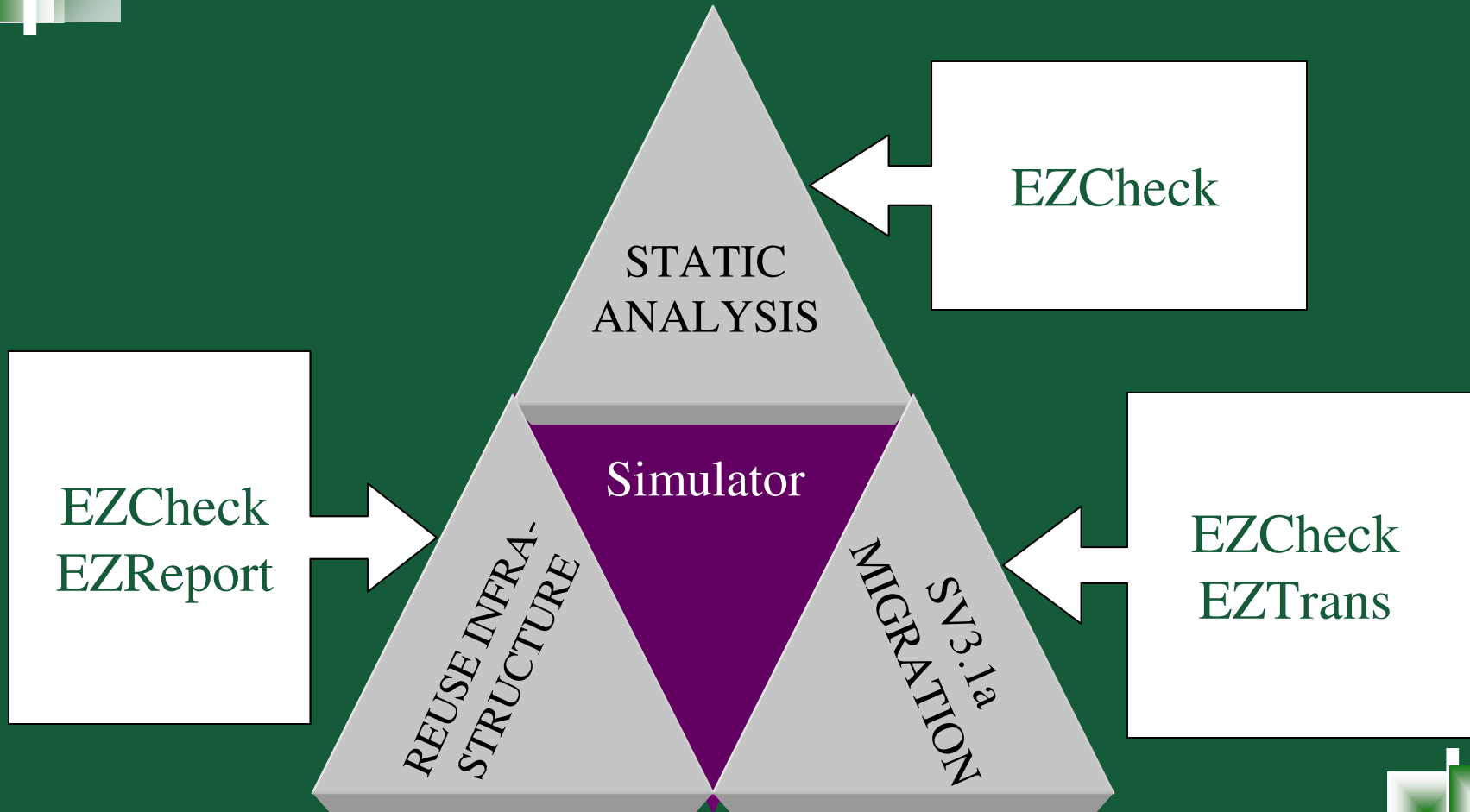
❖ Debug



The VeriEZ Advantage

- Verification Efficiency using static tools
 - ❖ Stand-alone tools – do not require simulation tools
 - ❖ Fit into existing flows
 - ❖ Easy to use and learn
- Focus on Module Creation and Reuse
 - ❖ Analysis
 - ❖ Knowledge Extraction
 - ❖ Translation

Technology Overview





Testbench Analysis

- Detect Performance issues
 - ❖ Constructs that can slow down simulation
 - ❖ Optimum DUT-TB connection
 - ❖ High-performance Coverage models
- Concurrency Analysis
 - ❖ Best practices for concurrency constructs
 - ❖ Checks for semaphore and mailbox calls
- OOP Practices
 - ❖ Class Design
 - ❖ Constructors, Hierarchy, Virtual Methods



Testbench Analysis

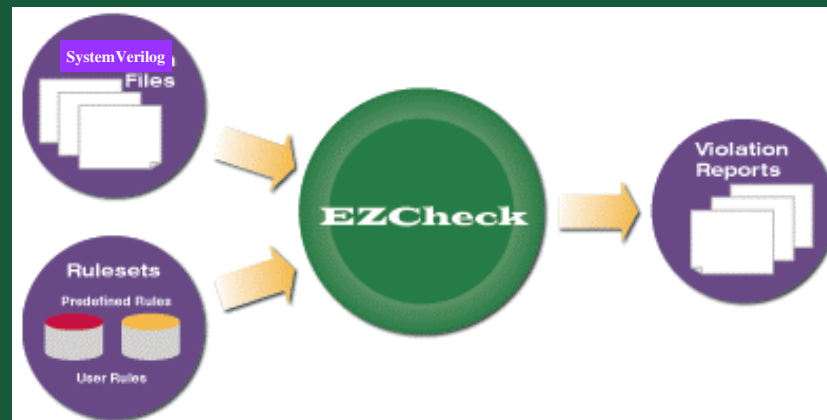
□ Classic Lint

- ❖ Uninitialized object
- ❖ Incompletely assigned subroutines
- ❖ Incomplete case statements
- ❖ RHS Truncation
- ❖ DPI parameter passing
- ❖ Invalid Array Access
- ❖ Dead Code

EZCheck – Static Analysis

Features:

- 200+ rules
- Pre-packaged rulesets
- Highly customizable
- Add your own rules



Rulesets:

- Basic
- Best Practices
- RVM/VVM

Benefits:

- Find errors that the compiler does not find
- Find errors before time-consuming simulations

Knowledge Extraction

Complex languages require effective tools

Class
Hierarchy

Interface
Connections

Synchronization
Mechanisms

Threads,
Global Objects
..

EZReport – Verification Knowledge Extractor



Includes
Interface
to Doxygen!

Features

- Class hierarchy
- Synchronization mechanisms
- Interfaces
- Global Variables and subroutines

Benefits

1. Understand external IP and legacy modules
2. Maintain up to date documentation



Translation

!! Reuse IP in a SystemVerilog Environment !!

- OpenVera => SystemVerilog
- e => SystemVerilog
- VHDL => SystemVerilog
- C/SystemC => SystemVerilog



Conclusion

SystemVerilog Has Arrived

- ❑ All major vendors have announced SV-compliant tool flows
- ❑ Users are using SV in production
- ❑ Creation, Reuse and Debug Tools available
- ❑ ...Look at the number of books!