

# Next-Generation EDA

**Jim Solomon**

*Silicon Navigator, CiraNova, Pyxis, Nascentric, AWR*

*Founder of SDA / Cadence*

# Designer's Needs are Changing

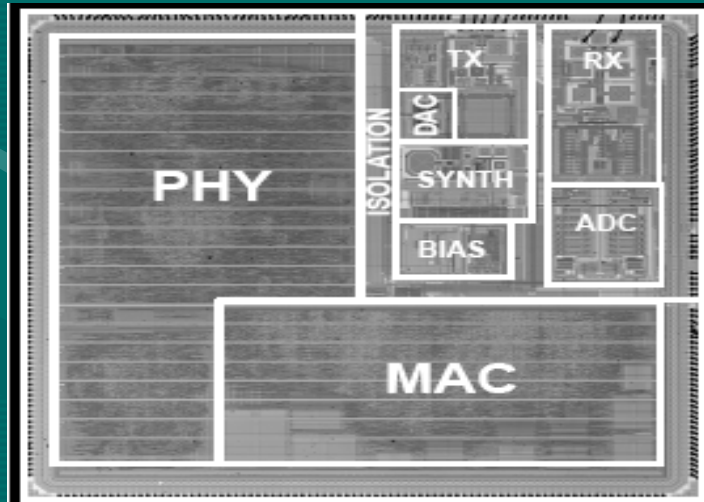
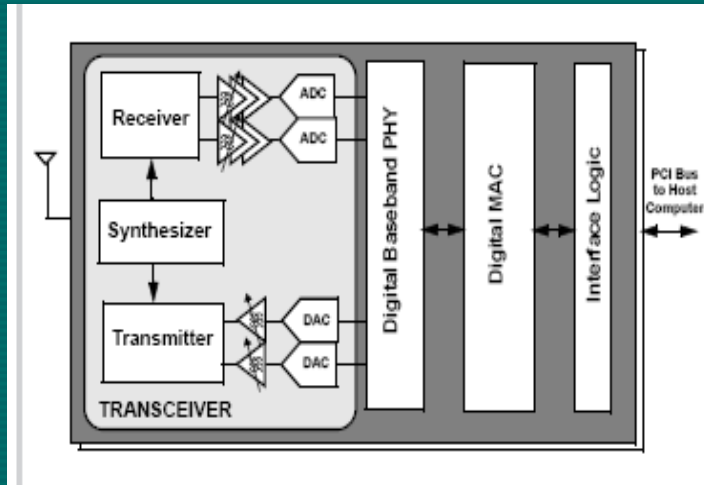
- About 80% of all SOC design starts are now mixed-signal\*
  - *Up from 20% in 1998*
  - *Cell phones, wireless LAN's, GPS's, MP3 players, PDA's, HDTV's, ...*
- This is causing major changes in design methods
  - *And it is breaking today's EDA tool flows*
- EDA providers without analog have incomplete solutions
  - *Even Cadence, the analog leader, has weak mixed-signal*
- Pure digital also sees change
  - *Designs are huge, must go system level*
  - *Sub-100nm nodes force us to transistor & wire details, DFM*

*\*Estimates from Designer's-Guide Consulting*

*Mixed-signal SOC's that break  
today's design flows*

*Some examples*

# 802.11G Wireless LAN Chip\*

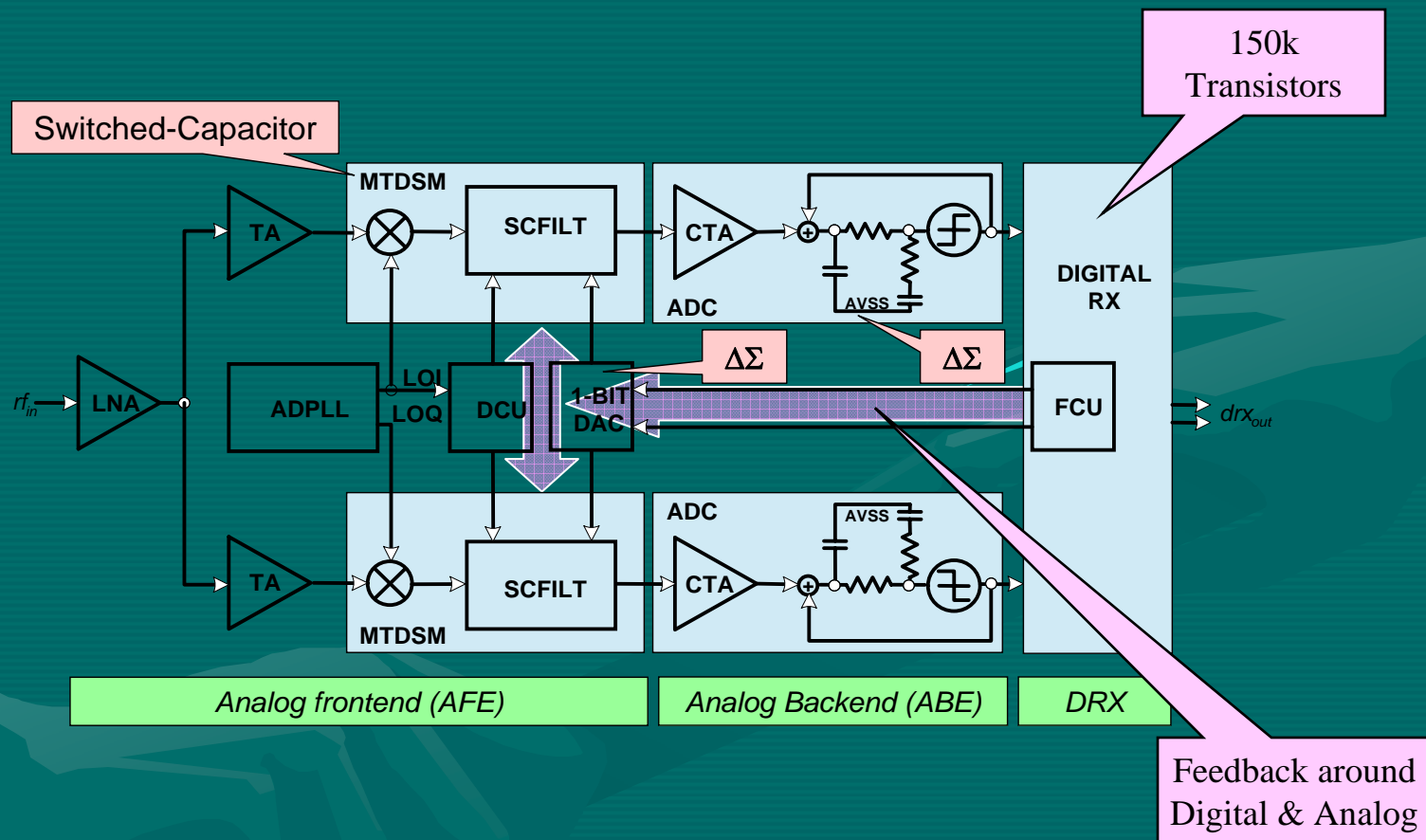


- New process nodes give us:
  - *Poor analog transistors, cheap gates*
- Use digital correction to fix analog
  - *Fixes dc offset, I/Q mismatch, RF carrier leakage*
- .18um CMOS
- Analysis requires transistor-level simulator
  - *Handle ~100k transistors, 10k cycles*

\* 2005 ISSCC Paper 5.2 Atheros, Stanford

# Algorithmic Mixed-Signal Radio

*for Cell Phones, other*

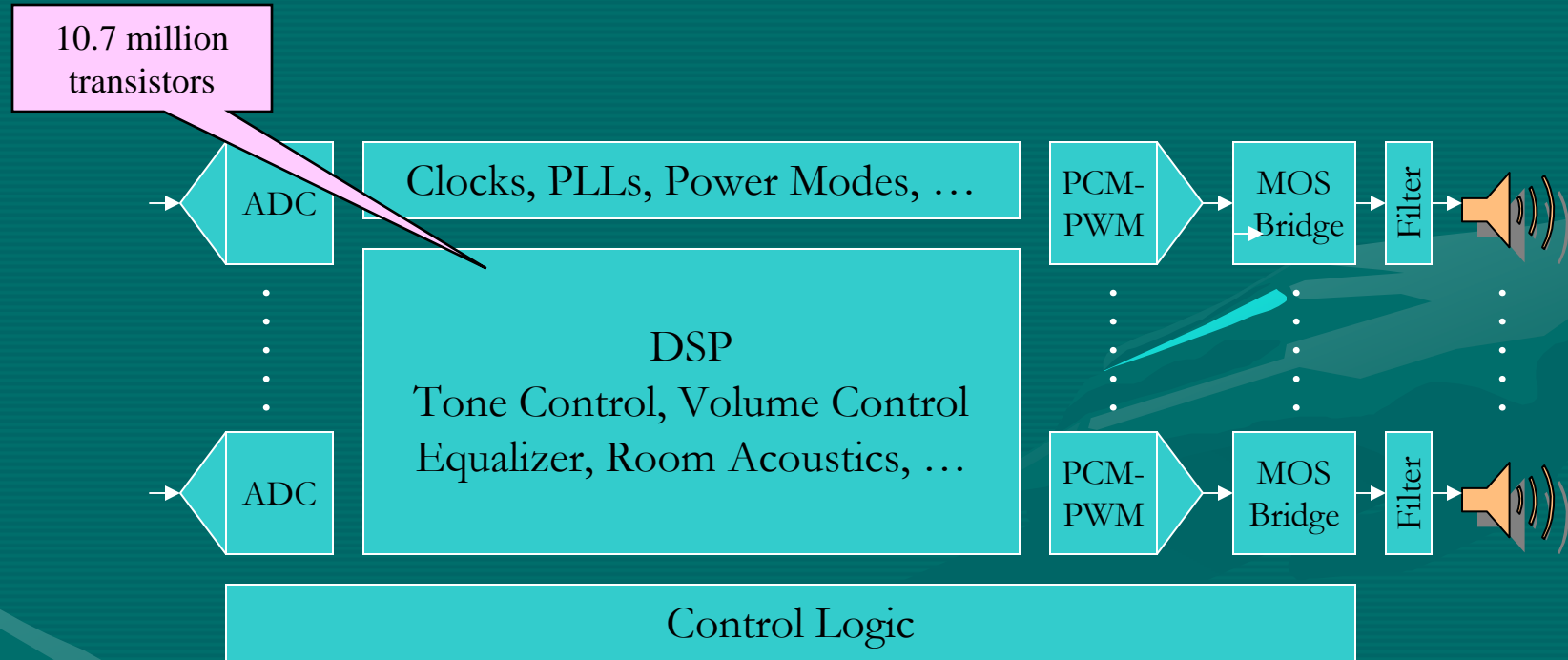


# Wireless Algorithmic Radios

*How do we design these?*

- Problem:
  - *Cannot simulate the analog-digital loop today - too big*
- Even though this is an RF system, *cannot use Harmonic Balance simulator*
  - *Must use time domain to handle gates + analog: Spectre or HSpice*
  - *But these are much too slow for 150k transistors, 100k cycles*
- Need new tool:
  - *Fast analog Spice that has ~100x speedup at full Spice accuracy*

# Multi-channel Digital-Audio Amp\*



*Need to verify chip & test features like power-up & speaker pop*

\* D2Audio design

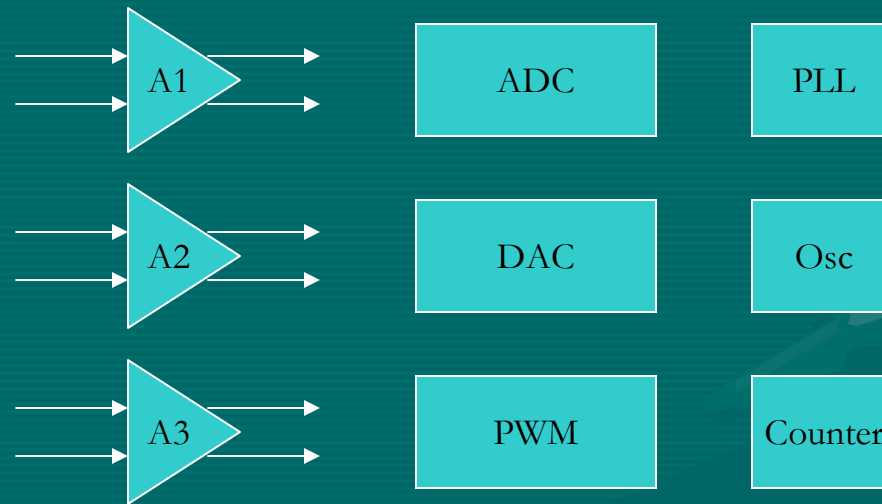
# Multi-channel Digital-Audio Amp

## *How do we verify this design?*

- Today's FastMOS simulators (HSim, NanoSim, UltraSim) do not speed-up random logic
  - *Little speedup over Spice, accuracy poor, may not converge*
- Could try Verilog & Verilog-A
  - *But generally no Verilog-A models available, want transistor-level*
- Requires a 3<sup>rd</sup> Generation FastMOS simulator
  - *Must handle 10M transistor random logic + memory and analog*
  - *Need ~10,000x speed-up over Spice*
- Co-simulate with *fast analog Spice* for mixed-signal

# Wideband Blocks for HD TV

*RF & Wideband Amps, ADCs, PLLs, Oscillators*



RF video amps, baseband amps

*Design for lowest distortion, highest precision*

# Wideband Blocks for HD TV

## *How do we design these?*

- Typical today
  - *Rough estimated parasitics used during circuit design*
  - *But layout is manual, cannot extract parasitics until design done*
- Big issue: *Need early simulation with accurate parasitics*
- What is needed:
  - *Analog-constrained floor planner, placer, router – “automatic” & quick*
  - *Build on procedural “PyCells” for IP reuse & process retargeting\**
  - *Tightly coupled layout & schematic editors for rapid incremental changes*

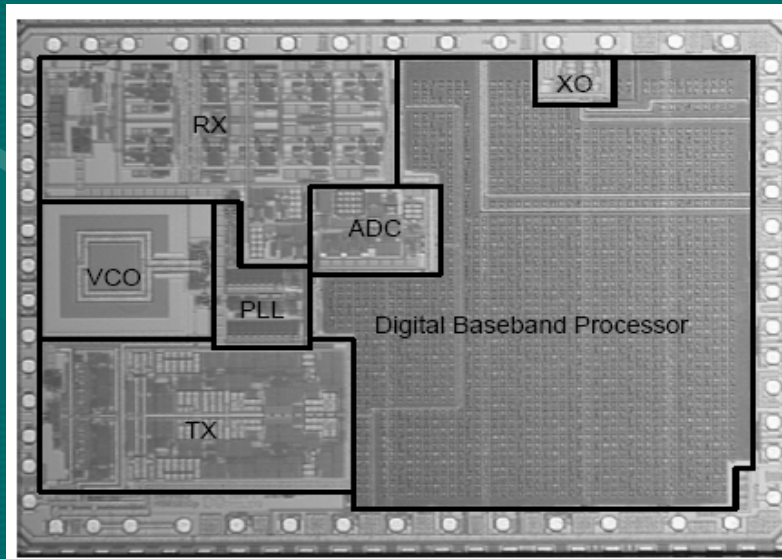
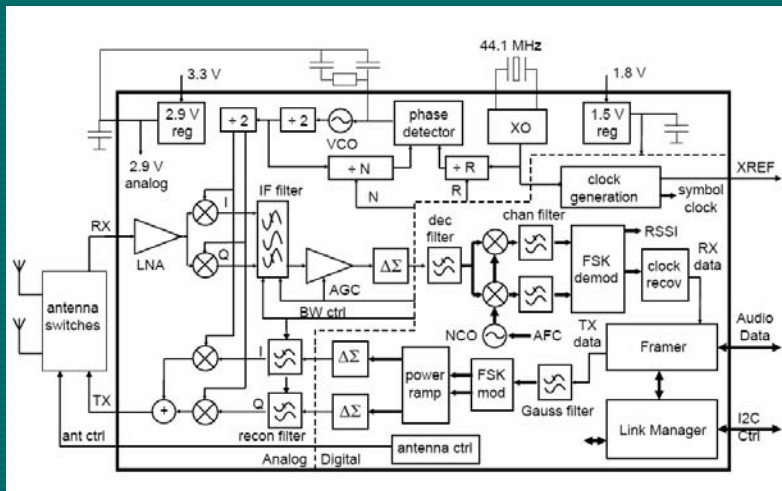
*\* Use of procedural PyCells at core of system is a very important add*

# What about Reusable Analog IP Blocks?

- Biggest need: *Expression handler that captures all electrical and physical design equations and data*
  - *When IP is reused, have all info needed to retarget block*
  - *Need new language: Python\* is best choice - complete language, open & portable, no memory management, rich libraries & IDE's*
- Analog electrical synthesis
  - *Automatically sizes transistors, includes optimizer for running corner cases, test bench design, etc.*

\* *Strong religious positioning needed, it is time we retire SKILL*

# Wireless Digital Audio TX/RX SOC\*



- High-end wireless headphones
- Single chip FSK 856MHz Tx/Rx
- Concerns: Clock noise in analog - substrate noise, power supply coupling, ...
- .25um BiCMOS 10mm<sup>2</sup>
- 55% of area is digital

\* 2005 ISSCC Paper 5.6 Catena & Philips

# Wireless Mixed-Signal SOCs

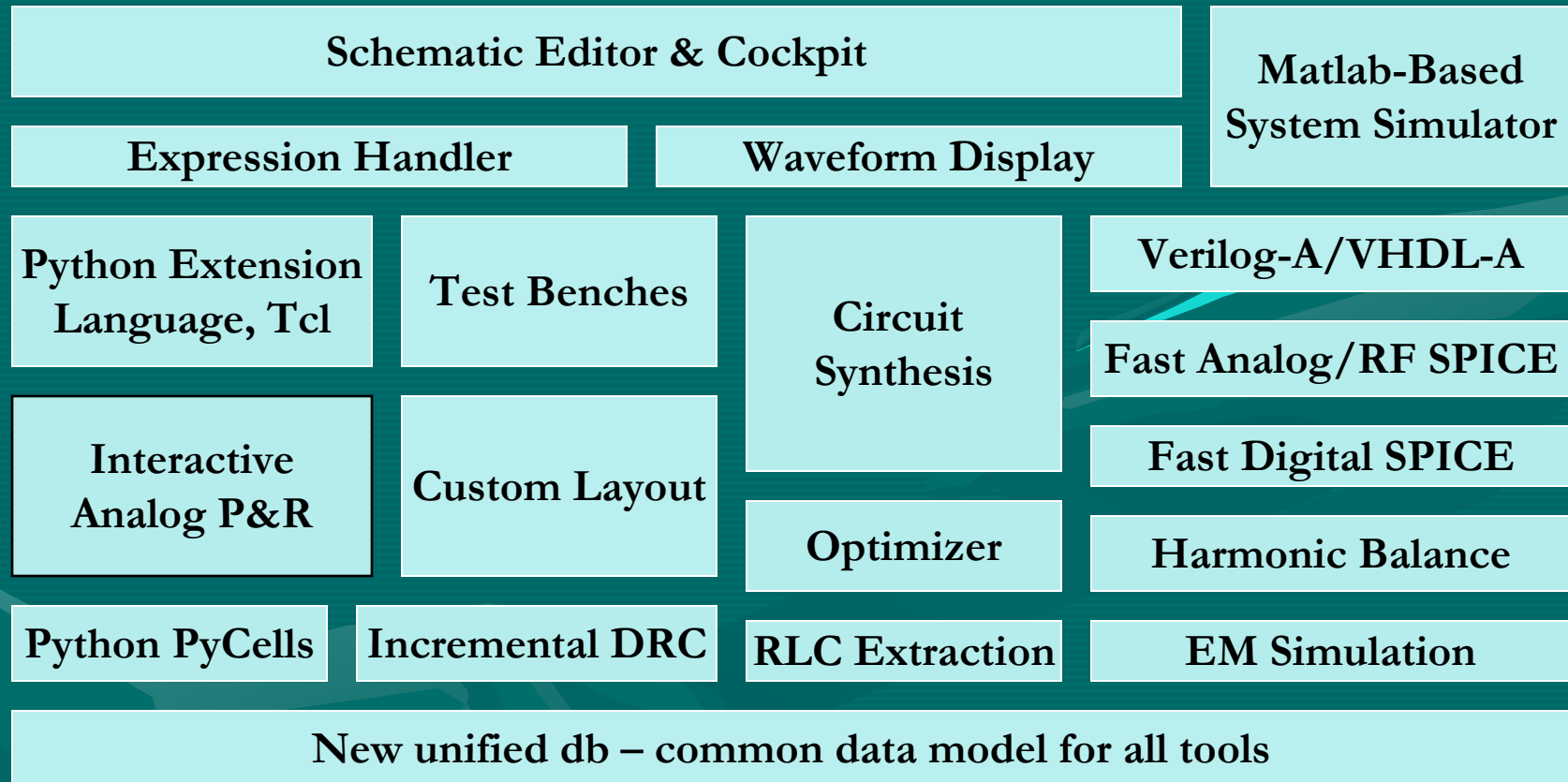
## *How do we design these?*

- Start with system simulation
  - *Need new Matlab-based simulator (not Ptolemy or SPW)*
- Need connectivity correspondence between system simulator & circuit simulator
- Next use transistor-level simulation
  - *Spectre time domain preferred, but too slow for SOC*
  - *Have analog-digital loops, need fast analog Spice*
  - *Assess substrate noise & power coupling*

# A Next Gen Analog Mixed-Signal Design System

*Most of needed capabilities identified by our design examples*

# Next Gen Analog-MS Design System



*New tools replace virtually every tool in last gen system*

# Some Features of Next Gen MS System

- Automatically propagate changes in the design equations
  - *All views of design immediately updated: electrical, physical*
- Immediately switch between any of several simulators
  - *Compare results, find problems*
- True transistor-level simulation for m-s SOCs
- Tightly coupled flows
  - *Can cross probe, quickly do parasitic re-simulation, run optimization loops to explore design space & corners*

*New: tools & db support analog constraints, parameterization, parasitics, wire models, ...*

# Do We Really Need a Next Gen System?

- FW's, db's & tools need to be re-written every 7-10 yrs
  - *Design styles, processes & target markets change*
  - *The Analog Artist/Virtuoso system completed in 1990, 15 years ago!*
- Much of today's code base is old, *needs re-write*
  - *Companies keep evolving old code, quality worsens*
- Many flows kludged together from acquisitions
  - *db translations, slow, error prone, poor usability, inflexible*
- Cost of maintaining worn-out legacy code is huge
  - *Little resource available to work on next-gen solutions*

# How can the Industry develop this?

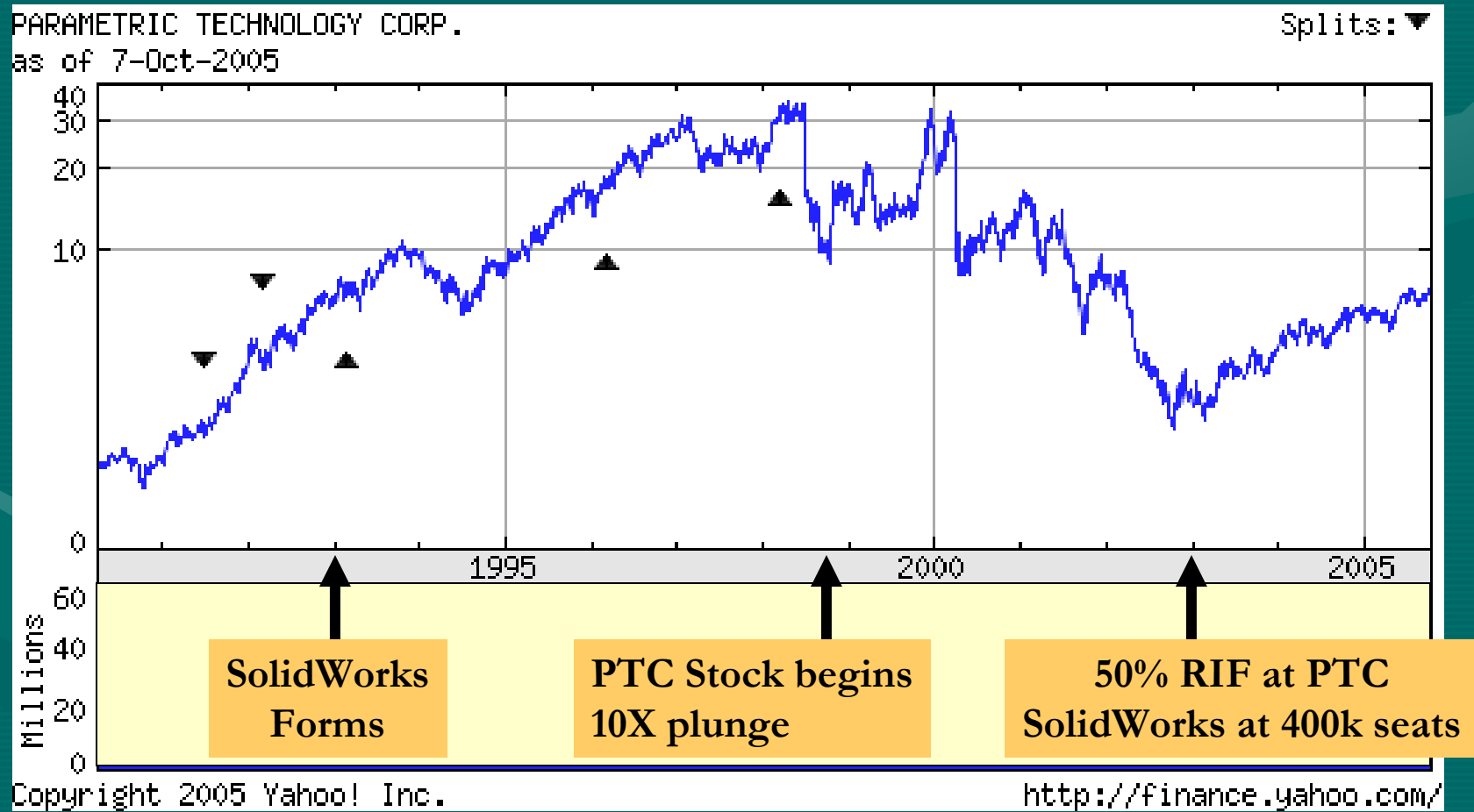
- Large companies need to move to “parallel track” development
  - *Small team owns present code, larger team develops next-gen*
  - *Similar to Intel, Microsoft, nVidia, ATI*
- Next-gen developers need modern software engineering
  - *Much of EDA still mired in “C-Unix-think”*
  - *Move to object-oriented C++, component architecture, COM-like plug & play, reconfigurable flows*
- *Companies who don't do this may go into decline*

*Remember IBM, DEC, SUN, SGI, PTI, ...?*

# A Saga in Mechanical CAD: Parametric Technology vs. SolidWorks

- PTC
  - The pioneering leader, high quality
  - *Remained mired in “C & Unix-think”, just evolved old code*
  - *Product was powerful, but difficult to learn and use*
- SolidWorks
  - *Started on Windows, used modern software engineering*
  - *High ease of use, minimal support*
  - *More efficient channel lowered cost*
  - *Priced product lower than PTC by about 2X*

# A Saga in Mechanical CAD: Parametric Technology vs. SolidWorks



# What if the Large EDA Companies Do Not Make the Needed Changes?

*Could a new EDA leader emerge?*

**Hold that thought,**

we are getting ahead of ourselves ...

*What about our aging FW & Tools?*

# Relevant New Thinking Started in 1999

- Free open source software initiatives gaining wide interest - *Linux, Python, Tcl,..*
- Open database would unify tools from all EDA companies
  - *Solves nightmare of integrating acquired companies' tools*
- Influencers at UC Berkeley & Cadence pushed to open Cadence's next-gen database
  - *Alberto S-V, Patrick Scaglia, Ted Vucurevich*
- *The EDA OpenAccess initiative began life*

# Where is OpenAccess Now?

- OpenAccess has taken 5+ years to develop (so far)
- It is the next generation Cadence database
  - *Cadence has “started” releasing tools on it*
- Many EDA startups are developing OA native apps
- Synopsys has committed to analog / m-s on OA
- We are well past critical mass for OA adoption
  - *OA will be the next-gen database for the EDA industry*
  - *All players can influence OA, and benefit from it*

# This is Great for EDA Customers

- “Best-in-class” OA components widely available:
  - *From large & small EDA companies, internal CAD/design groups*
  - *Can build special design flows by reconfiguring components*
- CAD & design groups can develop better customized flows
  - *OpenAccess assures interoperability, speed, usability\**

*\* Interoperability standards still need to be agreed upon for this to be true*

**It's not going to happen overnight - it will take time, but it is now unstoppable**

*The EDA Industry is heading toward a new era where all tools run on a single unified database*

# But take note: this is a discontinuity!

*OpenAccess introduces risk for existing EDA  
players & opportunities for new players*

*More discontinuities:  
Multi-core computing, changing design styles*

So, ...

*How are the various segments of the  
EDA Industry going to evolve in the  
coming OpenAccess era?*

The background is a solid teal color. In the lower half, there is a faint, semi-transparent image of two hands shaking, symbolizing agreement or partnership. The text 'The EDA Leaders' is centered in the upper half.

# The EDA Leaders

# Cadence Design

- Status
  - *A few tools (Virtuoso & Allegro) are on OA – about 50% native, but are aging, Catena router is only 100% OA native tool*
  - *Synthesis, P&R, ... not DFII, cannot use emulation*
- Apparent strategy
  - *“Evolve” tools onto OpenAccess, use translators initially*
  - *Avoid acquiring tools in future*
  - *Not clear how they avoid being late to their own party*
- Prospects:
  - *Presently the leader, but at RISK*

# Synopsys

- Status
  - *No tools on OA, no mixed-signal, acquired P&R aging*
  - *Recently committed to OA for analog & mixed-signal*
- Apparent Strategy
  - *Attack Cadence mixed-signal with OA native analog*
  - *Digital strategy not clear, native rewrite on OA likely*
- Prospects
  - *Better than Cadence, now focused on moving quickly. Can they find a way?*

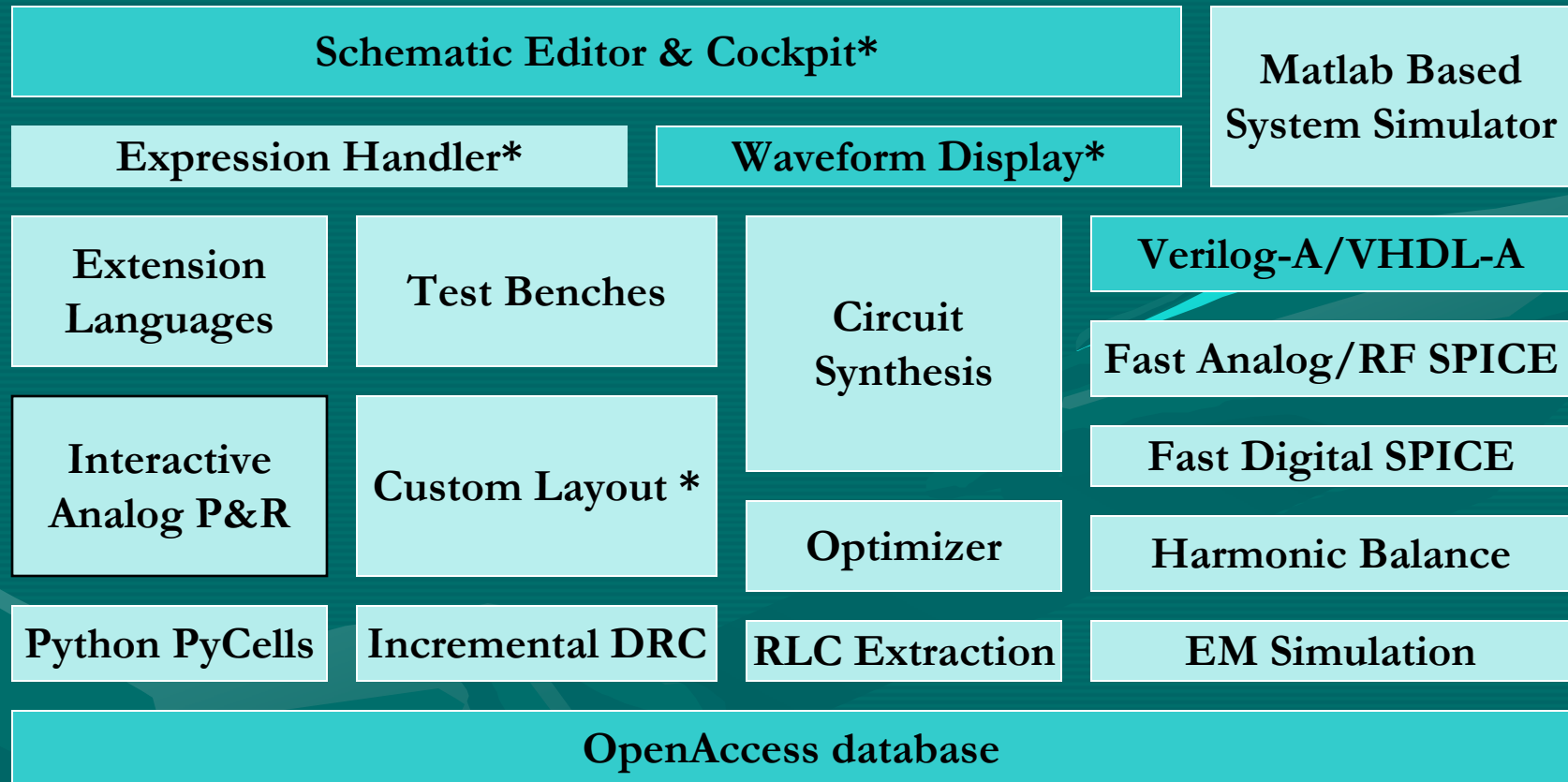
# Magma

- Status
  - *Have a solid digital flow on unified db, good performance*
  - *Innovative fixed timing closure, no mixed-signal, db not extensible*
- Apparent Strategy
  - *Emulate OA on their db*
- Prospects
  - *Only a temporary defense: feels like DEC defending VMS against UNIX*

# Next Gen OA-based EDA\*

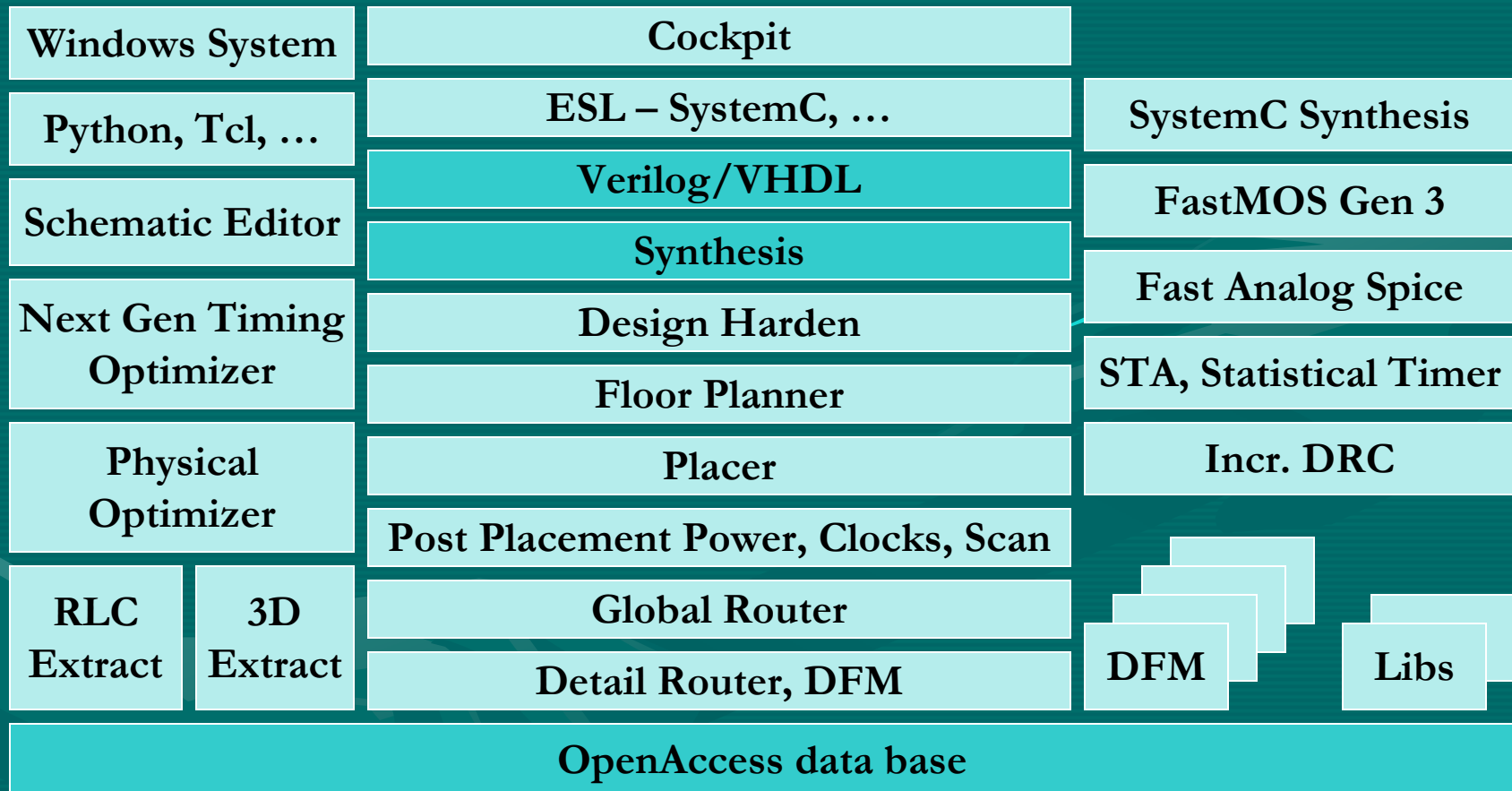
*\* Start-ups highlighted*

# Next Gen Analog-MS Design System



= *New tools from Start-ups*     
  = *Existing tools,*     
 \* *Need replacements*

# Next Gen Digital Design System



■ = *New tool from Start-up*

■ = *Existing tools*

# Features of Next Gen Digital System

- Componentized plug 'n play architecture enables customized design flows
  - *All tools built from reusable components that can be reconfigured*
  - *New design styles for consumer flows, low power, high performance, ...*
- New timers, timing optimization & synthesis algorithms
  - *Magma fixed timing flow now 5+ years old*
- *Multi-core computing used to speed up design turn-around*
- SystemC simulators & synthesis tightly integrated into flows
- Third gen FastMOS transistor-level simulator gives 10,000x speed-up on random logic, as well as memory

# Could Startups Disrupt the Leaders?

- First native OA flows will come largely from startups
  - *The EDA leaders are mired in legacy code support*
  - *But the leaders control customers with time-based licenses and the safety of “working with a large entity”*
- Possible outcomes
  - *The large EDA companies may have to make acquisitions to stay competitive on OA*
  - *The startups stay independent and offer complete design flows that threaten the large EDA companies*
  - *All EDA companies cooperate to provide best-in-class user flows*

# Summary

- New SOC designs are breaking today's EDA flows
- New features & data types in OpenAccess designed to enable next gen capabilities
- Significant *new algorithms, flows & reconfigurability* will give customers much improved solutions
- EDA startups are well ahead with native OA capabilities
- OpenAccess is a *discontinuity* that could disrupt today's leaders
- Wide adoption of next gen OA-based EDA starts in 2007

*It looks now is the time to start moving to OpenAccess*



# END

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