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Introducing V-SDC

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Formality® Equivalence Checker

Your Interoperability Partner

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Agenda

- Introduction to V-SDC
- RTL-to-gate equivalence checking challenges
- Use of V-SDC to remove the challenges

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V-SDC Definition

Verification - SDC

- A new Tcl-based standard
- Records common design optimizations that occur during implementation
- Allows downstream tools to better correlate between RTL and netlist
- Targets equivalence checking (EC) verification but can benefit any tool correlating RTL to gates

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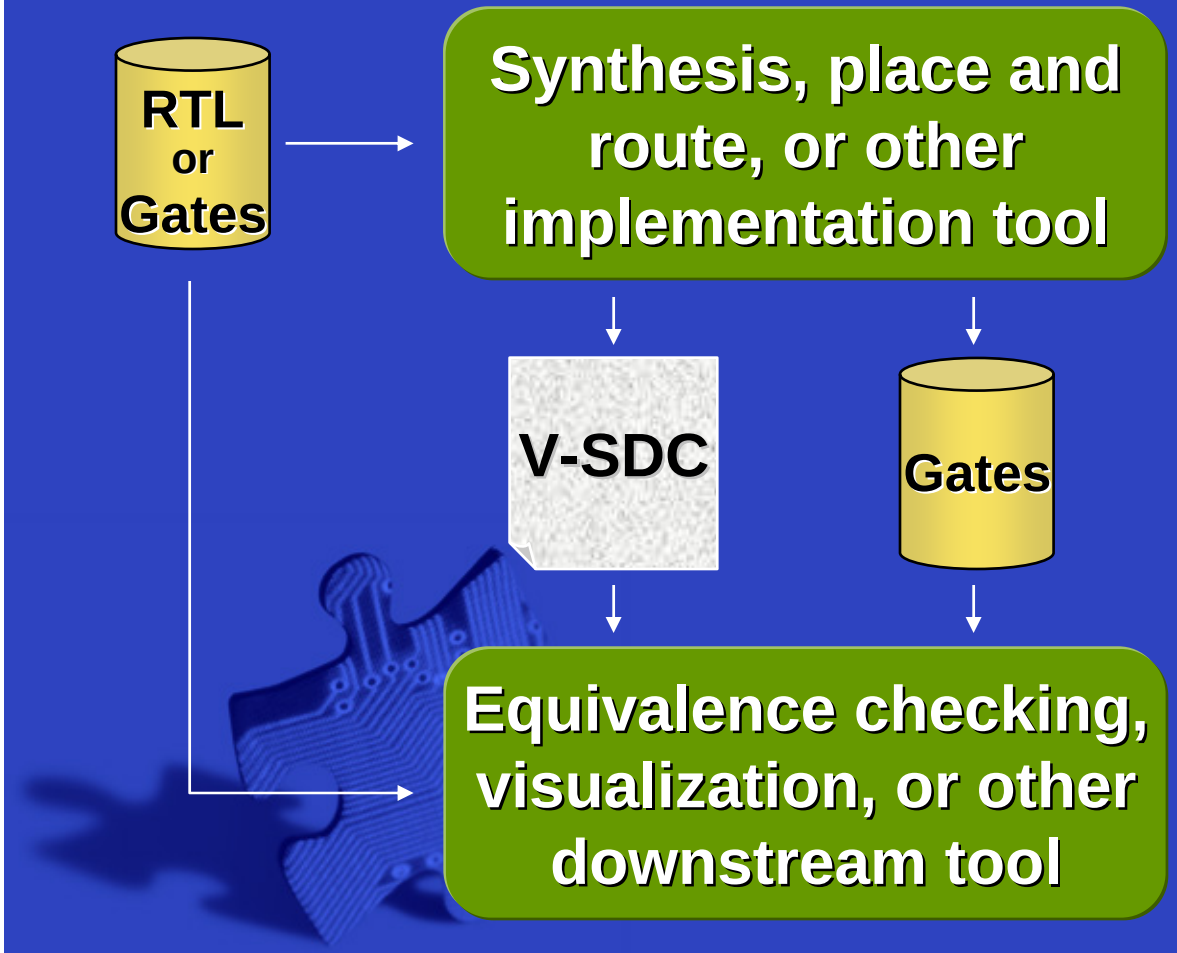
V-SDC Flow



- V-SDC data contained within its own file
- No impact to existing SDC flows

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What is Equivalence Checking (EC)

- Determines if two versions of a design are functionally equivalent
- Uses formal, static techniques
  - No test vectors
  - Mathematically exhaustive
  - Orders of magnitude faster than dynamic verification techniques

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Fundamentals of EC Verification

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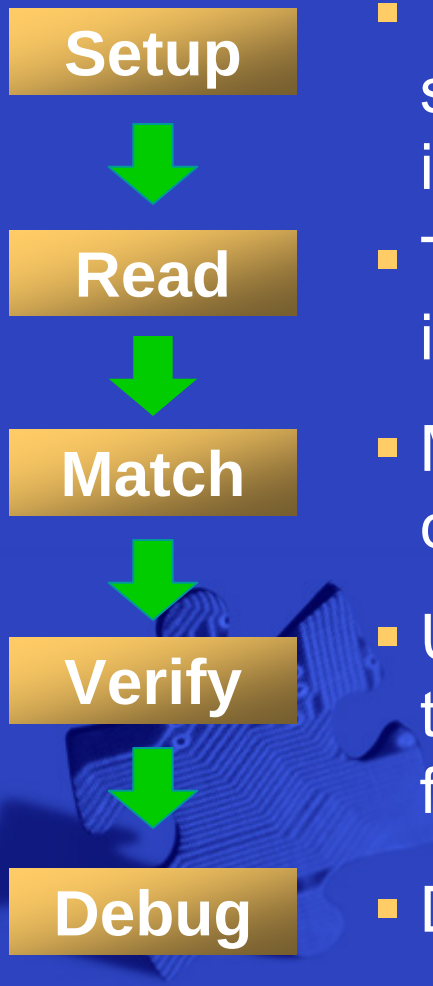
Review



- Tool is setup to read two versions of the same design (a golden reference and an implementation)
- The designs are read and segmented into manageable components
- Matching aligns corresponding components for verification
- Use mathematical techniques to verify that all matched components are functionally equivalent
- Debug as necessary

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Fundamentals of EC Verification

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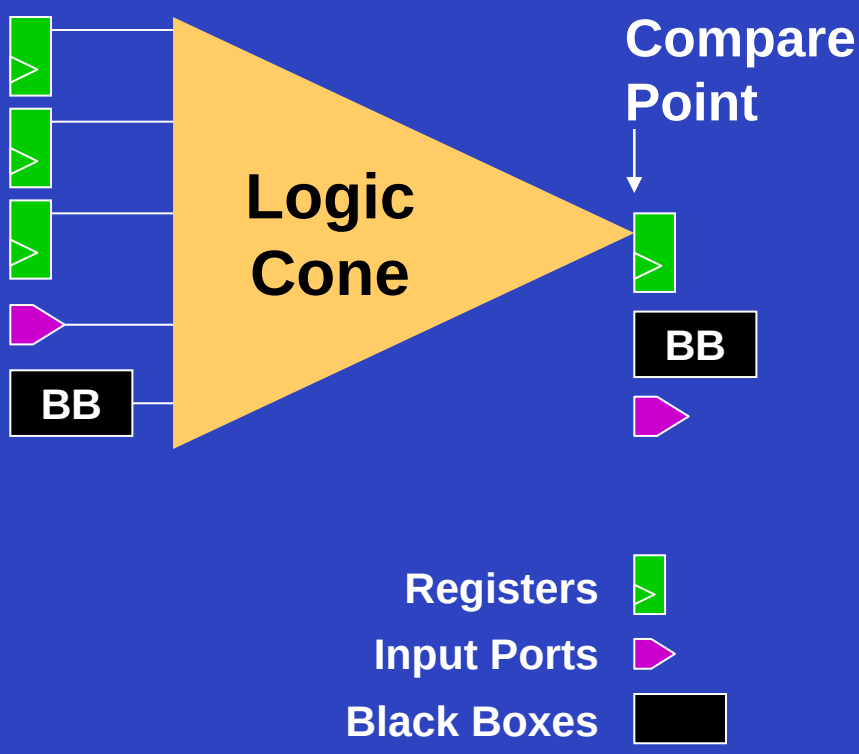
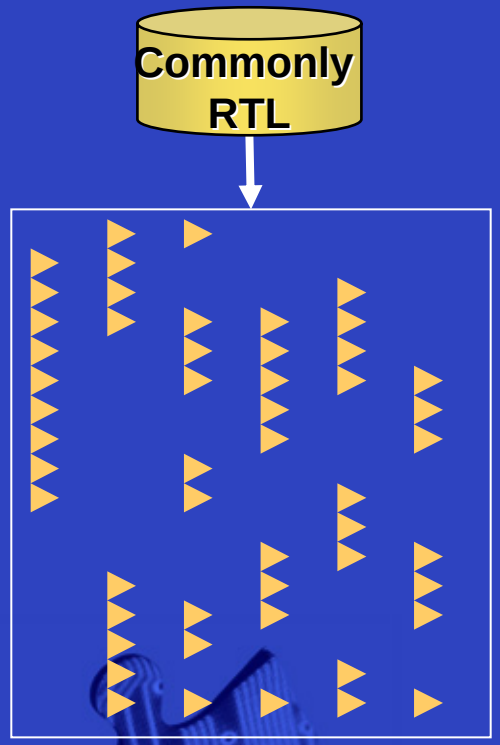
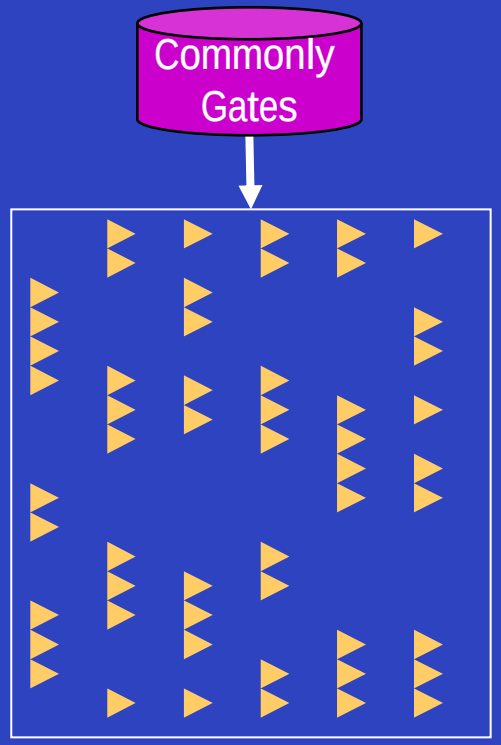
Logic Cones

- Smaller design segments are necessary for mathematical solvability
- Called “logic cones” these segments are primarily created by triggering off of register inputs and outputs
- Logic cone outputs are called compare points



Matching the Design Versions





After reading in the designs, there exists no alignment between logic cones. EC tools align corresponding cones by matching the compare points (cone outputs)

Matching the Compare Points

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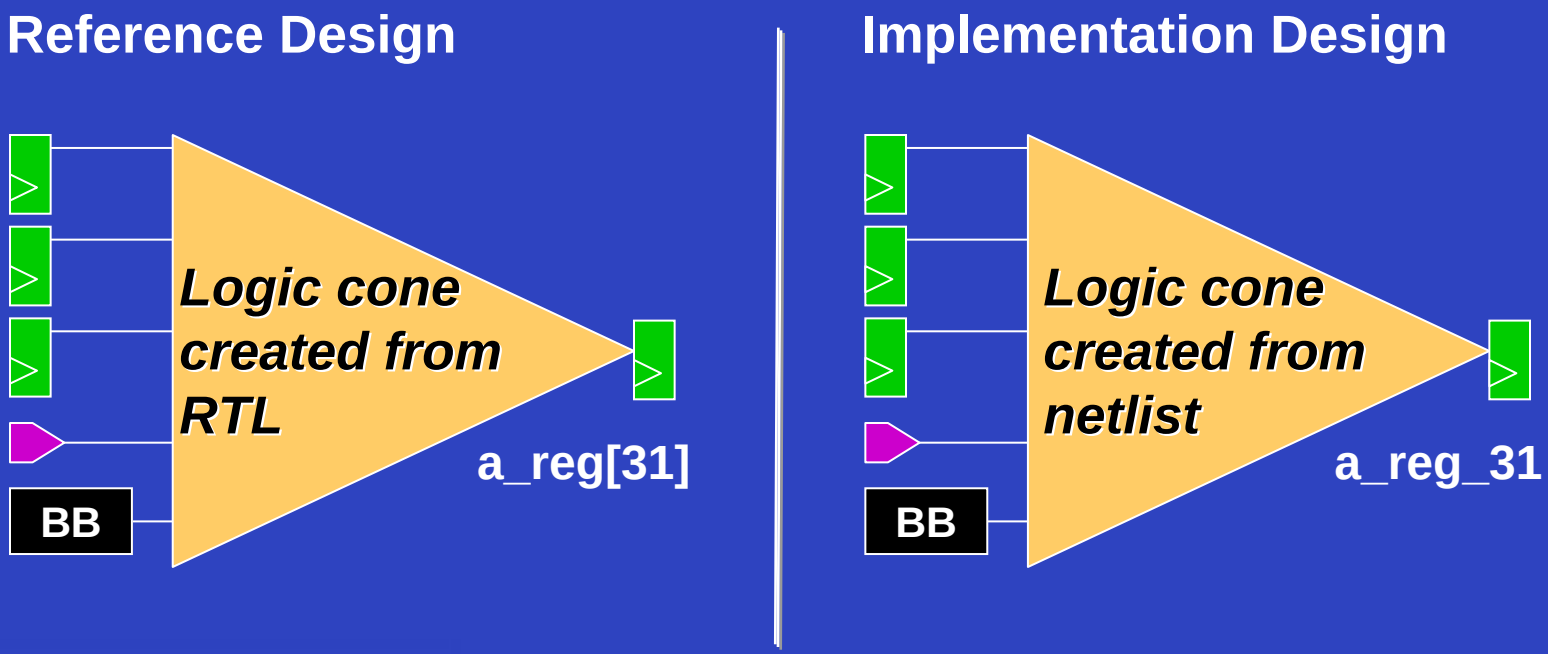

- Most efficient method to match logic cones is by considering compare point names (e.g. the above points match automatically by name)
- For compare points not automatically matched by name, manual matching or advanced algorithms can be used

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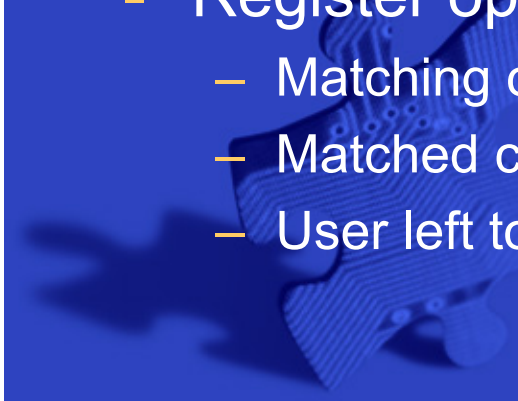
Key Observations

- Register naming and matching are fundamental to all EC technology
- Severe name changes complicate compare point matching
  - Manual or advanced algorithms may be necessary
  - Manual matching consumes bandwidth
  - Advanced algorithms take more time
- Register optimizations impact logic cones
  - Matching of some cones may not be possible
  - Matched cones may no longer be equivalent
  - User left to sort it out via manual intervention



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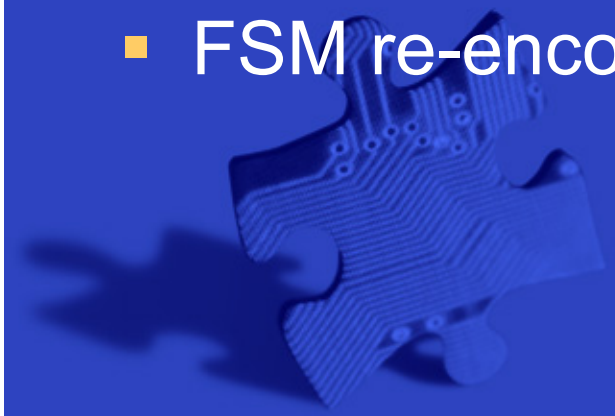
V-SDC Content

A Tcl Record of Common Changes

- Name changes caused by grouping, ungrouping, uniquifying, ununiquifying or other optimization
- Registers optimized away as constants
- Duplicate and merged registers
- FSM re-encoding



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Benefits of a Tcl Record

- Information can be used to automatically correlate between RTL and gate-level netlist
- Improves overall verification performance
  - More points can be matched by name, the fastest technique
- Maximize engineering resources
  - Less manual effort spent in setup
  - Removes design verification iterations due to missing setup

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V-SDC Example

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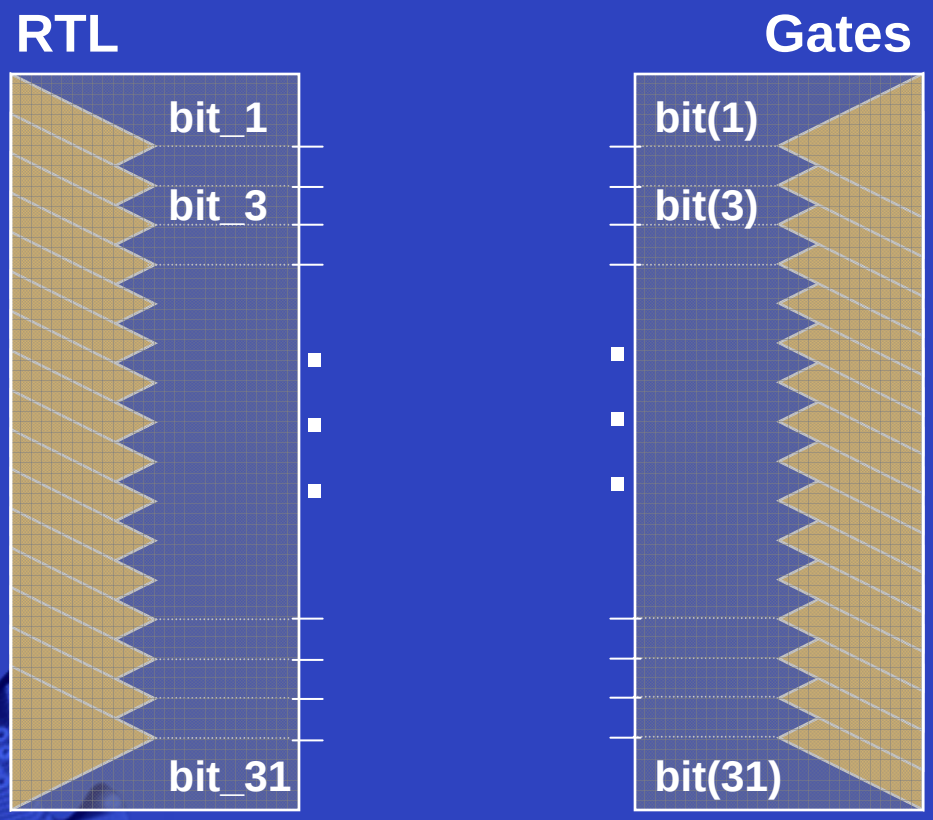
Unpredictable Name Changes



Any EC tool will match these points by name

V-SDC Example

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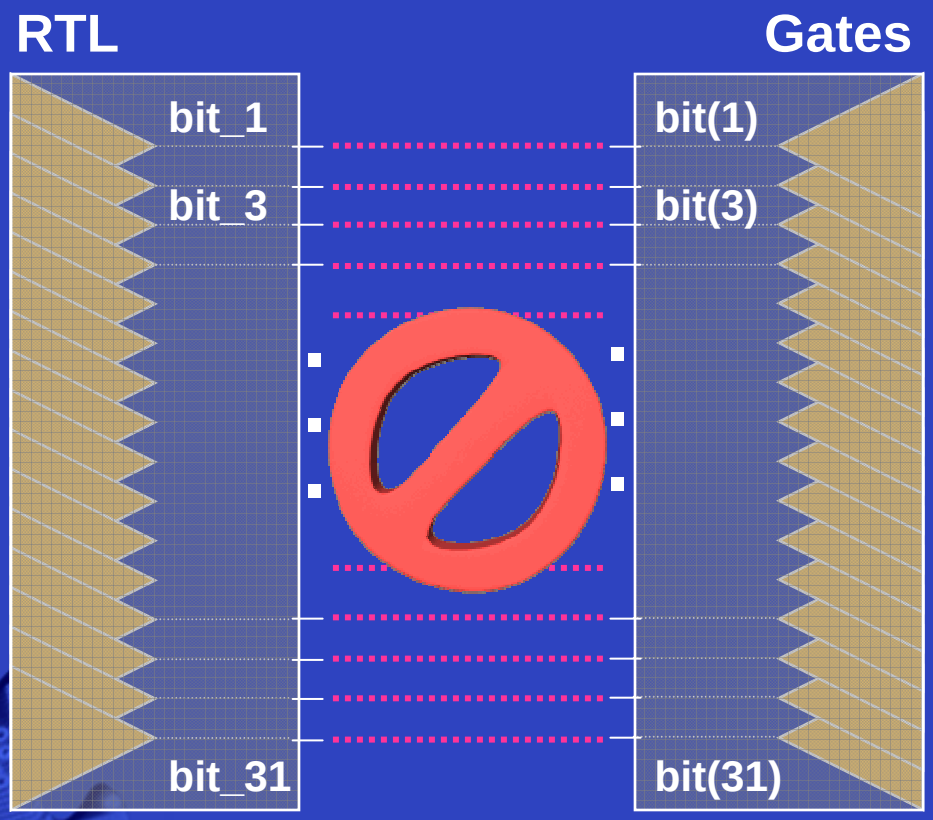
Unpredictable Name Changes



In this example, bit_1 ≠ bit(1) and bit_2 ≠ bit(2)…
In fact, there exists no predictable correlation

V-SDC Example

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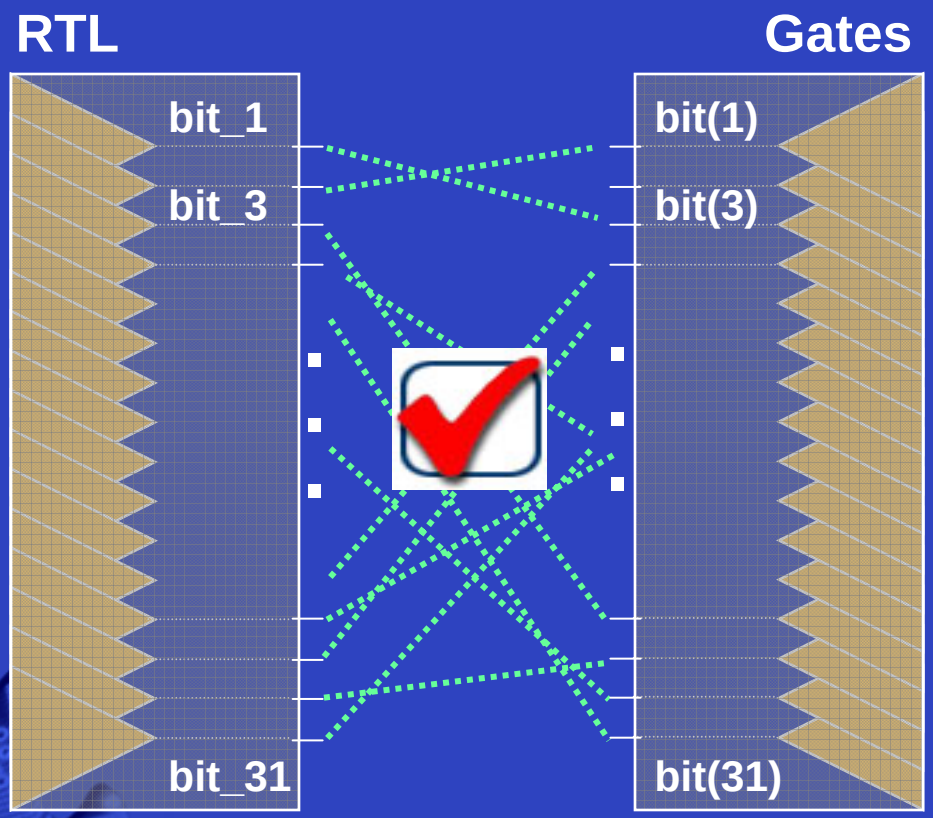
Unpredictable Name Changes



V-SDC provides proper mapping and the user will quickly and properly match the design for verification

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V-SDC Tcl Format

Syntax Example for Changed Names

guide_change_names -design designName
[-instance instanceName] [changeblock]

Arguments
-design designName, the design containing the names
-instance instanceName, the instance containing the names
changeblock, a colon-separated list specifying the object, old name, and new name

Example

```
guide_change_names -design test \
{ cell:U1:mycell3 \
port:clock:myclk }
```

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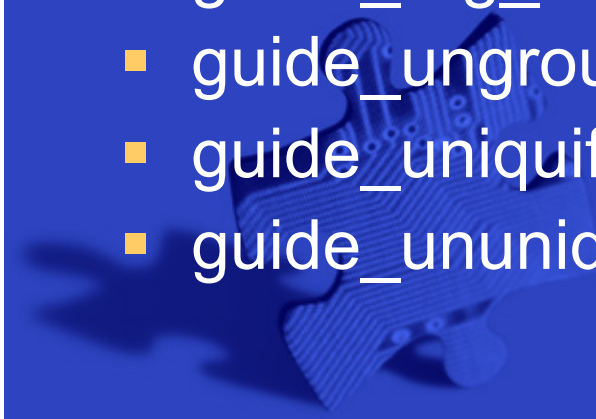
V-SDC Tcl Command List

- guide_change_names
- guide_fsm_reencoding
- guide_group
- guide_reg_constant
- guide_reg_duplication
- guide_reg_merging
- guide_ungroup
- guide_uniquify
- guide_ununiquify



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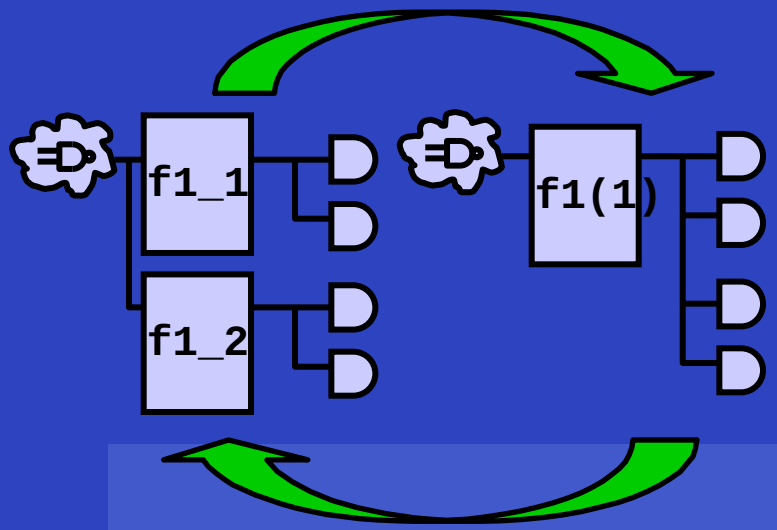
Duplicated/Merged Registers

Common optimization for area or fan-out

- Challenge:
  - f1_1 will match by name to f1(1) but they may not be functionally equivalent
  - Additionally, time spent searching for f1_2
  - Verification will likely fail
  - User left to sort it out
- V-SDC
  - EC tool accounts for the change before verifying



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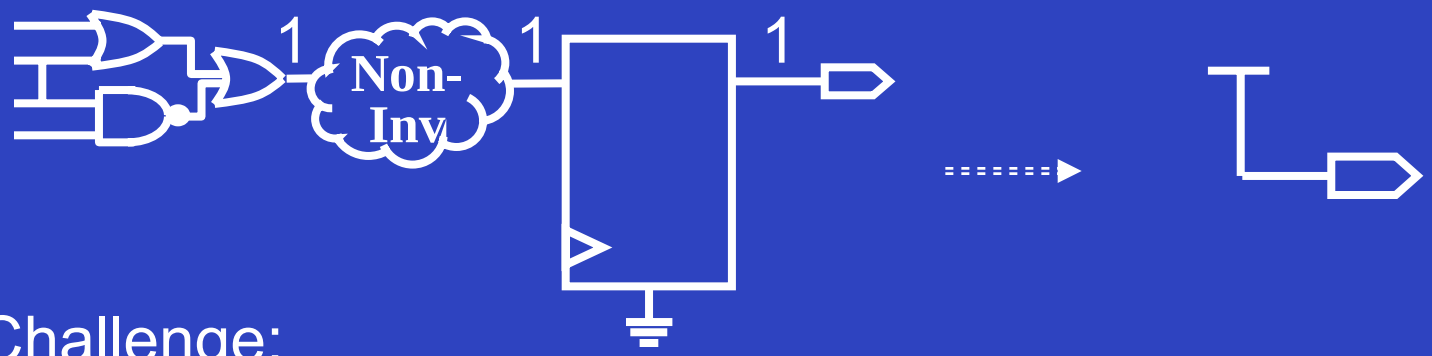
Constant Register

Automated Setup for Verification



- Challenge:
  - Not accounting for constants leads to numerous unmatched cones
  - Engineering resources required to isolate and properly setup for the constant
- V-SDC
  - Setup for constants is automatic
  - Constant should be proven or verified by the user before use

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Re-Encoded FSMs

Automated Setup for Verification

- Re-encode FSMs for area or performance benefits
- Challenge:
  - By default tools commonly infer binary encoding unless explicitly defined in RTL
  - Changes to logic cones cause verification to fail
- V-SDC
  - Setup is automatic
  - Re-encoding should be proven or verified before use

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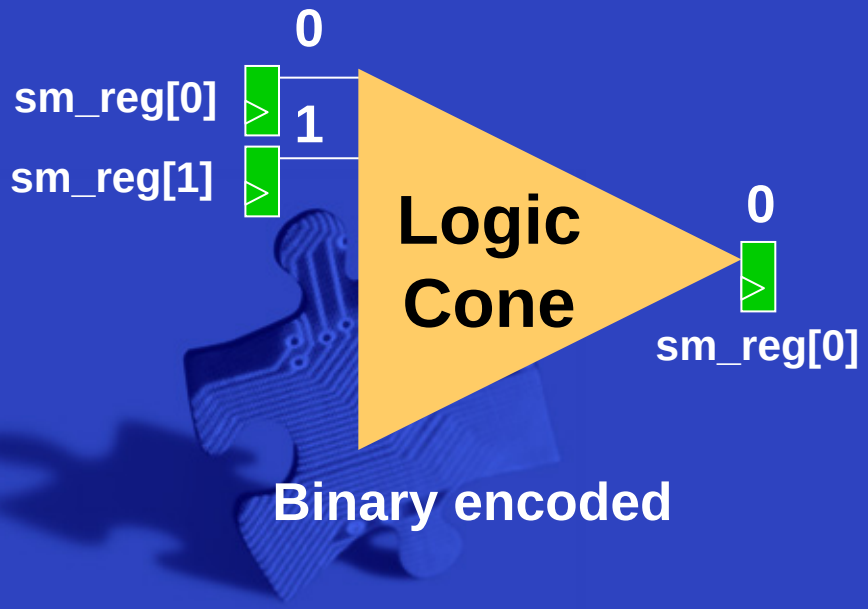
Re-Encoded FSMs

Automated Setup for Verification

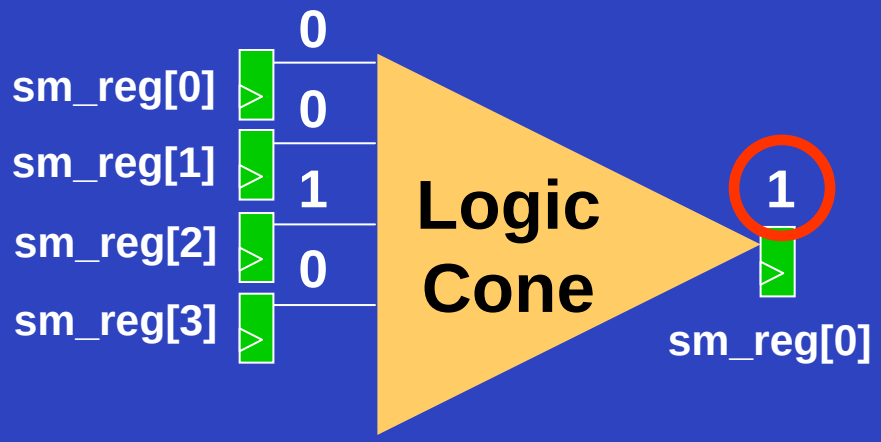
Reference Design



Binary encoded

Implementation Design

Extra State Points Can Cause Functional Difference



One-hot encoded

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V-SDC Availability

- Synopsys support
  - Design Compiler product portfolio writes V-SDC
  - Formality reads V-SDC
- Open and available to all via free Open-Source click-through license
- User Guide (version W-2005.12) is available for download from the TAP-in web site

www.synopsys.com/partners/tapin

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Summary

- V-SDC provides a recording of common RTL-to-gate optimizations
- V-SDC can be used to better correlate between the RTL and gate implementations
- V-SDC reduces setup, improves performance, and removes design iterations for equivalence checking tools
- V-SDC is available today and supported by major Synopsys flows

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