

## Enabling the SystemVerilog Ecosystem with the *Verification Methodology Manual for SystemVerilog*

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Product Line Manager  
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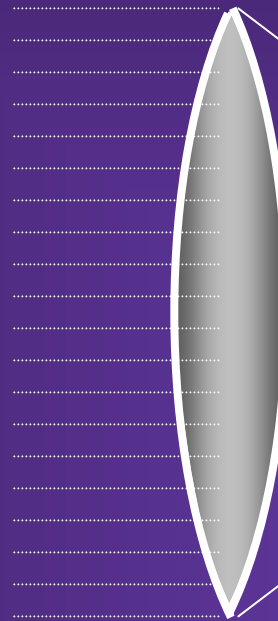


# Good Methodology is Essential to Capture the Power of SystemVerilog

## SystemVerilog Language Features

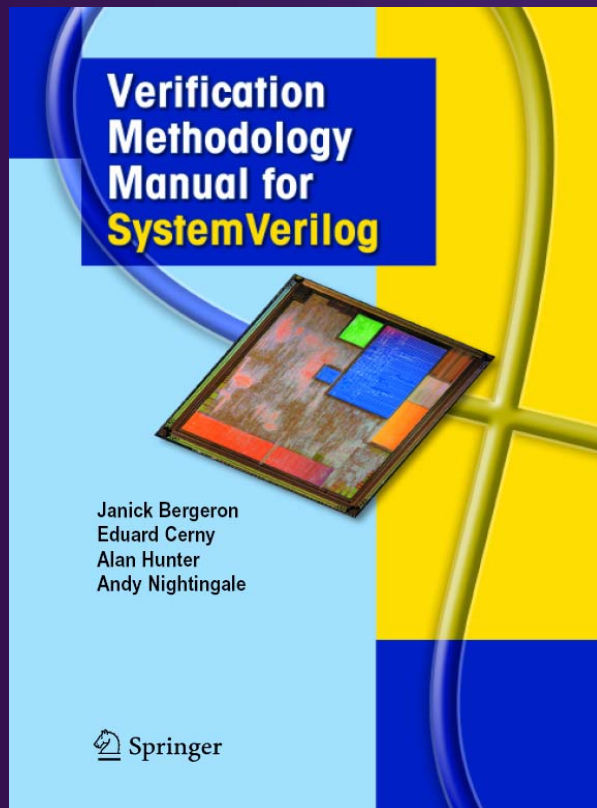
*Coverage Groups*      *Pass/Fail*  
*Events*      *Virtual Methods*  
*Assertions*      *Coverage-Driven*  
*Classes*      *Inheritance*      *Abstraction*  
*Random Generation*      *Interfaces*  
*Assertion Coverage*      *Transactors*  
*Configuration*      *Solver*      *Constraints*  
*Messages*      *Coverage Points*  
*Verification IP*      *Data Structures*  
*Self-Checking*

## Reference Methodology



**Find More Bugs  
in Less Time!**

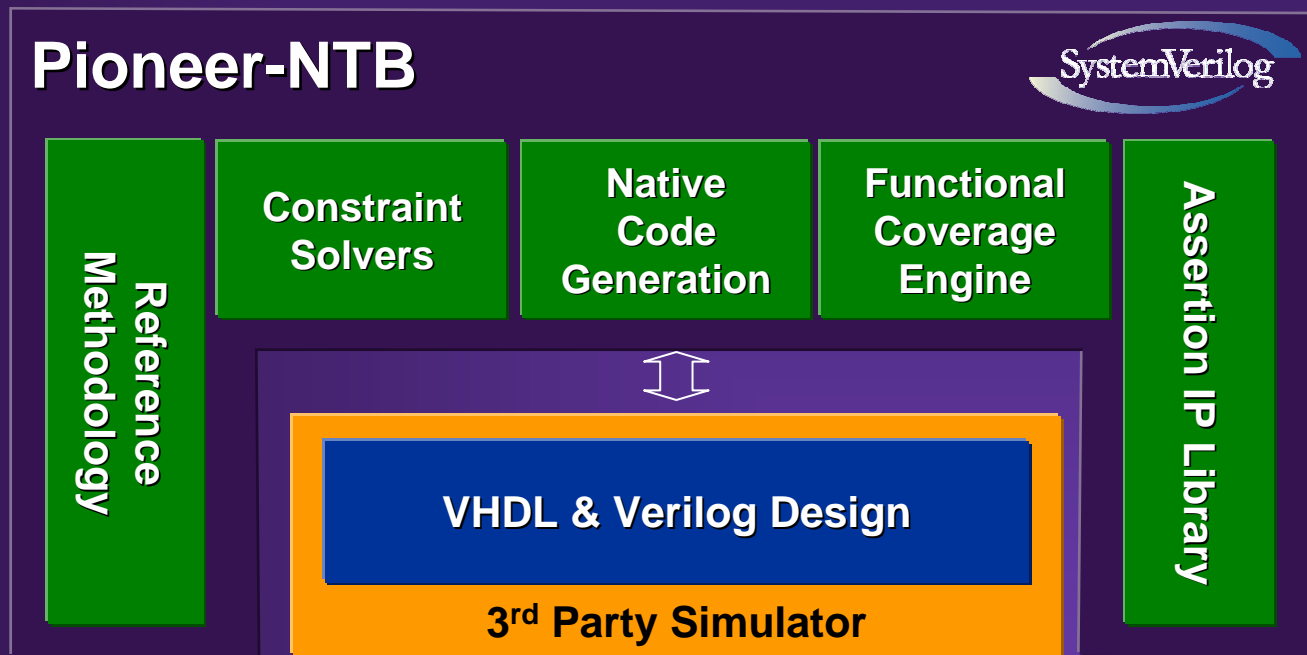
# ARM and Synopsys Collaborate to Address Verification Challenge



- Co-authored *Verification Methodology Manual (VMM) for SystemVerilog*
  - Based on experience from ARM and Synopsys experts
- Peer-reviewed by 30+ industry leaders
  - Documents industry best practices
  - Fully compliant with SystemVerilog
- Available now from Springer
- Supported by Synopsys' VCS and Pioneer-NTB

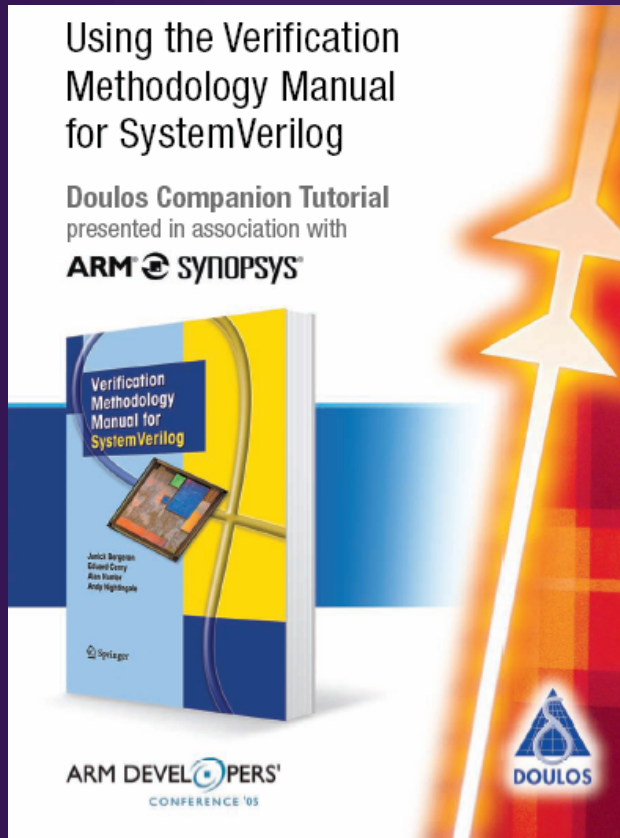
# Pioneer-NTB

## SystemVerilog Testbench Automation Tool



**Open-Standards Based Verification for VHDL & Verilog Designs  
Built on Proven VCS® and Vera® Technologies**

# VMM Launched at Boston SNUG and ARM Developers Conference



**Doulos seminars were popular with users at both events**



**Customers line up to get books signed by the VMM authors**

# Industry Leaders Endorse VMM

The Verification Methodology Manual for SystemVerilog defines the state-of-the-art for advanced, coverage-driven functional verification that engineers can use to increase chip development productivity and quality. This verification methodology is destined to have a significant and enduring impact on the chip development process.



**Tadahiko Nakamura**  
**IP Verification SWG**  
**STARC, Japan**

The Verification Methodology Manual for SystemVerilog is an invaluable reference for verification engineers. It enables users to elevate SystemVerilog from a collection of language constructs into a state-of-the-art methodology for coverage-driven functional verification.



**Mike Benjamin**  
**Functional Verification Group Manager, HPC IP and Design**  
**STMicroelectronics**

SystemVerilog is emerging as the hardware design and verification language of choice, but choosing the right language is only part of what is needed to develop a complete solution. The Verification Methodology Manual for SystemVerilog provides both strategies and details on how to use SystemVerilog's advanced capabilities to create efficient, modern, interoperable coverage-driven verification environments.



**Michael Garcia**  
**Design and Verification Methodology Manager**  
**Freescale Semiconductor**

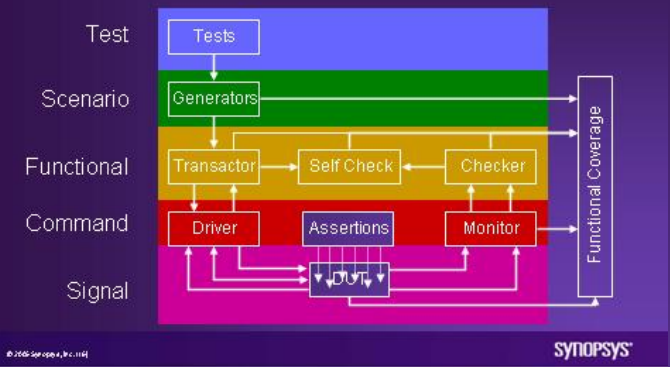
# VMM Enables Efficient, Interoperable Verification Ecosystems

- **High-productivity methodology**
  - Minimizes code writing for tests
  - Enables multiple levels of reuse
- **Widely applicable**
  - Block, chip, and system-level verification
  - Multiple application domains
- **Interoperable, plug-and-play VIP**
- **Consistent, universal training & services**

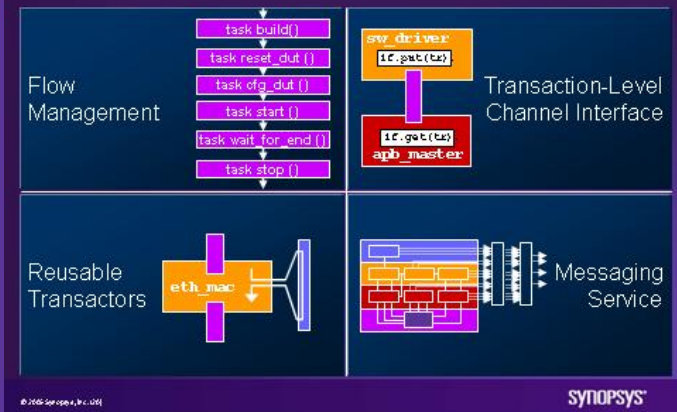
# What Does VMM Provide?

- A reference methodology
  - Verification architecture
  - Documented best practices
  
- Verification building blocks
  - VMM Standard Library
  - Fully specified in book

## VMM Layered Testbench Architecture



## VMM Standard Library Features



# Synopsys Announces VMM Standard Library Source Code License

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## Synopsys Announces Source-Code License for SystemVerilog Verification Library

### VMM Standard Library Enables Adoption of Techniques in the ARM-Synopsys Verification Methodology Manual (VMM) for SystemVerilog

MOUNTAIN VIEW, Calif., September 21, 2005--Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, today announced the availability of the SystemVerilog source code for its implementation of the VMM Standard Library, a base-class library to accelerate the adoption of the SystemVerilog standard for verification. The VMM Standard Library is specified in the ARM-Synopsys book *Verification Methodology Manual for SystemVerilog*, announced by Springer Science + Business Media, Inc. today. The library enables users to adopt the advanced verification techniques and methodology advocated in the book more quickly and easily.

# VMM Standard Library Source Code License Details

- Offered to SystemVerilog Catalyst members and Synopsys customers at no additional charge
  - Compiled version included with VCS and Pioneer-NTB
- Compliant with IEEE 1800 SystemVerilog
- License allows re-distribution of compiled library
- Available December 2005

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