



SYNOPSYS®

**Welcome to the 16th EDA
Interoperability Developers' Forum**

***Developing a
SystemVerilog Ecosystem***



> Your Interoperability Partner

November 9, 2005



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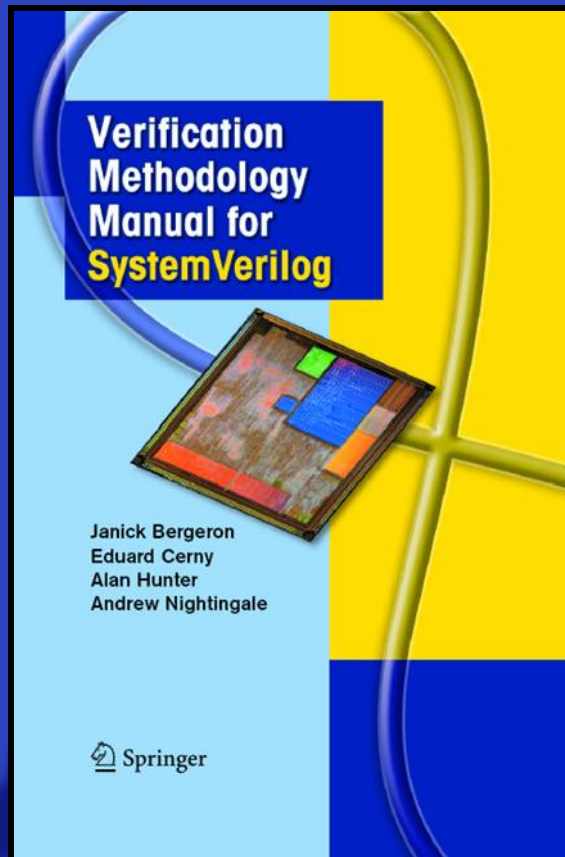
Tom Borgstrom
Product Line Manager,
Verification Group
Synopsys, Inc.



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 *Your Interoperability Partner*

Stick Around and Win!



- Raffle at end of session
 - An iPod® nano
 - 2 copies of *Verification Methodology Manual for SystemVerilog* (VMM)
 - \$50 gift certificate to the Blue Chalk Café in Palo Alto



Take Advantage of Synopsys' SystemVerilog Catalyst Program

- Advancing SystemVerilog-based tool and IP interoperability and availability
- Open to: EDA vendors, verification IP companies and training services providers
- Qualified access to Synopsys' SystemVerilog-based tools: VCS[®], Pioneer-NTB, HDL Compiler[™], LEDA[®], VMM Standard Library

www.synopsys.com/partners/systemverilog



SystemVerilog Catalyst Members

Agenda

- IEEE P1800 SystemVerilog Update
- SystemVerilog and VMM at ARM
- Enabling the SystemVerilog Ecosystem with VMM
- VMM Standard Library Overview
- VMM Deployment: Experience from the Field
- Coverage Driven Verification with SystemVerilog
- Use, Analysis and Debug of SystemVerilog Assertions
- SystemVerilog Productivity is VeriEZ

*Presentations will be available for download after November 23 at:
www.synopsys.com/devforum/nov2005/presentations*