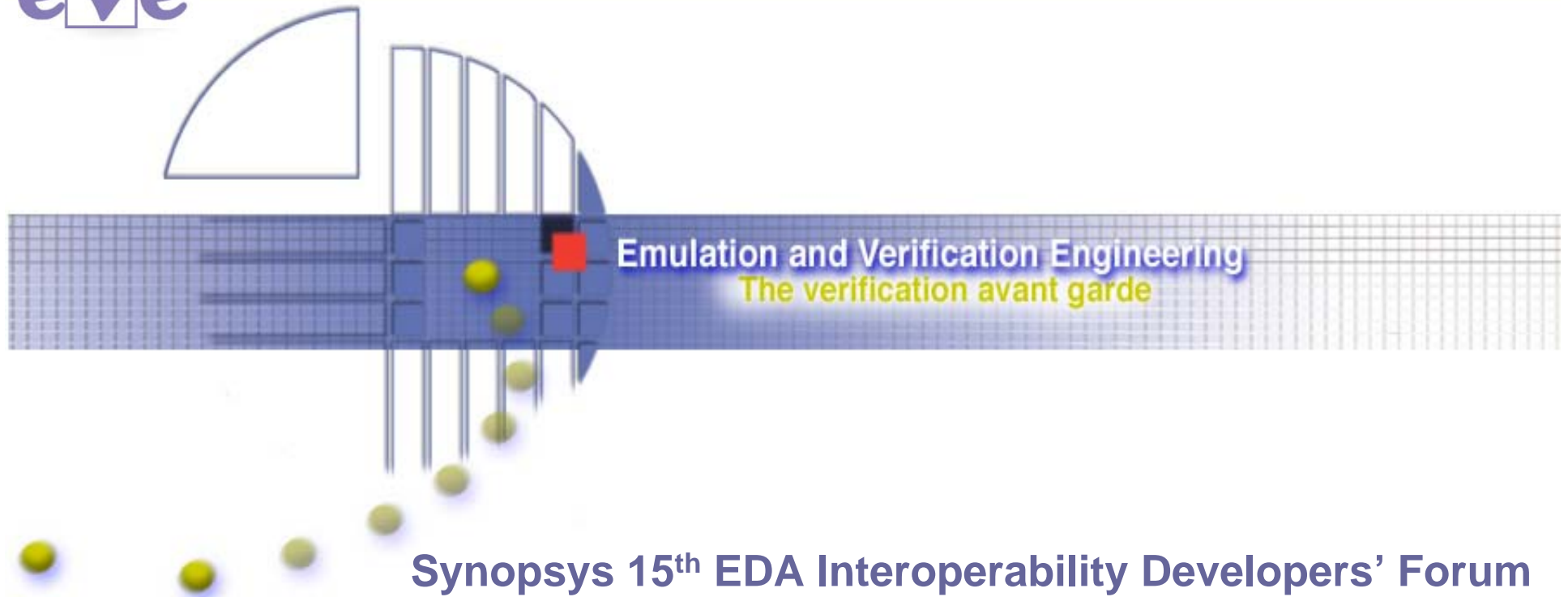


SystemVerilog-Assertion-Based Verification with ZeBu Hardware-Assisted Platform



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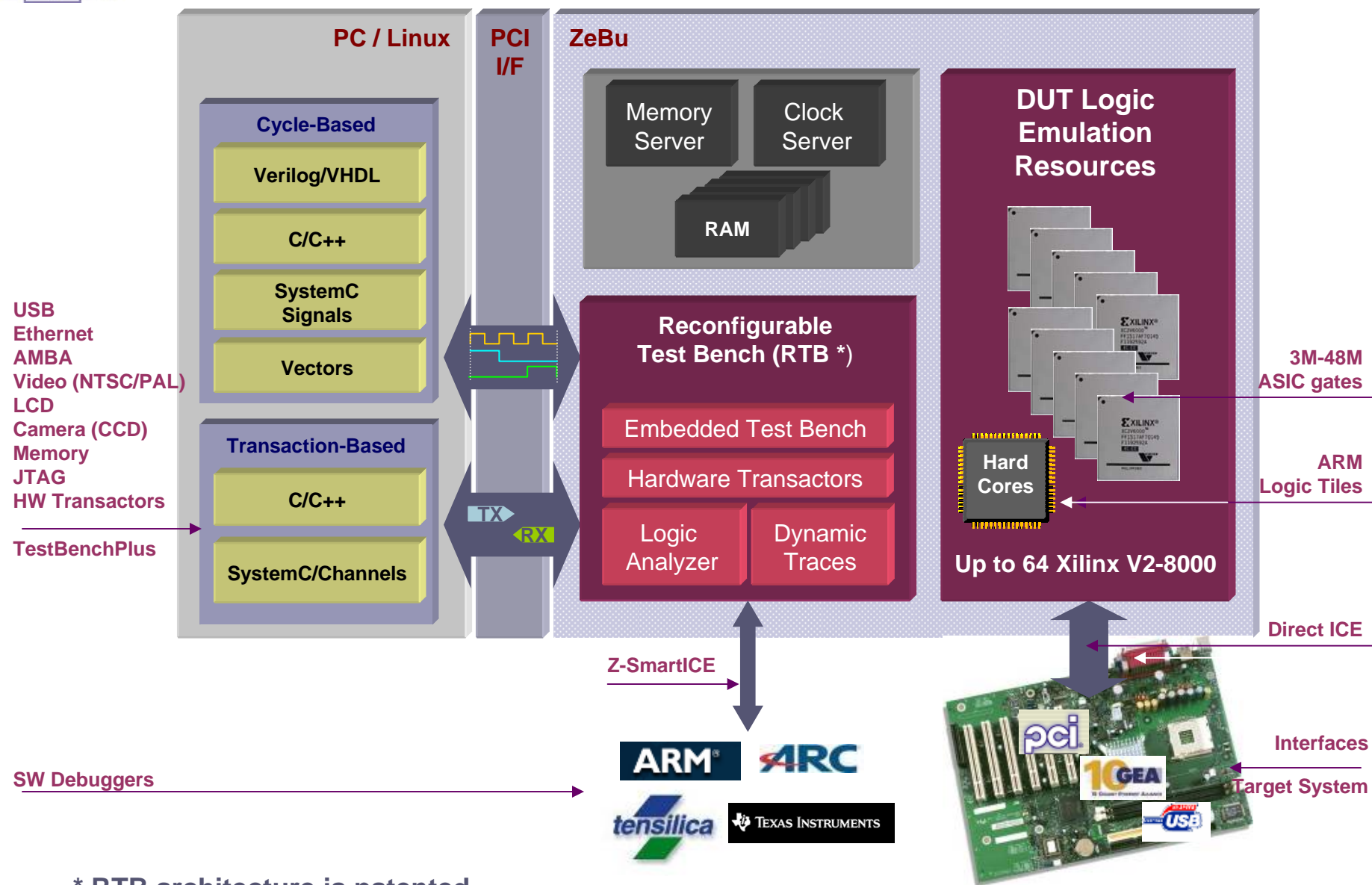
- **ZeBu Architecture Overview**
 - RTB versus DUT
 - ZeBu Compilation Flow

- **Scenario #1: Implementation of SV Assertions in simulation acceleration mode**
 - ZeBu Compilation Flow with SVA
 - ZeBu Architecture with SVA

- **Scenario #2: Implementation of SV Assertions in in-circuit emulation mode**
 - ZeBu Compilation Flow with SVA
 - ZeBu Architecture with SVA



ZeBu Architecture



* RTB architecture is patented



ZeBu Compilation Process

➤ ZeBu compiler performs:

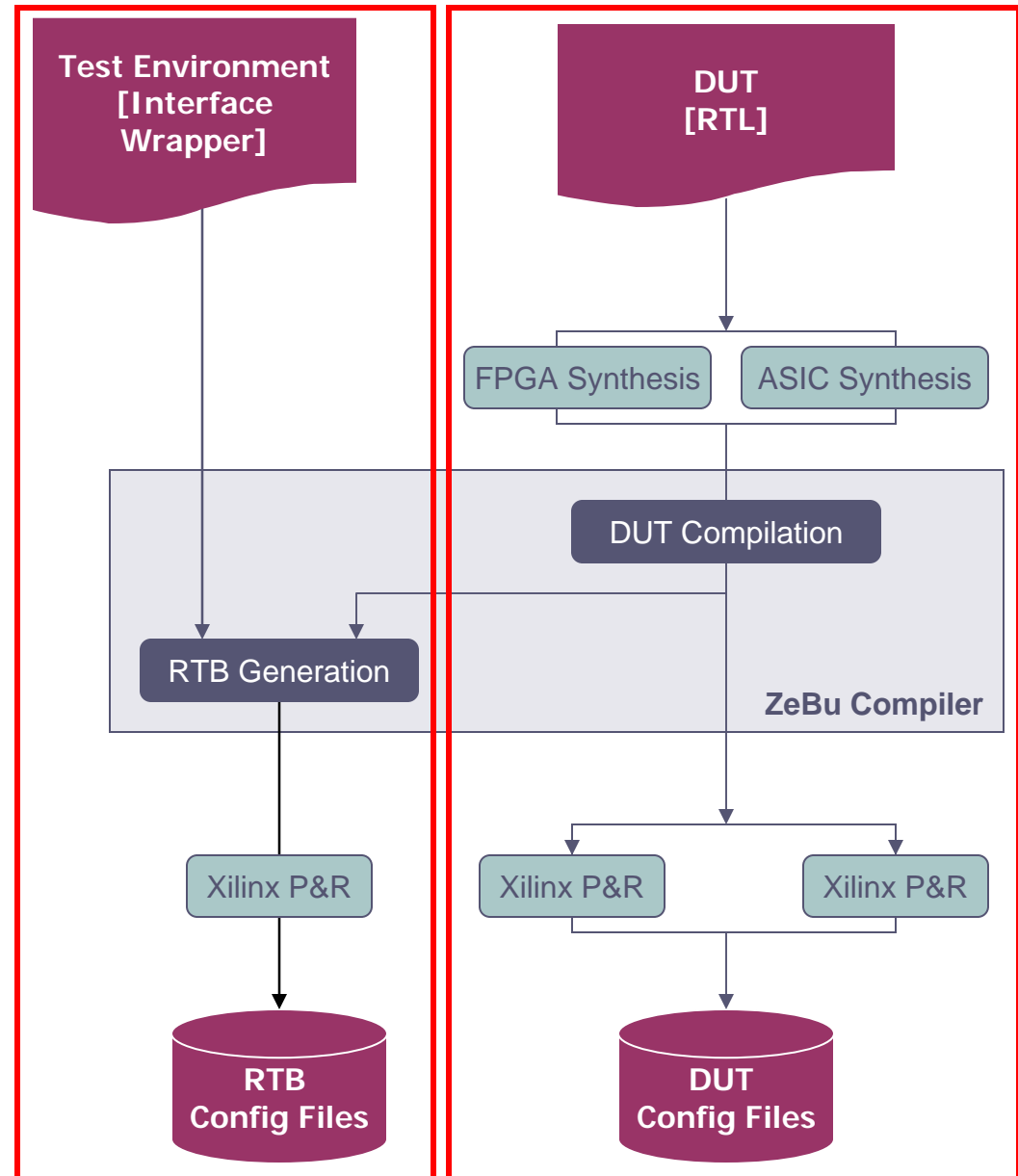
- DUT Compilation
 - Memory Generator
 - Netlist Merger
 - Automated Bus Resolution
 - Automated Clock Processing
 - Automated Clustering
 - Incremental compilation
- RTB Firmware generation
 - Mode/s of operation

➤ Total DUT mapping time (including synthesis, compilation, FPGA P&R):

- 2 hours on a farm of PCs

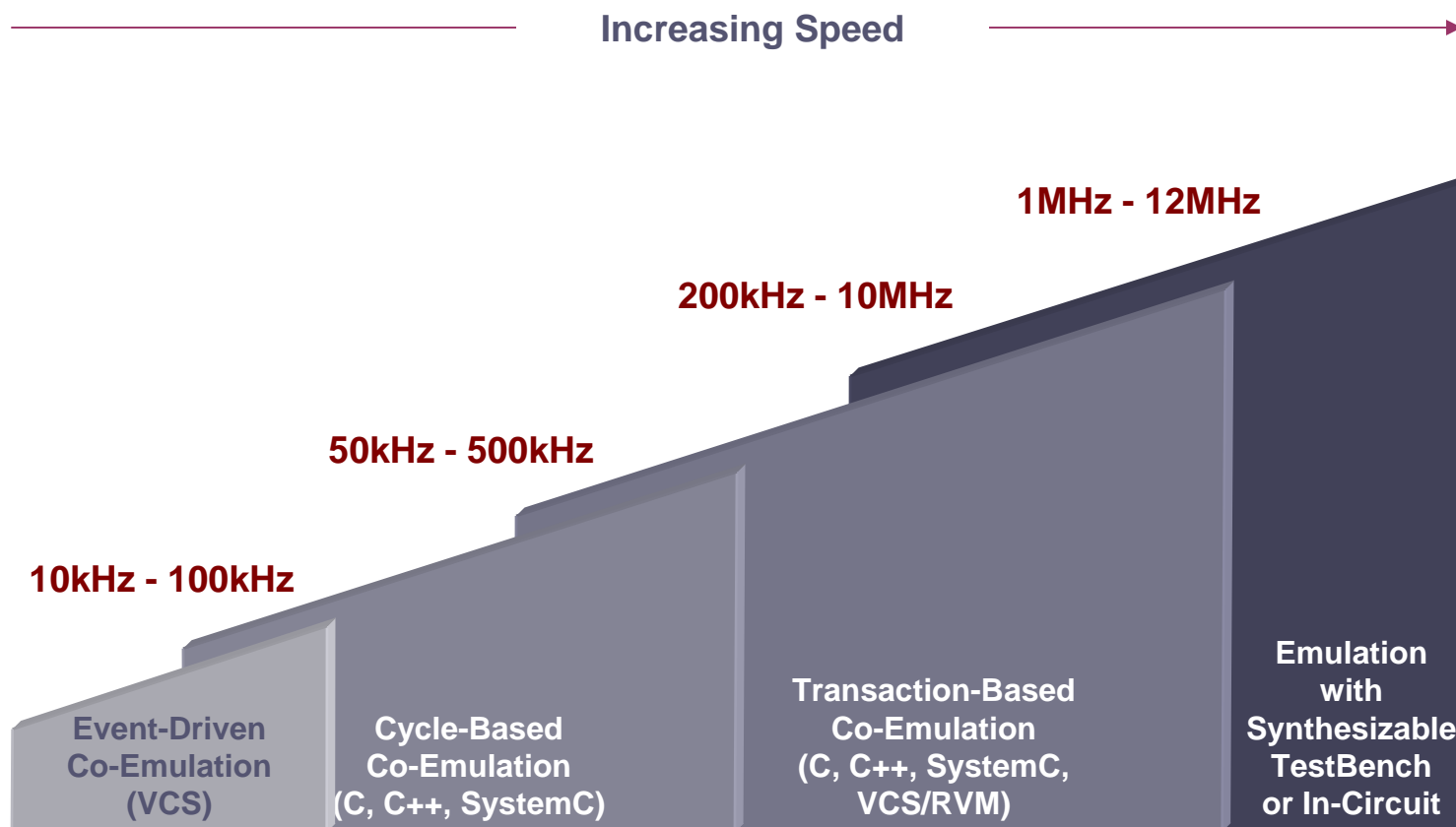
➤ Total RTB generation time:

- Few minutes on one PC





ZeBu Performance





Assertions in SystemVerilog

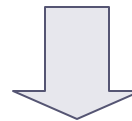
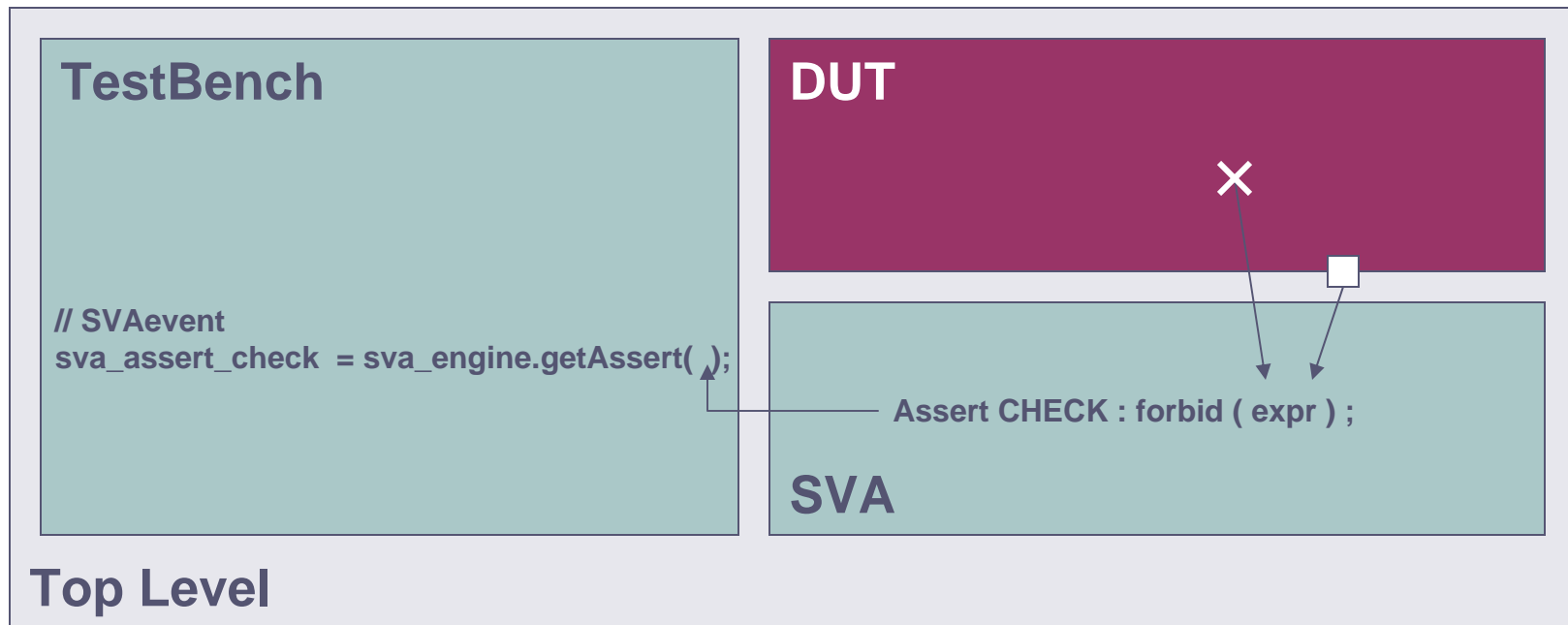
- **Assertions are part of SystemVerilog**
 - Interoperable with the design (Verilog / mixed HDL) & TB

- **SystemVerilog Assertions**
 - Concurrent Assertions
 - Procedural Assertions

- **SVA can be embedded within or separate from the design**
 - **In-line Assertions**
 - **Black-box Assertions**



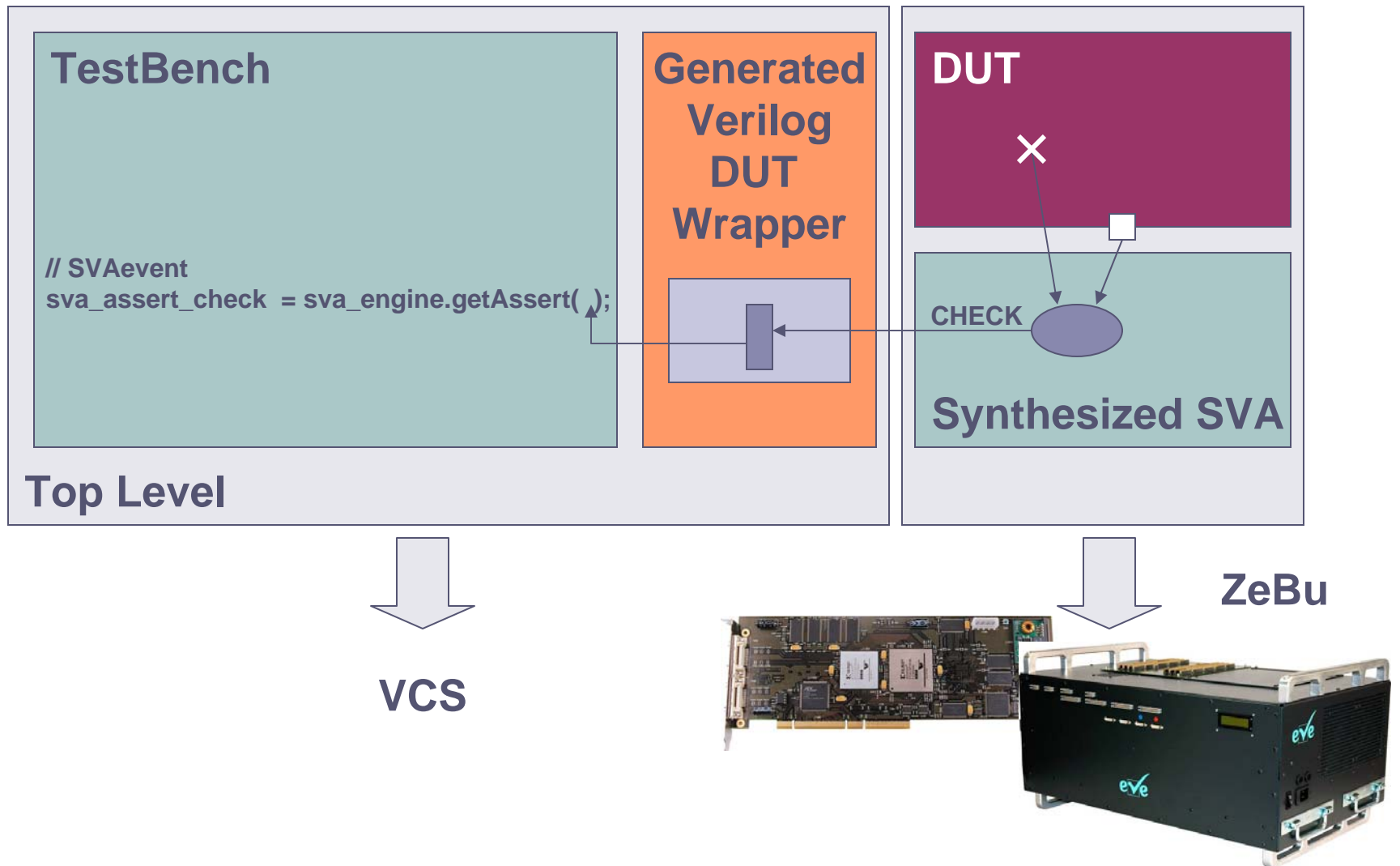
Scenario #1: Simulation with SVA



VCS



Scenario #1: Simulation Acceleration with SVA

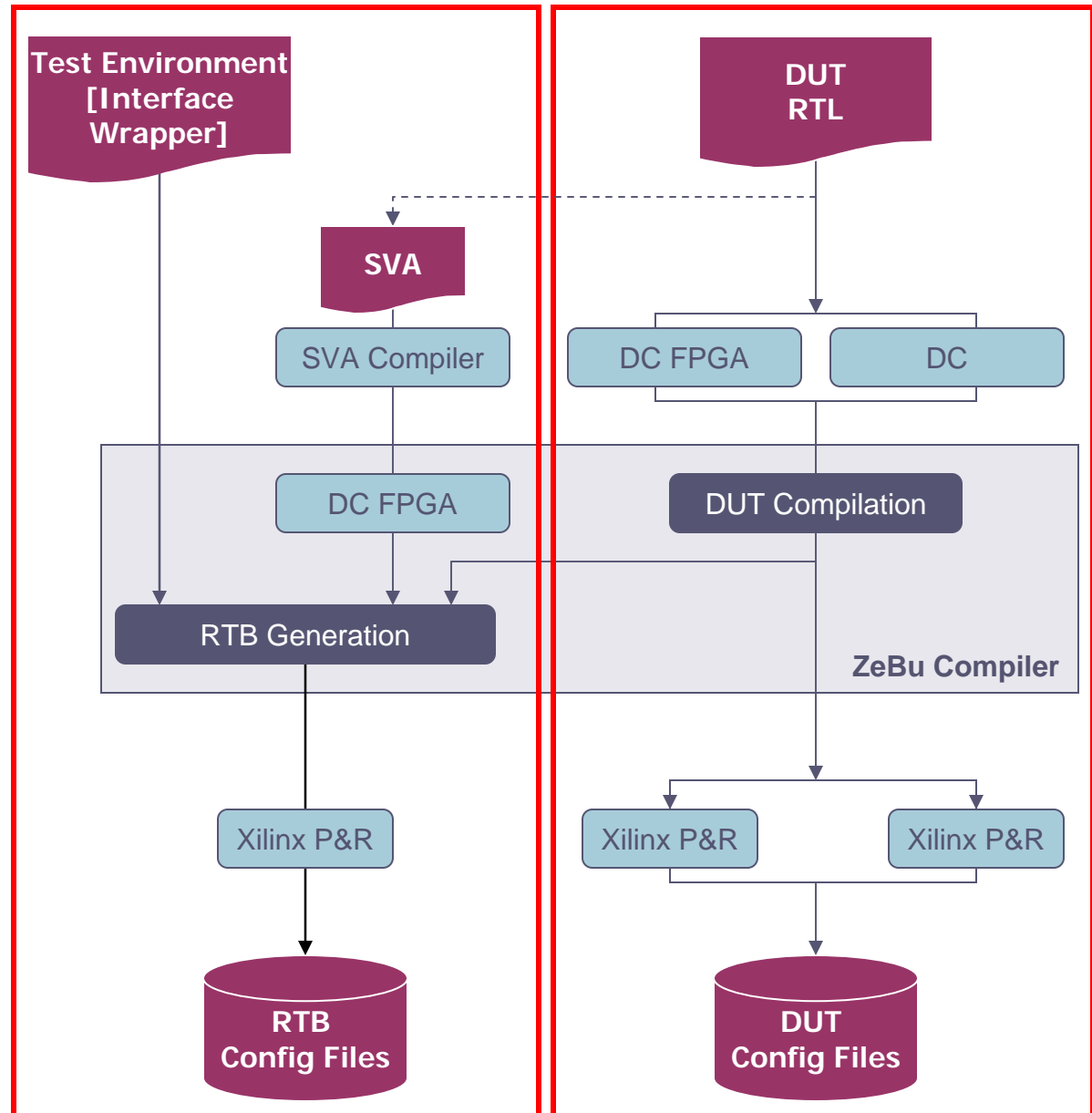




Scenario #1: ZeBu Compilation Process

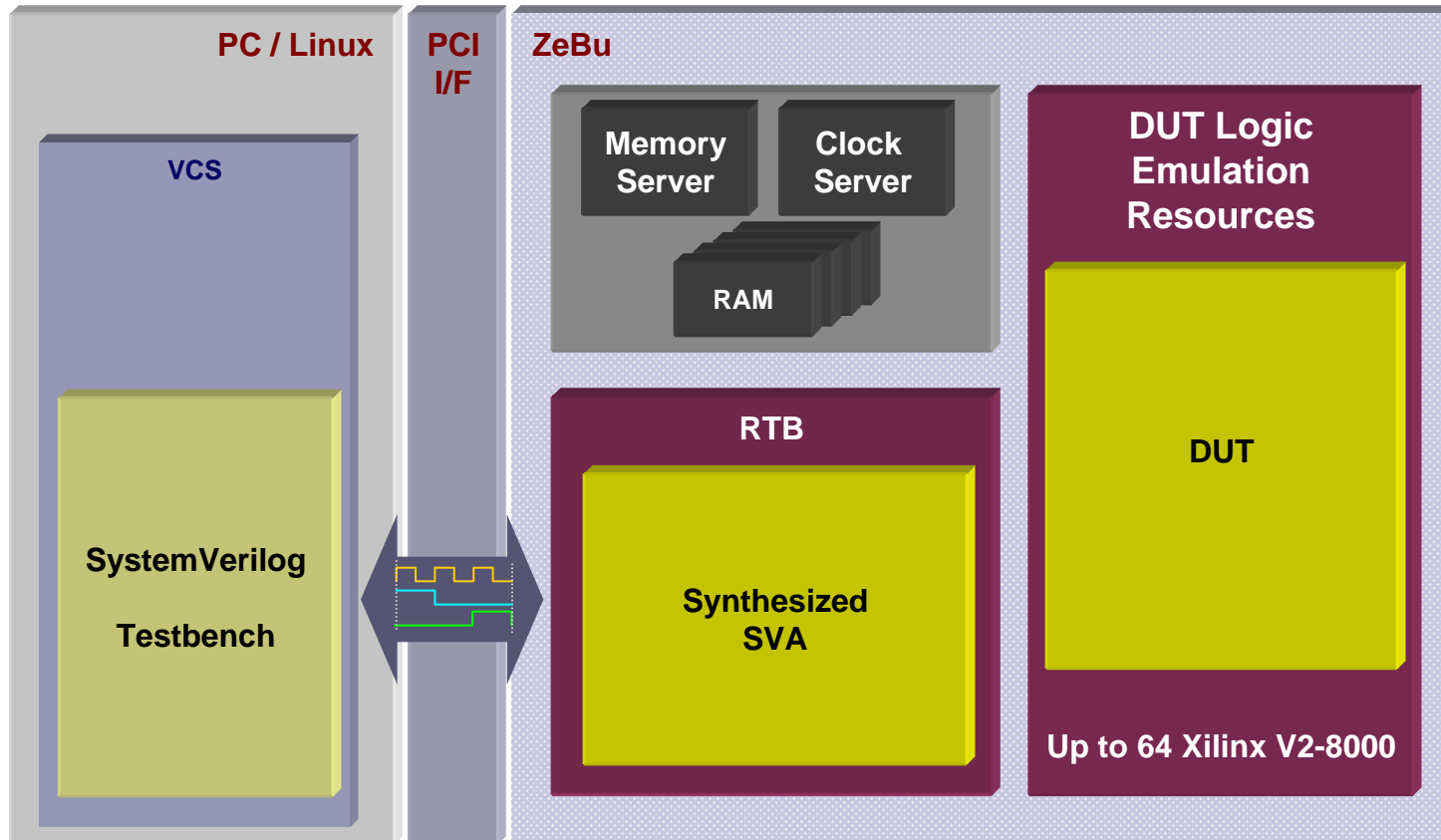
➤ ZeBu SVA Integration:

- Synthesizable SVA Generation with SVA Compiler + DC FPGA
- Synthesis of DUT with DC-FPGA (or DC)
- Merge with Interface wrapper
- Incremental RTB compilation:
 - No need to re-compile DUT
 - 5' with a single PC





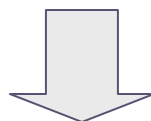
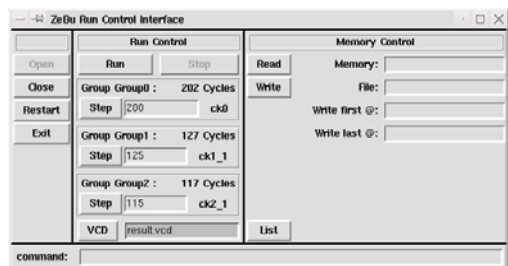
Scenario #1: TestBench and SVA with ZeBu





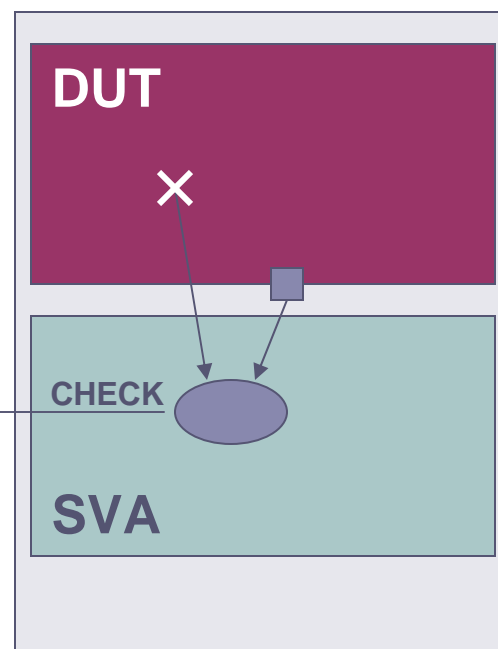
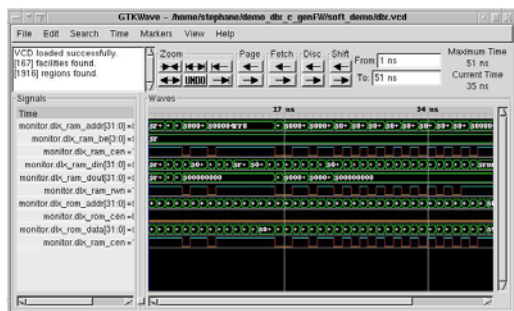
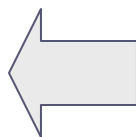
Scenario #2: In-Circuit Emulation with SVA

ICE Control Panel



HW Logic Analyzer:

- HW Triggers
- Trace Memory
- VCD Generation



➤ SVA at run-time with ICE:

- Connection to HW triggers to control emulation run and trace capability
- Assertion monitoring and tracing (at speed) for further assertion coverage and firing analysis



Target System



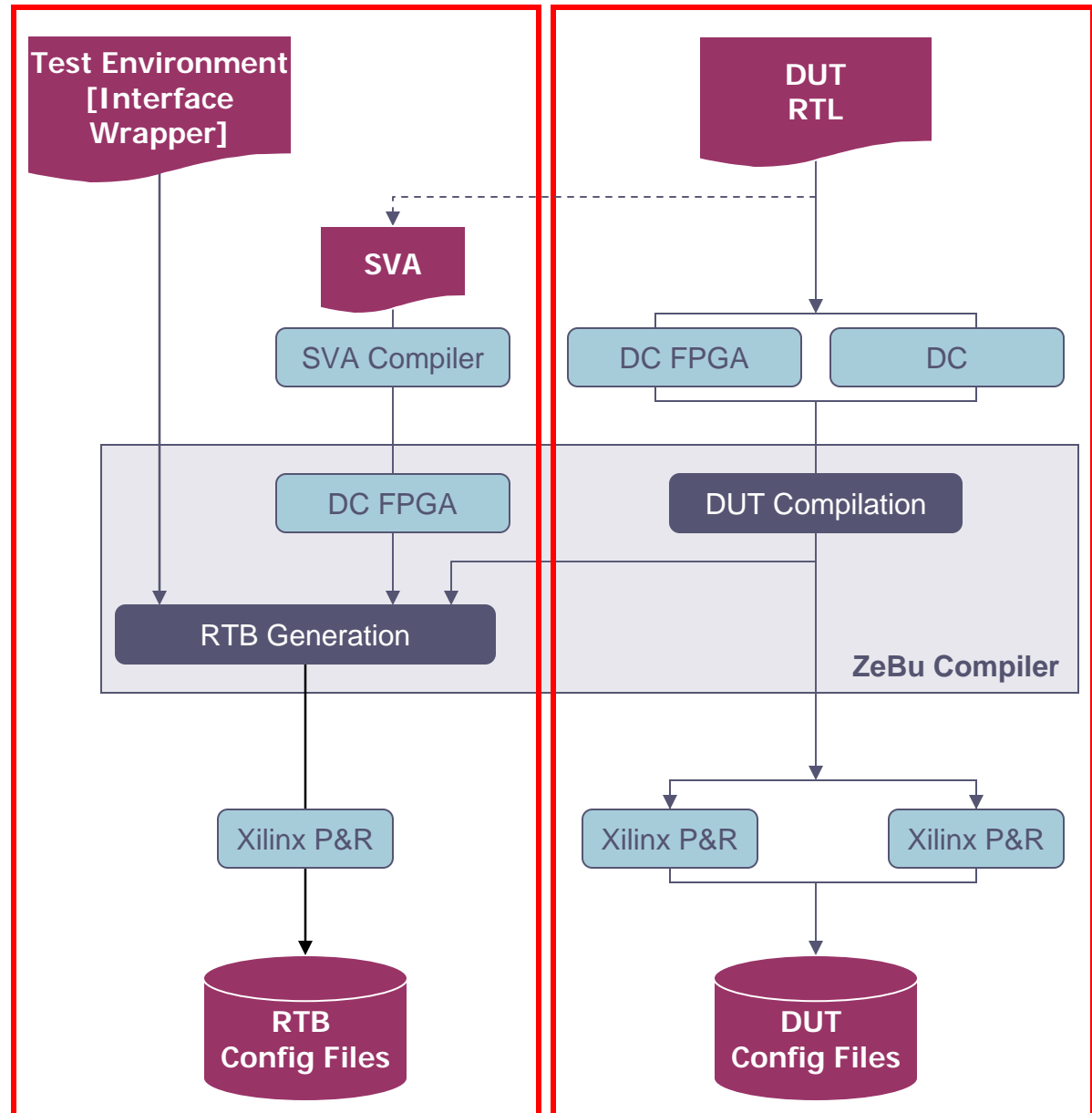
ZeBu



Scenario #2: ZeBu Compilation Process

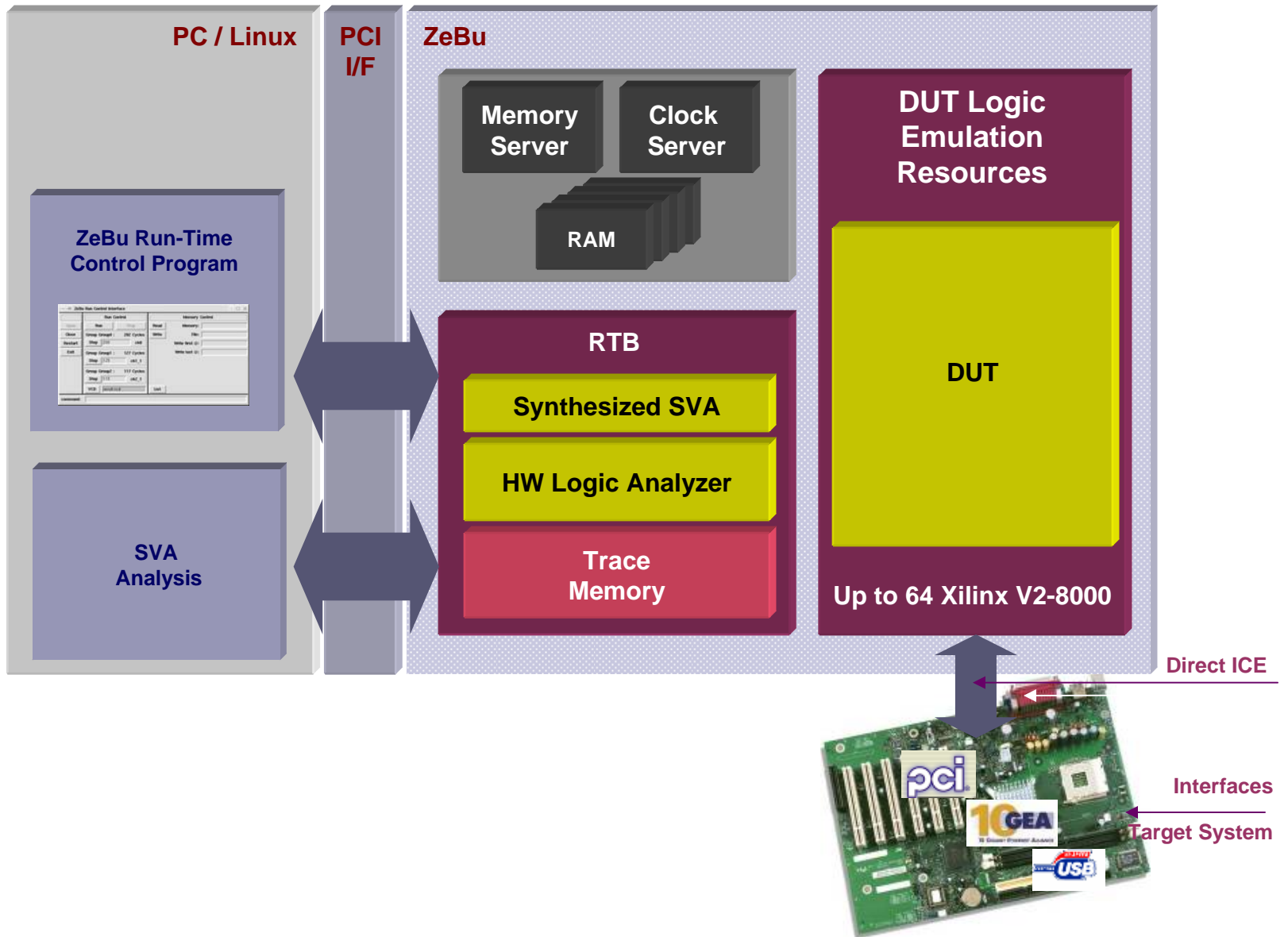
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Scenario #2: In-Circuit Emulation with SVA





- **EVE is uniquely positioned to exploit the power of SystemVerilog Assertions in a hardware-assisted verification flow**

- **The flexibility and versatility of the ZeBu platform effectively support :**
 - **Synthesizable assertions with Testbenches in acceleration mode**
 - Automatically-generated wrapper to make assertions transparent to testbench (as if they were in simulation)

 - **Synthesizable assertions in in-circuit emulation**
 - Assertion coverage (Functional coverage)
 - Assertion firing analysis (Illegal condition occurred)