



SYNOPSYS®


Welcome to the 15th EDA Interoperability Developers' Forum

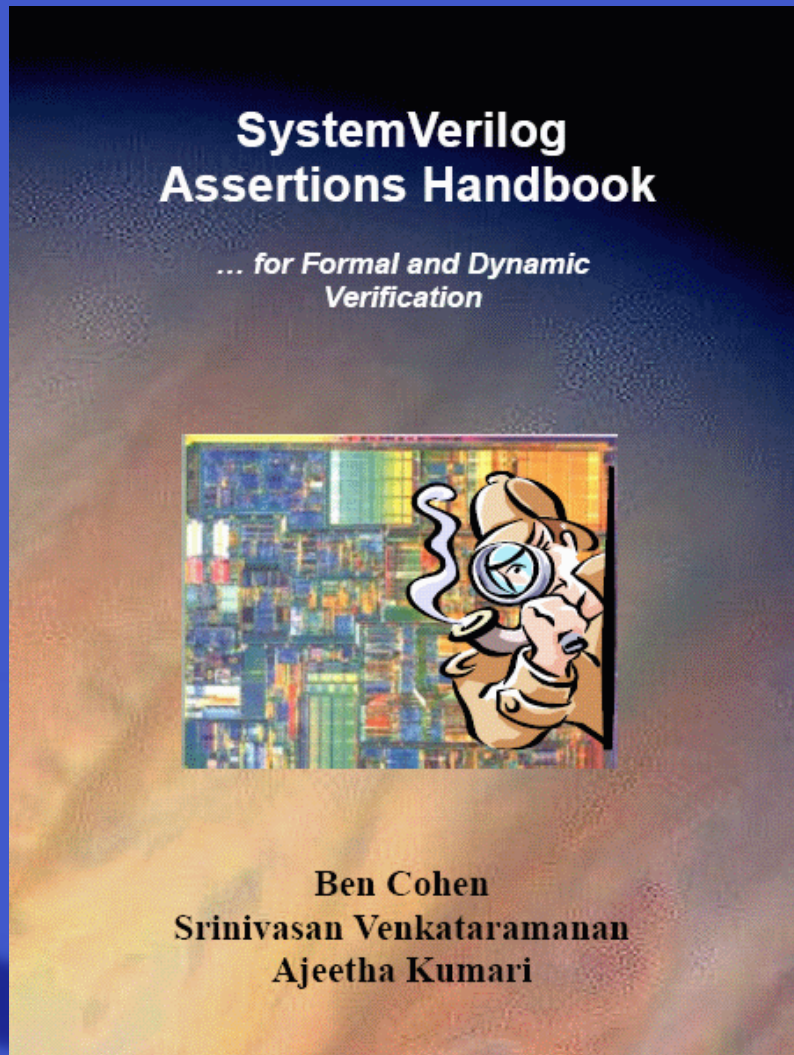
SystemVerilog Forum

sponsored by



April 7, 2005

 *Your Interoperability Partner*



- Look for a star to win SystemVerilog Assertions Handbook
- Bring star to registration desk to claim prize during break



Get involved!


- Join IEEE SystemVerilog Working Group
 - IEEE P1800™ - Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language

<http://www.eda.org/sv-ieee1800>

- Visit Accellera's SystemVerilog web site
 - Download version 3.1a LRM and reference documents
 - Post your company's product information

www.SystemVerilog.org




 *Your Interoperability Partner*



- Join Synopsys' SystemVerilog Catalyst Program
 - Advancing SystemVerilog-based tool and IP interoperability and availability
 - Open to: EDA vendors, Verification IP companies and Training services providers
 - Qualified access to Synopsys' SystemVerilog-based tools: VCS[®], HDL Compiler[™], LEDA[®]

www.synopsys.com/partners/systemverilog



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SystemVerilog Catalyst Program Members



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Agenda

- User's Perspective on SystemVerilog – Jon Michelson, CISCO
- SystemVerilog API – Synopsys
- Systemverilog Assertions for Mixed-Language Support – Ben Cohen, VHDLCOHEN
- EDA Vendor's Perspective – Jerry Kaczynski, Aldec
- Training Vendor's Perspective – Tim Corcoran, Willamette HDL
- Assertion-Based, Hardware-Assisted Verification – Lauro Rizzatti, EVE-USA
- Assertion-Based Verification of Timing Exceptions – Ajay Daga, Fishtail Design Automation

Stay for raffle for iPod® shuffle at end of session

*Presentations will be available for download from the web at:
www.synopsys.com/devforum/apr2005/presentations*

