


Interoperability Update

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News

- Updates to SDC
- Current versions of common formats
- Tenzing Norgay award nominations



Synopsys Interoperability Programs

- Compute Platforms
- in-Sync
- MAP-in
- SystemVerilog Catalyst
- TAP-in
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SDC Open Source Parser Update

- Current version: 1.4
- Version 1.5 and SDC 2005.06 Application Notes will be available Q3, 2005.
- SDC 1.5 parser will support all previous SDC formats (1.1, 1.2, 1.3 & 1.4)



www.synopsys.com/partners/tapin

New SDC 1.5 Commands

- `set_timing_derate`
 - `[-early] [-late]`
 - `[-clock] [-data]`
 - `[-net_delay] [-cell_delay] [-cell_check]`
 - `derate_value`
 - `object_list`
- `get_<object> [pattern]`
 - In addition to existing `get_<objects>` command
 - Type of objects: cell, net, port, etc...
 - If no pattern specified, `get_<object>` and `get_<objects>` return all objects of that type

SDC 1.5 Enhancements

- Support for the following *new* options to previously supported commands:

get_cells

-of_object

get_nets

-of_object

get_clock_latency

-clock

set_clock_uncertainty

-rise_to / -rise_from

set_clock_uncertainty

-fall_to / -fall_from

set_max_transistion

-clock_path

set_operating_condition

-object_list

Download Current Versions

- Synopsys Open Source Formats:
 - www.synopsys.com/partners/tapin
 - Liberty™ V2004.06
 - V2004.12 available VERY SOON
 - SAIF 2.0
 - SDC 1.4
 - SDC 1.5 available in Q3, 2005
 - OpenVera®: www.open-vera.com
 - Updates available VERY SOON
 - 1.4.2 Testbench LRM
 - 1.4.1 Assertions LRM

Download Current Versions

- Milkyway™ Access Program (MAP-inSM):
 - MDE/C-API V2004.06

www.synopsys.com/partners/mapin

- Open SystemC™ Initiative:
 - V2.1 Reference Simulator released & publicly available
 - IEEE P1666 Working Group for SystemC
 - V2.0.1 LRM transferred to IEEE for standardization
 - V2.1 LRM completion & transfer to IEEE targeted for April 2005

www.SystemC.org
www.eda.org/systemc



Get involved!

- Join IEEE SystemVerilog Working Group
 - IEEE P1800™ - Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language

www.eda.org/sv-ieee1800

- Visit Accellera's SystemVerilog web site
 - Download version 3.1a LRM and reference documents
 - Post your company's product information

www.SystemVerilog.org



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5th Annual Tenzing Norgay Interoperability Achievement Award

- Presented to an EDA company that
 - Surpasses common levels of interoperability
 - Contributes to overall industry advancement
 - Provides a new view of the future
 - Ensures customer success



*Tenzing Norgay
on Mt. Everest*

Tenzing Norgay Award

■ Previous winners:

- CoWare (2001)
- Mentor Graphics (2002)
- Silicon Metrics (2003)
- Novas (2004)

■ 2005 Nominees

- @HDL
- ARM
- Atrenta
- Electronic Tools Company
- Library Technologies
- Verific Design Automation
- Zenasis



And the winner...



**...will be announced at the
Synopsis Interoperability Breakfast
Event at DAC**

Wednesday, June 15, 2005



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16th EDA Interoperability Developers' Forum

- Thursday, October 13, 2005
- Located in Silicon Valley
- Invite your colleagues
- Want to speak?



Thank you!

Wait, there's more...



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Coming Up Next:
SystemVerilog Forum



- But first, we want your feedback.
- Complete your feedback form now and qualify for the prize drawings for a Sony PSP and a Delphi XM Satellite Radio.