

IEEE P1800 Status Report

Synopsys EDA Interoperability Developers' Forum

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The SystemVerilog logo, featuring the text 'SystemVerilog' in a blue serif font, with a green and yellow swoosh underneath it.

SystemVerilog

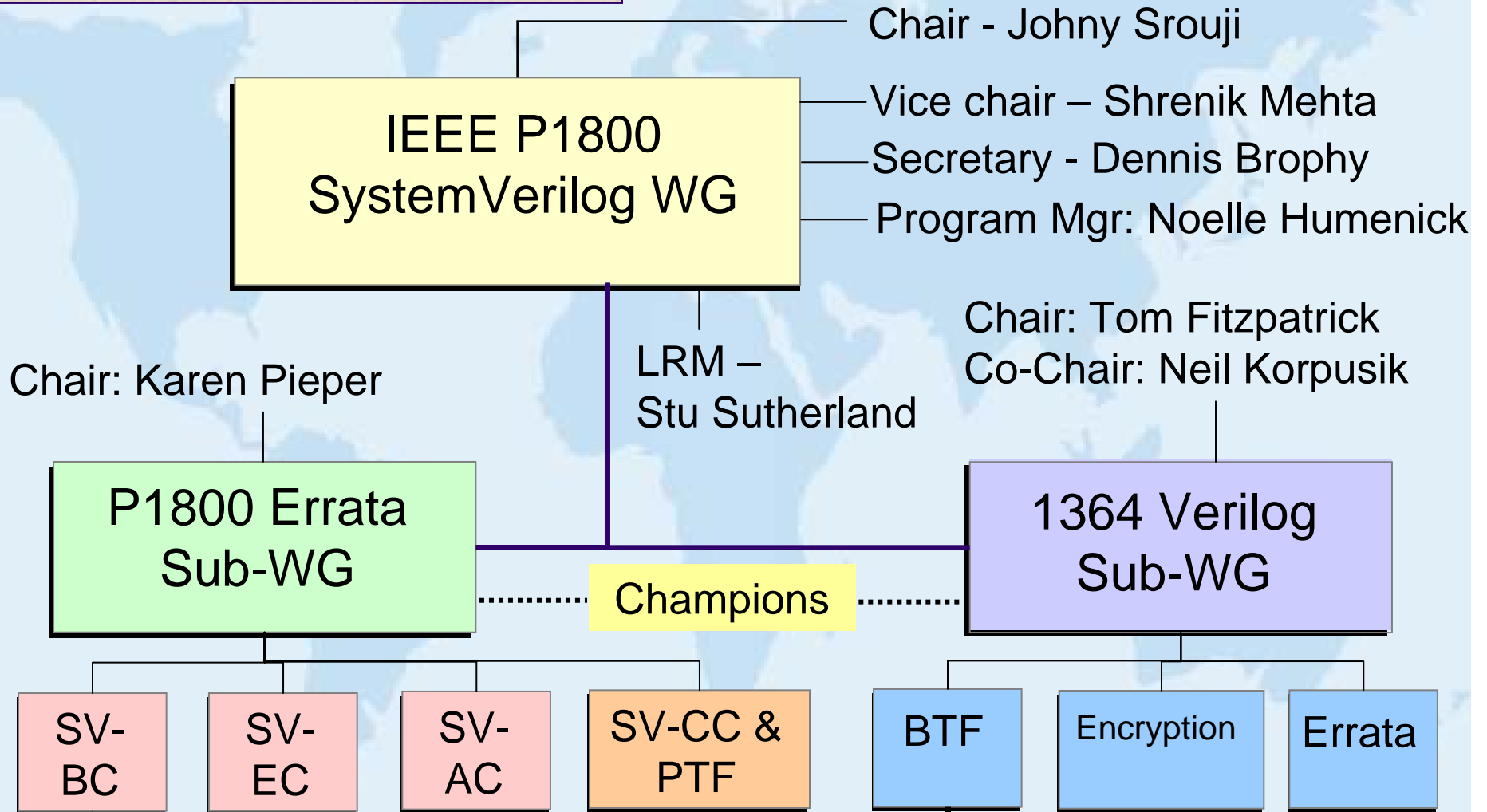
Agenda

- Organization & Structure
- Main Goals – *The Big Picture*
- Progress
- Ballot Status & Initial Results
- Next Mile Stones
- How can you participate?
- Contacts

Organization

- Over 50 members on iee1800 reflector
- 11 active members from Users' and EDA entities
- Elected Officers:
 - Chair: Johny Srouji, IBM corporation
 - Secretary: Dennis Brophy, Mentor Graphics
 - Vice-chair: Shrenik Mehta, SUN corporation

IEEE P1800 Structure



P1800 Goals - The Big Picture

- Publish and Ballot SystemVerilog LRM
 - Draft by DAC 2005
- Publish and Ballot 1364 2005 LRM
 - Errata corrections
 - Consistency
 - Draft by end of 2005
- Publish a single LRM
 - Over the next 2-3 years

Progress

- SystemVerilog & Verilog Drafts and technical issues resolution are on track
- A quality ballot draft for SystemVerilog (Draft4.0) and Verilog (Draft 6.0) were made ready
 - 287 SystemVerilog Issues were resolved by technical committees
- Work-Group got ready for Ballot
 - Ballot resolution processes and timelines were put in place

Ballot Status

- Ballot Drafts were made ready
- Ballot invitations were sent for P1800 and P1364
 - P1800 Ballot Status - 14 entities registered
4 Users; 6 Producers; 4 Others
 - P1364 Ballot Status – 12 entities registered
3 Users; 5 Producers; 4 Others
- Ballot Period: 22 February – 24 March
- Issues Resolution by Technical Committees by April'11
- Ballot Resolution Approvals by WG members by April'19 (F2F meeting)

“Initial” Ballot Results

SystemVerilog P1800

14 eligible entities in this ballot group.

- 11 affirmative votes
- 3 negative votes with comments

→ 14 ballot return = **100%** vs. required rate of 75%

→ 11 affirmative votes = **78% affirmative** vs. required rate of 75%

Verilog P1364

13 eligible entities in this ballot group.

- 10 affirmative votes
- 2 negative votes with comments

→ 12 ballot return = **92%** vs. required rate of 75%

→ 10 affirmative votes = **83% affirmative** vs. required rate of 75%

Major “Next” Milestones

Feb'22-Mar'24, 2005	30-day initial ballot of SystemVerilog Draft4.0 and Verilog Draft6.0
Apr'20, 2005	technical writer prepares SystemVerilog draft5 and Verilog draft7. Secretary prepares ballot comment matrix with dispositions for recirculation. Program manager prepares cover letter to balloters.
May'20, 2005	10-day recirculation ballot of SystemVerilog draft 5 and Verilog draft 7. Results sent to WG chair / sponsor / program manager
Aug'12, 2005	RevCom submission deadline
Sep'21, 2005	RevCom approves P1800 SystemVerilog and P1364 Verilog

Contacts & Participation

- IEEE meetings are open to the public
 - Everyone is welcome to attend meetings and voice their opinions
- Voting membership / balloting
 - By company, requires IEEE-SA membership
- Working Group:
 - Web site: <http://www.eda.org/sv-ieee1800/>
 - Chair: Srouji@US.IBM.com
 - Vice Chair: Shrenik.Mehta@sun.com
 - Secretary: dennisb@model.com