

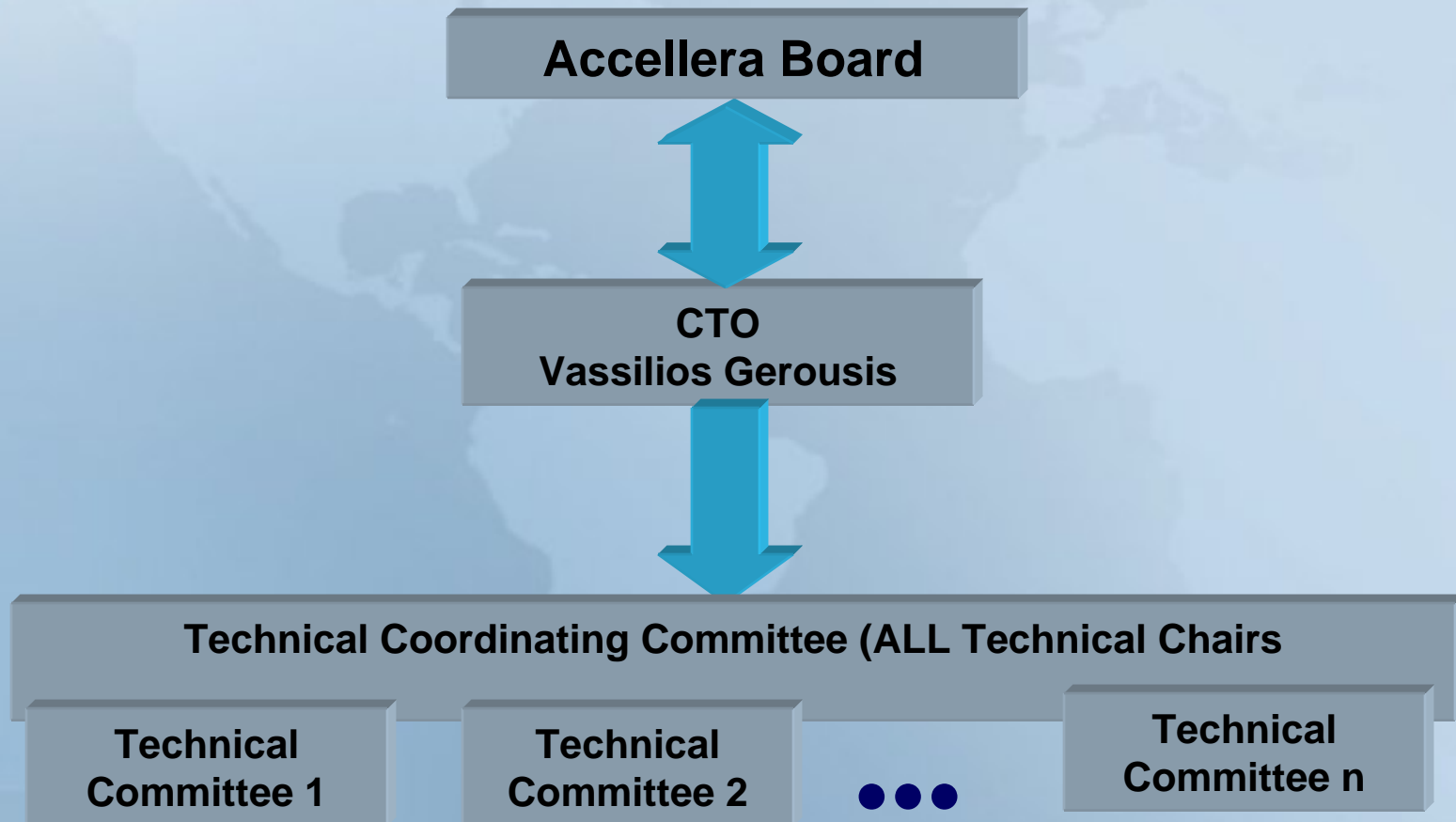


Accellera OK Status

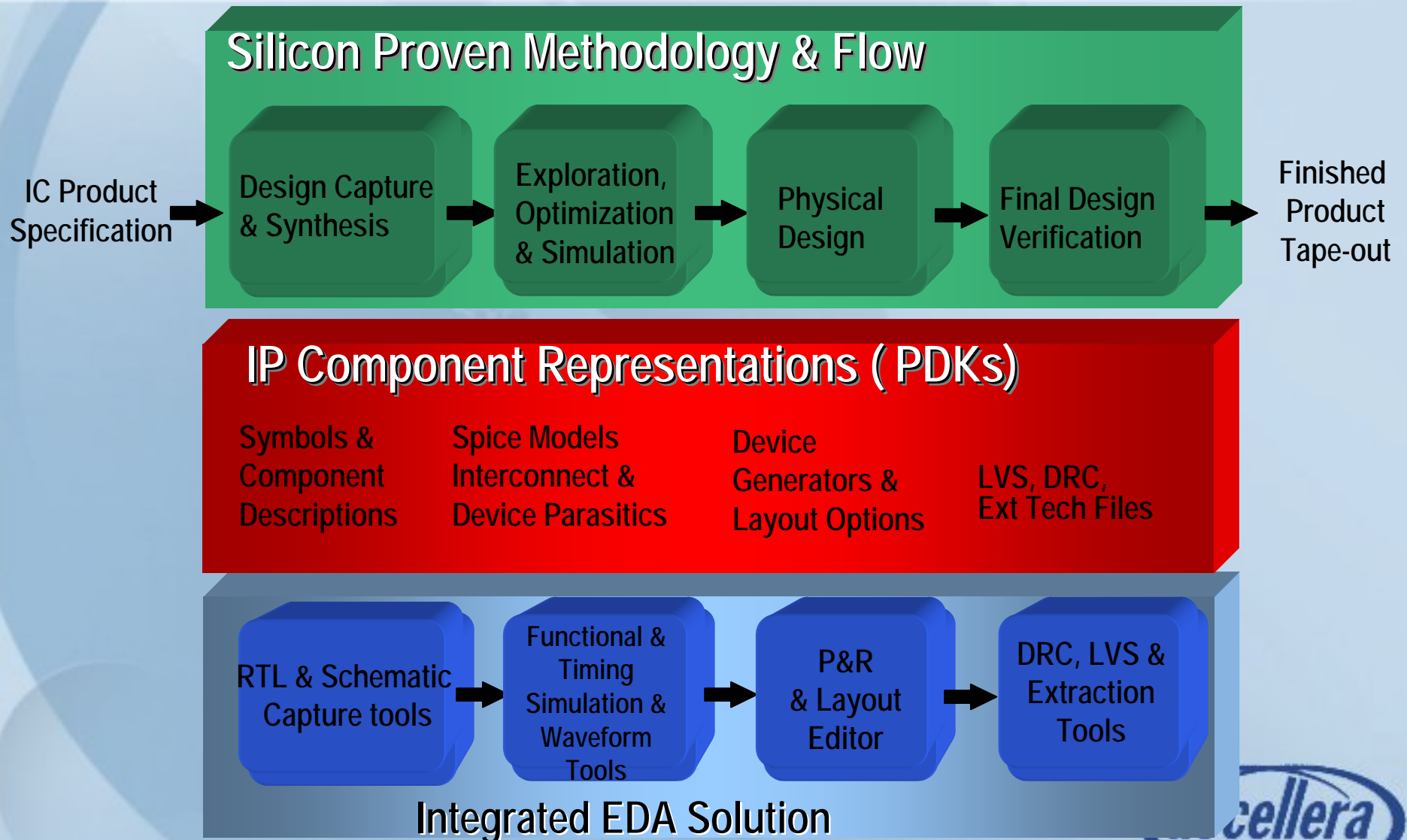
Vassilios Gerousis – Accellera Technical Chairman

Compiled By OK Chairs
Wolfgang Roethig – NEC
Edward Lechner – ARM
Mahmoud Shahram - Synopsys
Paul Koch - Cadence

Accellera Technical Structure



Design Platform Architecture



OK Four Working Groups

- WG1(Symbols) : Paul Koch
- WG2 (Physical) : Wolfgang Roethig
- WG3 (Standard Electrical Spec & Spice Model Format/Template): Mahmoud Shahram
- WG4 (Pcell WG) : Edward Lechner



OK Symbol WG Status

- History

- Defined scope of supported device for symbol standard
- Defined terminology for consistent communication around symbol standards issues
- Defined set of eight symbol footprints to drive initial standards
- Updated target representation to be EDIF 400 (versus 300) because of alignment with Open Access and expanded scope for future extensions (e.g. PCB & SIP)
- Legal issues associated with submission resolved
- Extended symbol library to include comprehensive inductor and transformer symbols

- Update

- Initial symbol set assembled (table, TAR file containing CDBA, OA 2.0 and OA 2.2 versions)
- Total of 67 symbols included in the donation

- Next steps

- Conversion to EDIF 400 and documentation.



OK Physical WG (WG2) Status

- Draft spec for physical rule description under review to prepare for ballot
 - Fully based on IEEE 1603-2003 std (ALF)
 - Staged on OKTC web page
<http://www.accelera.org/apps/org/workgroup/ok-tc/documents.php>
 - Validated with ALF parser/compiler
- Proposed time table for ratification
 - Gathering review comments – e/o January 2005
 - Addressing review comments in spec – e/o March 2005
 - Ready for Accellera board approval – e/o April 2005



Data Exchange WG (WG3) Status

- Electronic data exchange format developed and uploaded to the website for review
- Foundry donation process stalled
- WG3 activities tabled until donation problems resolved



PCELL WG (WG4) Status

- Working Group formed in November 2004
- Great deal of interest in this activity
- Standard pcell devices will be those defined by WG1
- Areas being discussed for standardization
 - Pcell generation language
 - Syntax
 - Evaluation protocols
 - Data representation formats
 - XML, ALF, something other than paper
 - Standard APIs for physical pcell construction



How To Join OK Committee

- Information and public documents are available on
- <http://www.accellera.org/activities/OK/OK>
- To join any of the committees, please send an email to the respective chair
 - WG1 : pkoch@cadence.com
 - WG2 : wroethig@necelam.com
 - WG3 : Mahmoud.Shahram@synopsys.com
 - WG4 : Edward.Lechner@arm.com

