

Welcome to the 14th EDA Interoperability Developers' Forum

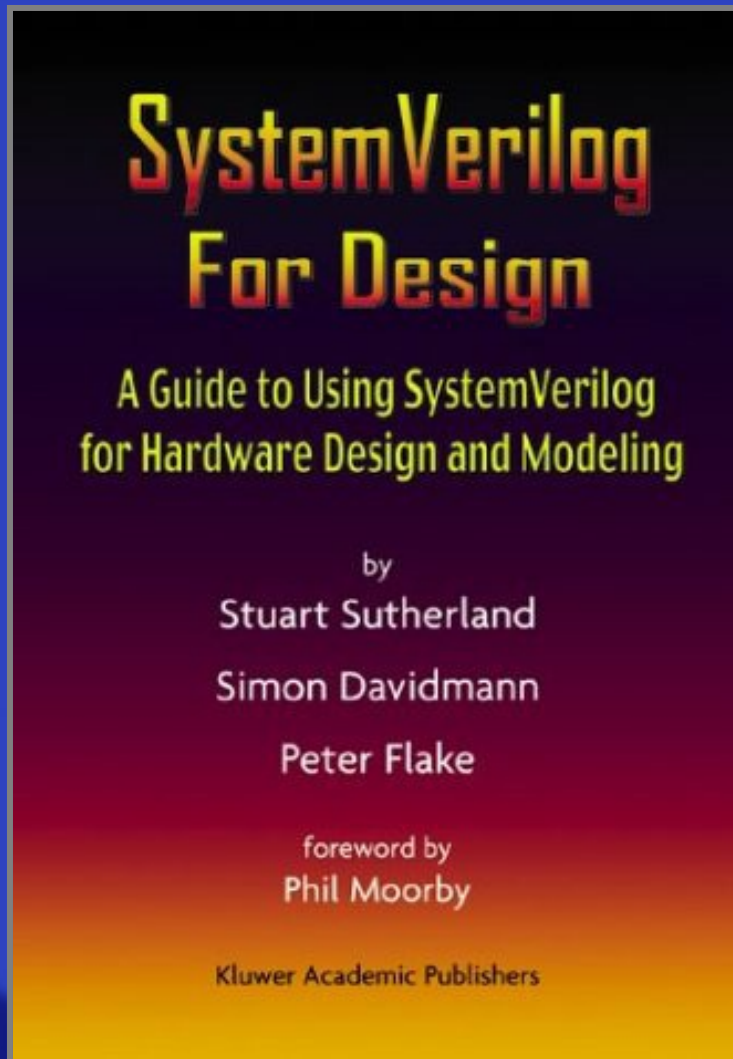
System Verilog Forum

sponsored by



October 21, 2004

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- Look for a star to win SystemVerilog For Design
- Bring star to registration desk to claim prize during break



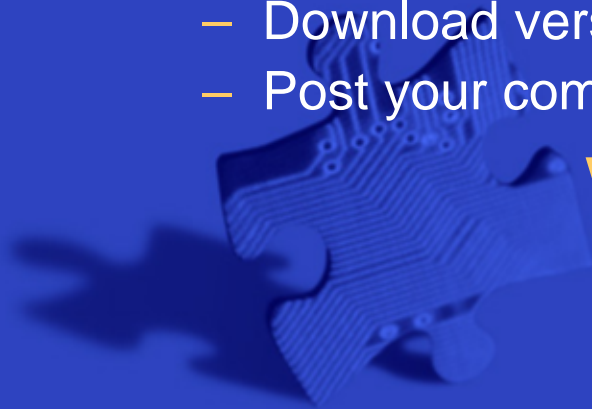
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- Join Synopsys' SystemVerilog Catalyst Program
 - Advancing SystemVerilog-based tool and IP interoperability and availability
 - Open to: EDA vendors, Verification IP companies and Training services providers
 - Qualified access to Synopsys' SystemVerilog-based tools: VCS® , HDL Compiler™ , LEDA®

www.synopsys.com/partners/systemverilog

- Visit Accellera's SystemVerilog web site
 - Download version 3.1a LRM and reference documents
 - Post your company's product information

www.SystemVerilog.org



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Agenda

- SystemVerilog Testbench Update – Synopsys
- User's Perspective on SystemVerilog – Sun Microsystems
- Exploiting SystemVerilog Testbench Support in ModelSim – Mentor Graphics
- Synopsys SystemVerilog Support – Synopsys
- FinSim's Support of SystemVerilog – Fintronic USA

Stay for raffle for iPod® mini at end of session

Presentations will be available for download from the web for attendees at: www.synopsys.com/devforum/oct2004/presentations