Silicon IP for Low Power Design

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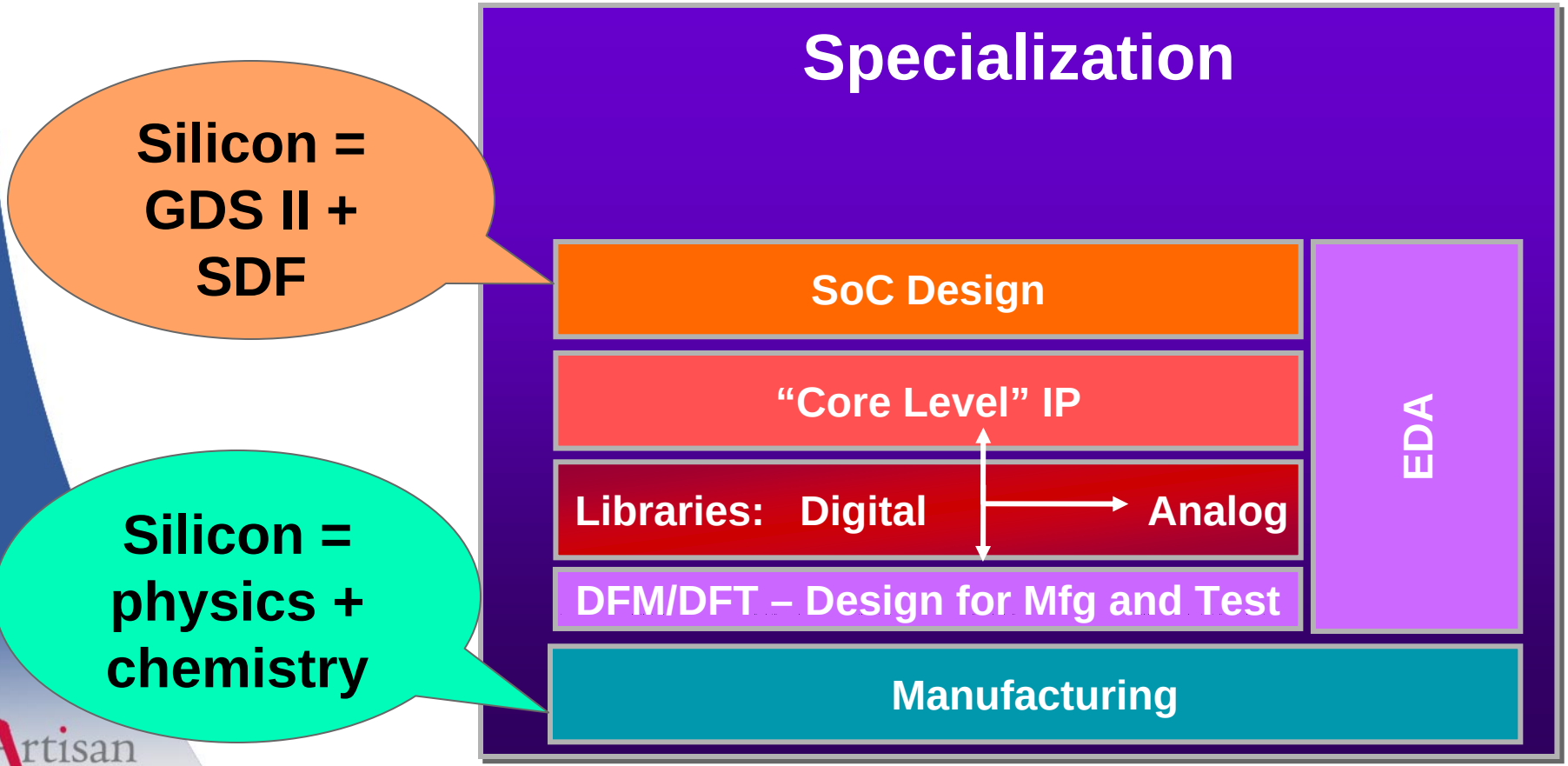
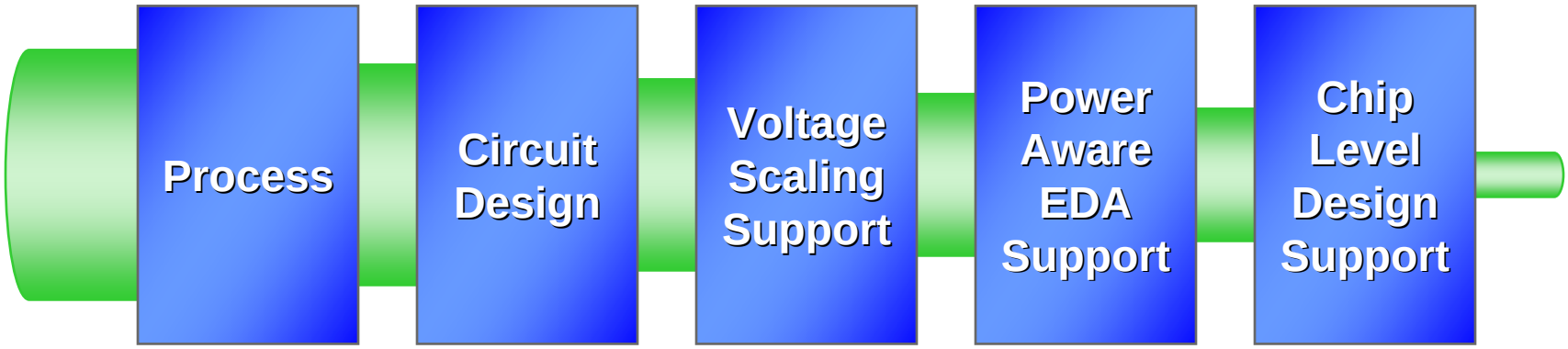
Power: Where Silicon IP Fits

- Silicon IP is the interface between design and process
- Tools cannot exploit features of the process (multi-Vt) or technology (multi-VDD, MT-CMOS) without support from IP



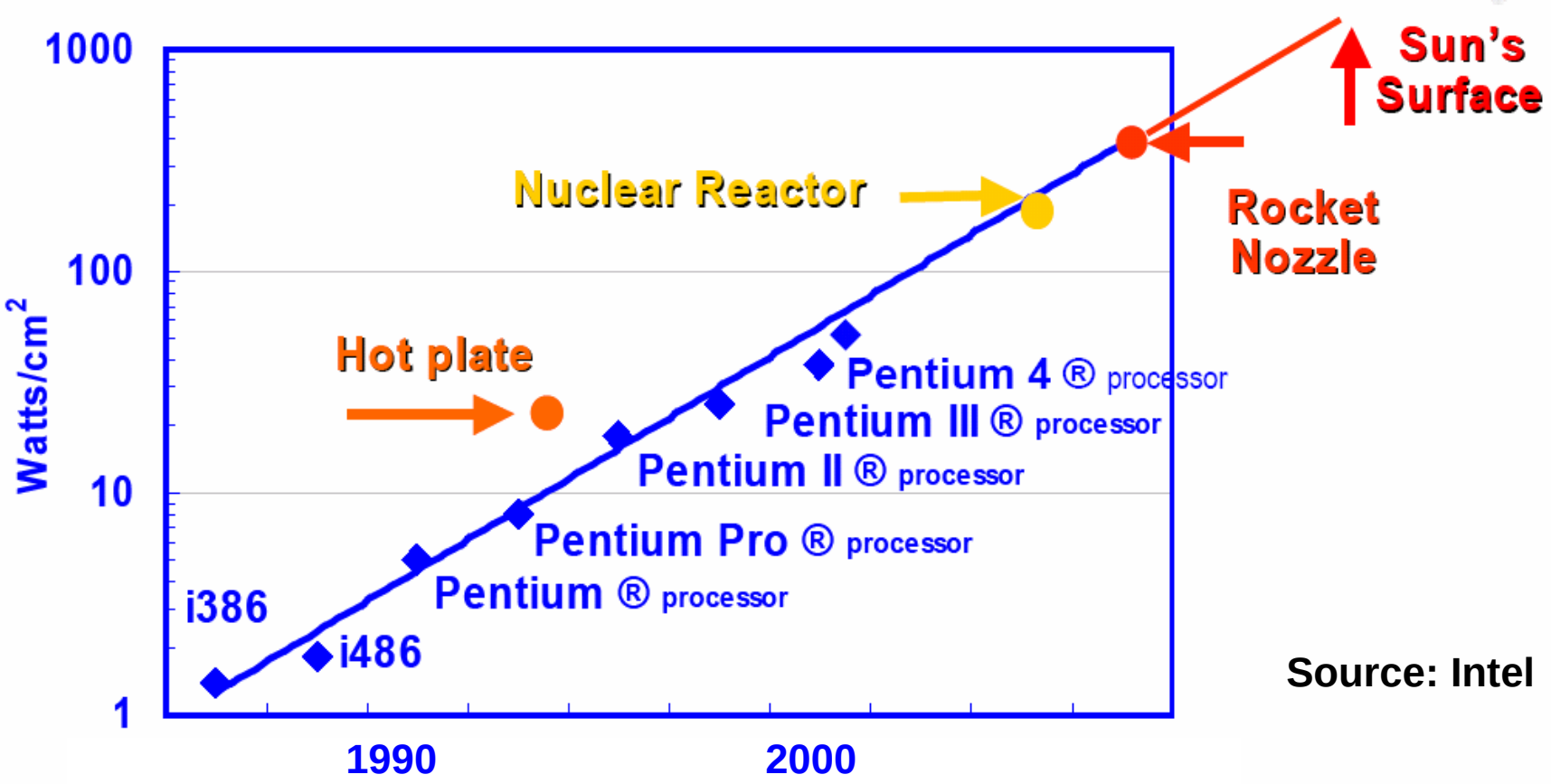
Metro™ Low Power IP Broadly Targeted

METRO™



Process	Circuit Design	Voltage Scaling Support	Power Aware EDA Support	Chip Level Design Support
Low leakage devices	Optimal power & performance tradeoffs	Modeled for multi-voltages	Accurate power models	Full clock gating support
Low area bitcells	Variable & low voltage support	Adjustable memory margin	Multi-voltage timing	Voltage island support
	Expanded margin windows	Level shifters	Leakage/speed synthesis optimization	Analog & mixed signal elements included

Power Panic: Moore Means More



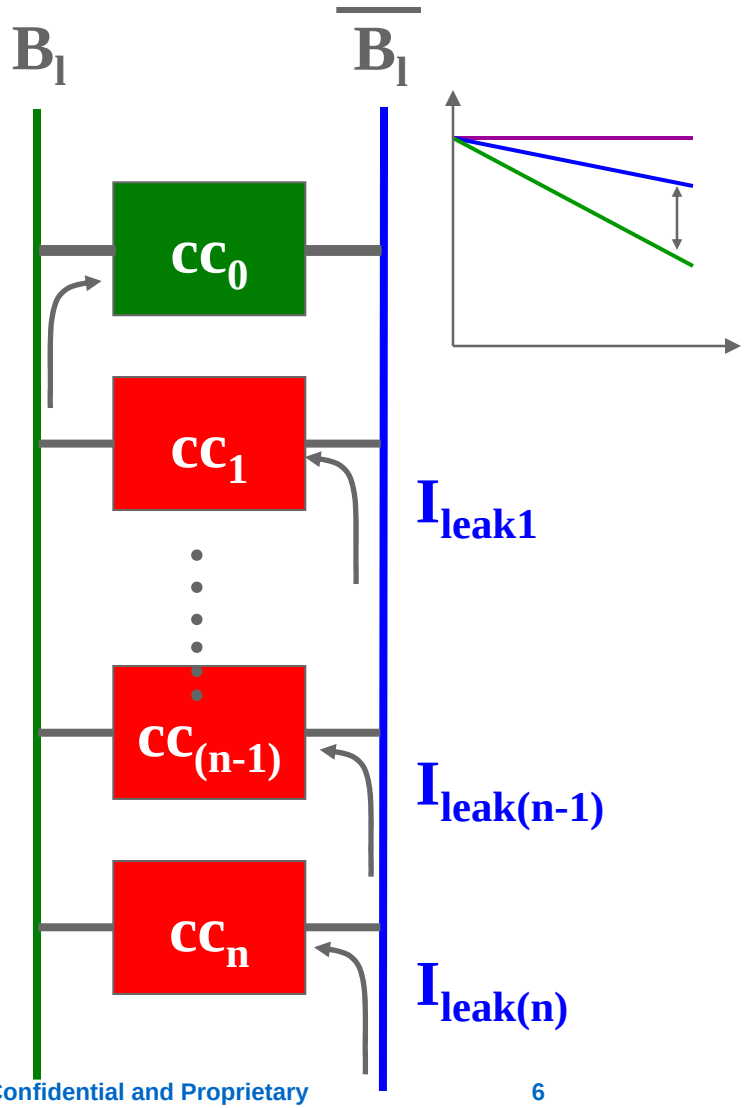
Source: Intel

Outline

- **Power**
  - Leakage reduction
  - Dynamic reduction
  - Examples

Leakage can be a design problem

- Memory performance and functionality affected by leakage
- High Vt implants to reduce leakage have reduced read current
- Fewer rows possible
  - Half as many in 90nm as in 130nm
- Local variations can cause higher than predicted leakage
- Need more offset in matched transistors

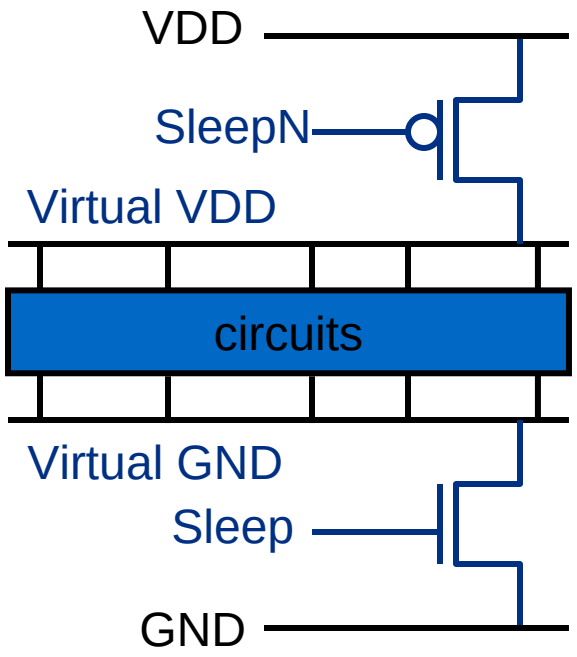


Leakage Management Support at Artisan

- **Multi-Vt standard cell libraries**
  - Footprint compatible (drop in replacement post-placement)
- **Vt optimization in memories**
- **Transistor size optimization**
- **Transistor stacking**
- **Variable transistor length**
- **Multi-voltage islands with Power down modes**
  - retention flops, separate core/periphery power
- **MT-CMOS/ Power gating**
- **Well-biasing**
- **State-dependent leakage power data reported in .lib**

Example: MT-CMOS

- **Use HVT transistors to power down portions of the design**
  - Header, footer, or both
  - 90%+ leakage reduction possible
- **Memory**
  - Periphery only, or with core
- **Basic**
  - For a fixed size group of standard cells
- **Optimized**
  - For an optimized balance (leakage reduction versus switching time)

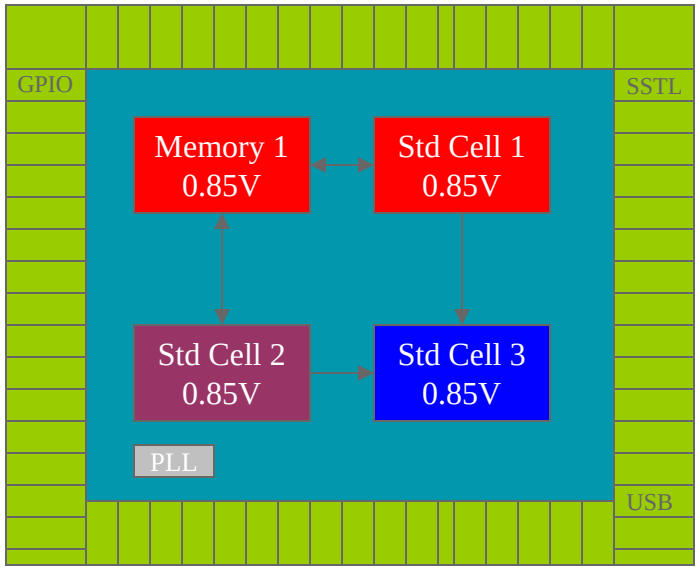


Dynamic Power (CV^2f)

- **Need to reduce C, V, or f**
- **Reduce C**
  - Minimize capacitance switched on every clock
    - Through architecture or clock gating
  - Better device size optimization
  - Compact layout
- **Reduce V**
  - Ultra-low VDD operation (characterization)
  - Multi-VDD support (level shifters, characterization)
- **Reduce f**
  - Turn off clock whenever possible to each block
  - Reduce glitches

Vdd Reduction Approaches

Simple Voltage Scaling



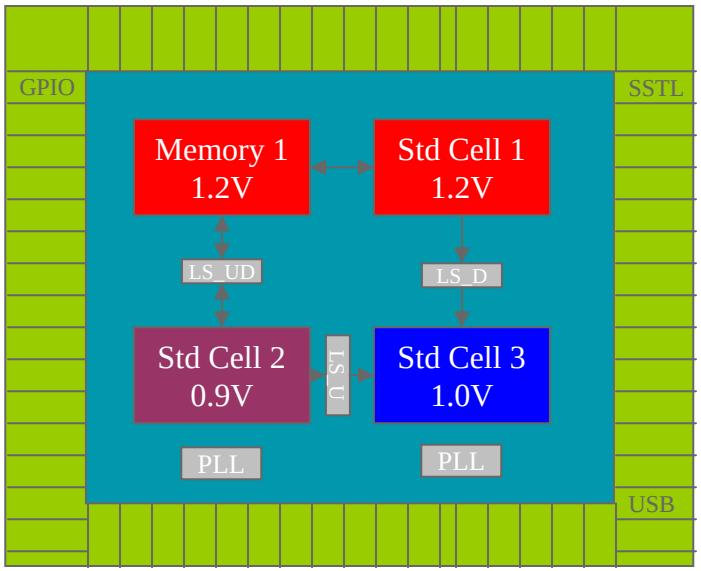
Entire core runs at same, low Vdd

Metro™ products enable this design style through:

- Characterization of all products at low operating voltages
- Architecture and circuit design techniques that minimize dynamic and static power
- Inclusion of Mixed Signal and Specialty IO blocks on-chip enable single chip solution

Vdd Reduction Approaches

Static Voltage Scaling



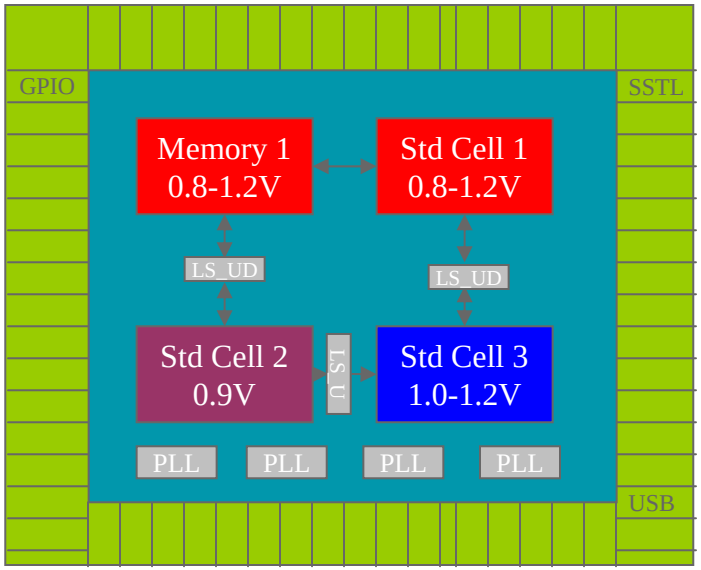
Different blocks in core run at different, but constant supply voltages.

Metro™ products enable this design style through:

- Characterization of all products at multiple operating voltages
- Voltage Level shifters to move signals between voltage domains
- Voltage regulators to isolate mixed signal IP on separate supply from digital blocks.

Vdd Reduction Approaches

Dynamic Voltage and Frequency Scaling

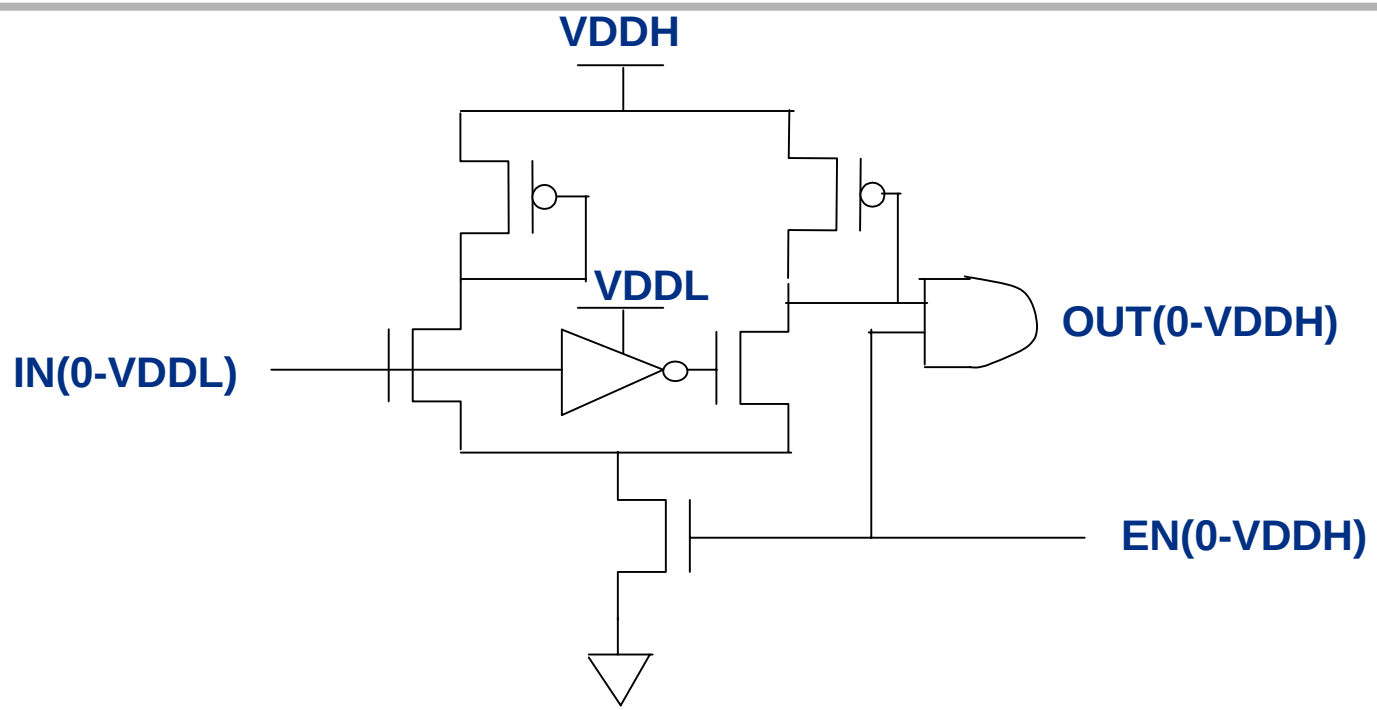


Different blocks in core run at variable and different supply voltages and frequencies

Metro™ products enable this design style through:

- Characterization of all products at multiple operating voltages
- Voltage Level shifters to move signals between voltage domains; clamps on output to enable stable operation if one block powered down completely.
- Voltage regulators to isolate mixed signal IP on separate supply from digital blocks.
- PLLs with fast lock time to enable fast transition to new clock frequency.

Example Low-High Level Shifter



- **High-Low level shifter is specially characterized standard cell (e.g. INV, AND2)**
- **Layout issues for LH level shifter**
  - May need two NWELLs if VDDL can exceed VDDH
  - VDDH needs to be a rail, but what about VDDL?
- **Placement issues for level shifters**
  - At block boundaries, enables from inside or outside

Conclusions

- **Silicon IP must be specifically designed for low power**
  - Both leakage and dynamic power important
- **Designers need choices**
  - Multi-VDD, IEM
  - MT-CMOS
  - Characterization points
- **Artisan's Metro platform is a comprehensive solution**