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# Interoperability Developer's Forum

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**ARM**

THE ARCHITECTURE FOR THE DIGITAL WORLD™

# IEM: What is it?

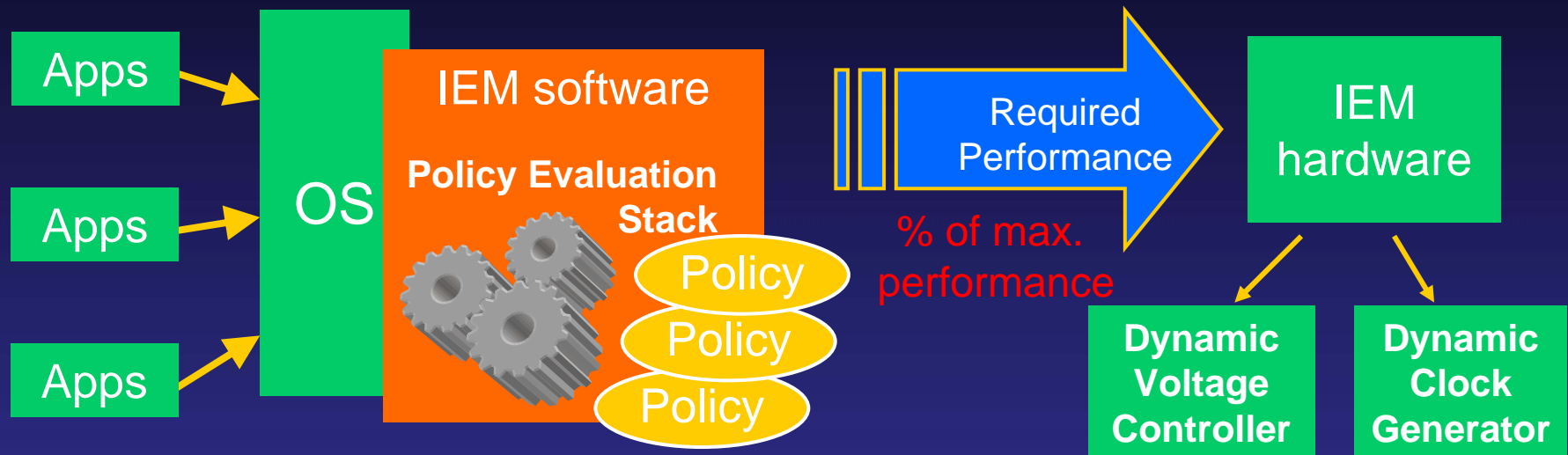
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- IEM is an exciting new technology that dynamically controls ARM processors and other on-chip components to run at their most energy efficient level whilst maintaining the user experience
- IEM extends battery life

- IEM builds on the functionality of conventional power management solutions by adding sophisticated control of performance scaling hardware to reduce both dynamic and static energy requirements.

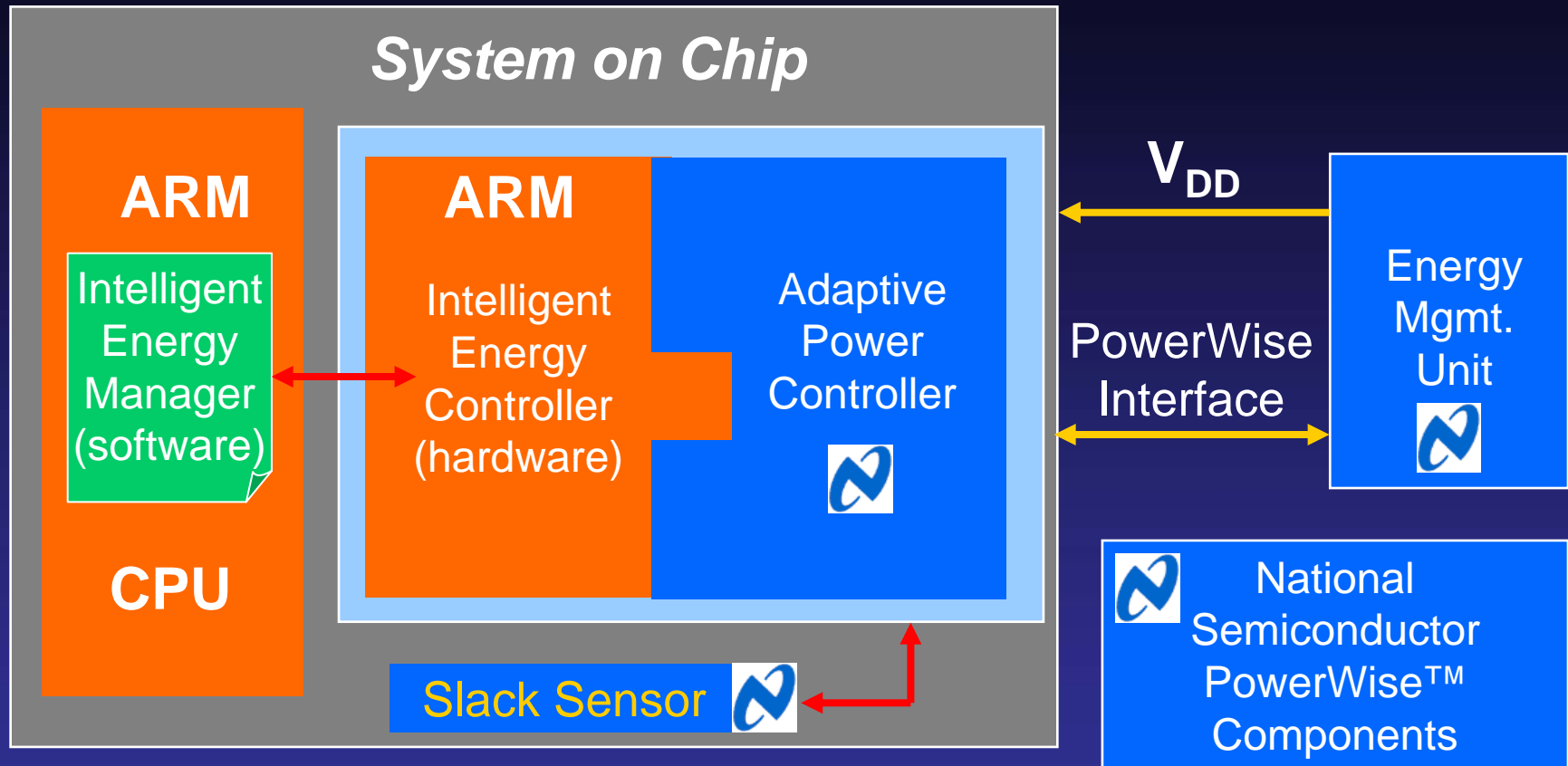
# IEM: Flow of Control

IEM technology controlling voltage & frequency (DVS)



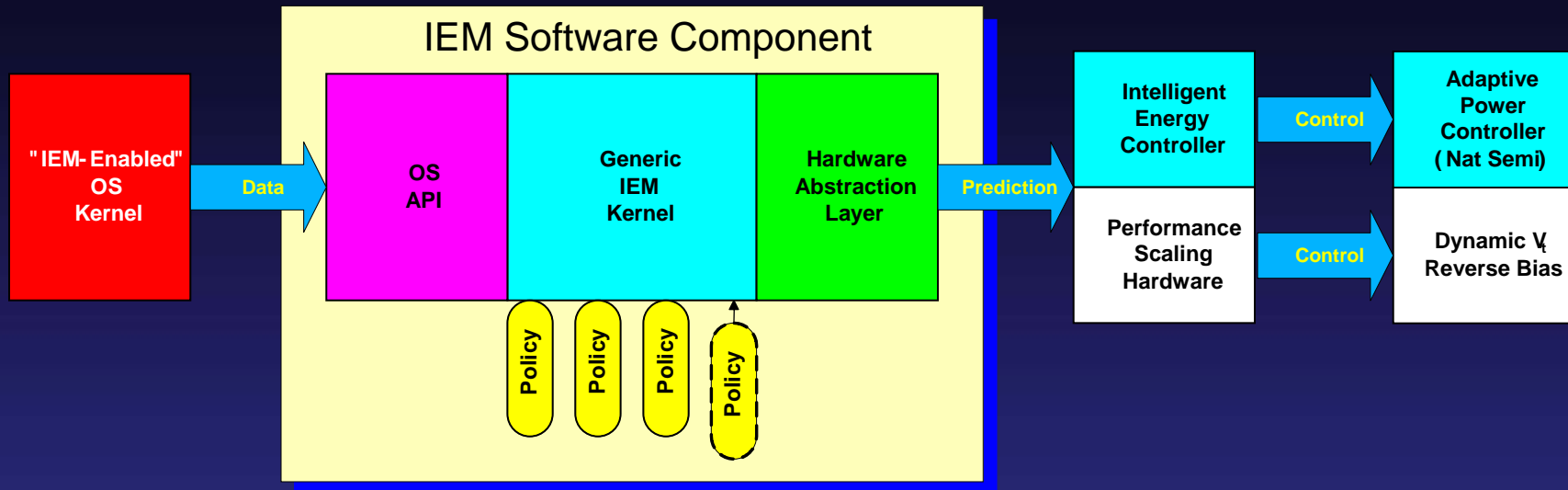
- IEM software component connects to OS kernel and collects data
- Multiple policies categorize the software workload
- Prediction of future performance requirement is made
- IEM hardware component manages SoC-specific hardware to achieve performance point (voltage and frequency combination)

# IEM: Closed Loop System



- National Semiconductor Adaptive Power Controller includes “Slack Sensor” to enable dynamic compensation for temperature and process variation

# IEM: Modular Software Architecture



- IEM interfaces to multiple OSes through OS API layer
- IEM supports existing ASICs using custom scaling hardware through software HAL
- IEM supports new SoC designs using ARM 'thin' HAL to connect directly to Intelligent Energy Controller (IEC)
- IEC can be used to control different process parameters

# IEM: Custom ASIC and multiple OSes

Microsoft  
Windows CE



**OR**

Symbian  
Operating  
System



**+**

Intelligent  
Energy  
Manager



Intel  
"Lubbock"  
platform



# Performance Monitor Requirements

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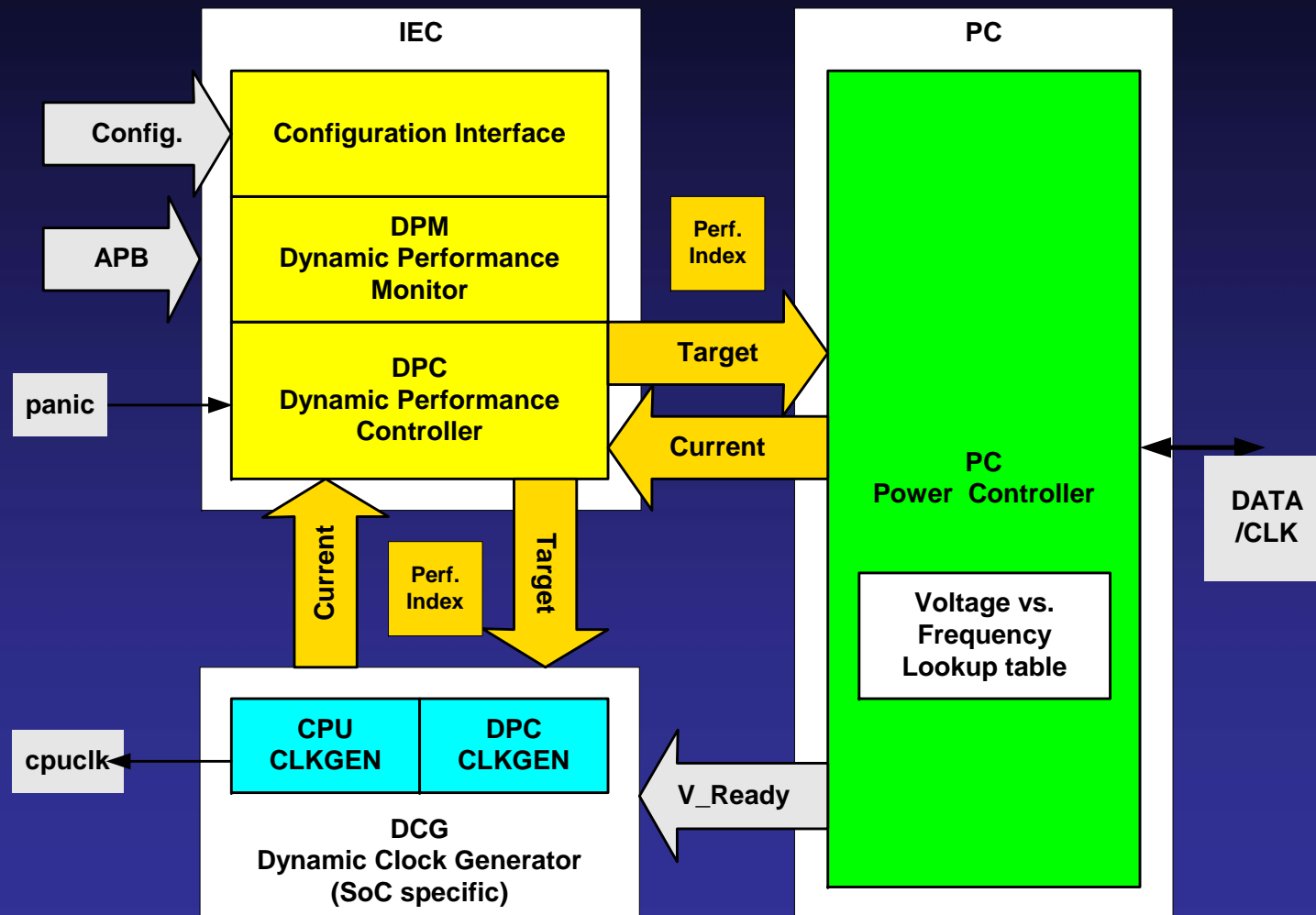
- In essence need to capture:
  - 'Real' time interval since task restarted
  - 'CPU' time reflecting work done in last interval
- Resolution needs to be order microseconds
  - Not OS centisecond/millisecond "clock" times
- CPU time measurement depends on:
  - Frequency switching times (PLL/divider dependent)
  - Voltage settling times (PSU dependent)
  - OS/Kernel overheads (hopefully fairly constant)
  - Not only the dynamic clock times but also depends on CPU <-> cache/memory access profile

# IEC - Modular HW Interfaces

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- The Intelligent Energy Controller provides:
  - Common register “API” interface to the OS
    - ‘Fractional’ Performance Setting (7-bit fractional)
      - Mapped in hardware to the SOC-specific set of discrete operating performance levels [configuration interface]
    - ‘Demand driven’ interface for frequency/voltage:
      - SOC-specific Dynamic Clock Generator
      - SOC/PSU-specific Dynamic Voltage Controller
      - ‘Max-Performance’ real-time/interrupt override
    - Dynamic performance monitoring support
      - Automatically accumulate CPU time (work done)
      - Allow efficient OS view on
    - Defined handshakes to DFS/DVS controllers
      - Ready for multi-processor systems

# IEC and Power Controller Integration



# IEM Technology and Interoperability

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IEM provides Dynamic Performance Scaling, *but...*

- IEM-enabled (CPU) cores require
  - Level-shifter interfaces, isolation clamps
    - Library IP, fast-settling PLLs
    - Extended characterization for cell libraries, memory
  - Power-aware RTL coding
    - Global power/ground in current HDLs inadequate
    - Careful hierarchical design for now
  - Latency-aware clock design
    - Clock tree balancing becomes dynamic challenge
    - Either asynchronous or complex clock generation
  - Comprehensive implementation and analysis EDA
    - Plus verification, test and production yield extensions

# Leakage Mitigation approaches

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1. Mixed Vt libraries
  - Reduce leakage on non-critical paths, no system issues  
**NO PROBLEM!**
2. Power-Switched domains
  - Clamp interfaces, long power ramp times, state save req.
3. Switched 'Virtual' Power Rails (MTCMOS etc)
  - Clamps, cell area and delay cost, state save/restore
4. Reverse Bias Power Switching
  - Area/power cost, superior leakage, VBB generation req.  
**STATE LOSS/RECOVERY + PSU DELAY!**
5. Retention Registers -
  - Area cost, extra power routing, fast re-start
6. Dynamic Threshold scaling (VtCMOS, ABB, etc)
  - Well/Bulk routing overheads, triple-well process, PSU++  
**STATE RETAINED, SOME PSU DELAY!**

# IEM – Interoperability Summary

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- Modular Approach to Energy management
  - Extensible/upgradeable SW policies
  - Operating-System portable policy stack
  - Co-exist with dynamic power management
    - Device driver and OS system sleep modes
  - IEC request/acknowledge interfaces to:
    - Dynamic Voltage Controllers (DVS, AVS etc.)
    - Dynamic Clock Generators (PLL, dividers, etc.)
    - Real-time overrides/interrupts
  - Extensible for Threshold Scaling...
    - Technology-independent leakage ‘hand-shakes’

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