

# IEEE P1800 SystemVerilog Group Overview & Update

*Synopsys Interoperability Developers' Forum*

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The SystemVerilog logo, featuring the text 'SystemVerilog' in a blue serif font, with a green and yellow swoosh underneath it.

SystemVerilog

# Agenda

- SystemVerilog P1800 Objectives
- Organization
- Progress
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- How can you participate?
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# P1800 Objectives

- Create a SystemVerilog IEEE Standard that is based on Accellera SystemVerilog 3.1a donation
  - Standard publication by October 2005
- Create a single Verilog HDL
  - IEEE, this summer, assigned P1364 Verilog PAR to P1800
  - Language alignment is addressed

# Organization

- Over 50 members on iee1800 reflector
- 11 active members both from Users' and EDA entities
- Appointed Officers:
  - Chair: Johny Srouji, Intel Corporation
  - Secretary: Dennis Brophy, Mentor Graphics
  - Official election process for chair, vice-chair and secretary was initiated

# Goals: The Big Picture

- Publish and Ballot SystemVerilog LRM
  - Draft by DAC 2005
- Publish and Ballot 1364 2005 LRM
  - Errata corrections
  - Consistency
  - Draft by end of 2005
- Publish a single LRM
  - Over the next 2-3 years

# Progress

- P1800 PAR was approved in June
  - Co-sponsored by DASC-SC and CAG
- Procedures & Policies were prepared, reviewed, approved and Ratified by sponsors
- Established contract with IEEE funded services to help in the LRM development, processes, and publication of the standard

## Progress (*cont*)

- A SystemVerilog Errata sub-group was formed to collect Errata and Propose solutions
  - Karen Pieper, of Synopsys, was elected to chair this sub-group
  - Accellera technical committees were moved under this sub-group
  - A group of language champions was identified
- Decisions on 1364:
  - Errata committee work continues
  - PTF (PLI) and P1800 sv-cc merged
  - Looking into alignment/merge of 1364 BTF (Behavioral)

# Schedule

DATE	Mile Stone	Comment
9/13/2004	Collection of Errata	submitted Errata after this date, will be captured in the Data Base but will not included in first draft
13-Sep-04	Formation of Balloting Pool	
1-Oct-04	IEEE Contract Closure	
1-Oct-04	Initial Draft Std.	SV3.1a in IEEE style
1-Feb-05	2 <sup>nd</sup> Draft Complete	Includes resolved Errata
15-Feb-05	Invitation to Ballot	
15-Mar-05	Closing on vote	
30-Mar-05	Formation of the Balloting Review Committee	
1-May-05	Ballot Resolution	
1-Jun-05	Complete Ballotable Draft	
2-Jun-05	Recirculation (as required)	
13-Jun-05	Close of Ballot	
30-Jul-05	Resolve Ballot Cmts, mod std, RevCom	Deadline is August 12. Next deadline is Oct 18
22-Sep-05	IEEE Standards Board Approval	Next deadline is Dec 6-7
15-Oct-05	Standard Publication	

# How can you participate

- IEEE meetings are open to the public
  - Everyone is welcome to attend meetings and voice their opinions
- Voting membership / balloting
  - By company, requires IEEE-SA membership
- Working Group:
  - Web site: <http://www.eda.org/sv-ieee1800/>
  - Chair: [johny.srouji@intel.com](mailto:johny.srouji@intel.com)
  - Secretary: [dennisb@model.com](mailto:dennisb@model.com)