

# 14th EDA Interoperability Developers' Forum: Interoperability Update

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## News

- New extensions to Liberty™ and SDC open source formats
- Additional updates in Liberty 2004.12
- Current versions of common formats
- Developments in Synopsys interoperability programs
- Tenzing Norgay award

## 2004.12 Liberty Enhancements

- CCS (Composite Current Source) modeling
  - Stayed tuned for more information after lunch
- Swing support for complex IO blocks
- Yield modeling support
- Frequency based max\_transition constraint

A stylized graphic of a puzzle piece with a circuit board pattern, positioned behind the URL text.

[www.synopsys.com/partners/tapin](http://www.synopsys.com/partners/tapin)

# Swing Support for Complex IO Blocks

- Feature
  - Liberty extended to support partial swings in special IO blocks like LVDS cells
  - One pair of extra attributes defined for the output and the input pins
  
- Attributes supported on output pins:
  - output\_signal\_level\_high
  - output\_signal\_level\_low
  
- Attributes supported on input pins:
  - input\_signal\_level\_high
  - input\_signal\_level\_low

## Yield Modeling Enhancement

- Imperfections in the fabrication process result in yield-reducing manufacturing defects
- Goal is to use yield enhancement techniques at the synthesis and design stage
- Synopsys Liberty syntax enhanced to consider the effect of failure\_rate constraint for synthesis
- Need to characterize the failure\_rate value for each cell



# Yield Modeling Syntax

```
library(library_namestring) {  
  ...  
  default_cell_failure_rate : <value>;  
  ...  
  cell(cell_namestring) {  
    ...  
    failure_rate : <value>;  
    ...  
  } /* cell */  
  ...  
} /* library */
```

- **Note: Failure Rate is ppb (parts per billion)**

# Frequency Based max\_transition Constraint

- Motivation
  - The max\_transition constraint is dependent on the operating frequency of the cell
- Features
  - The lookup table (LUT) will be one-dimensional where max\_transition is indexed by frequency.



# Frequency Based max\_transition Constraint

```
library(library_namestring) {  
  delay_model : table_lookup;  
  ...  
  maxtrans_lut_template(template_name1string) {  
    variable_1 : frequency;  
    index_1: ("float, float, ..., float");  
  }  
  cell(cell_name) {  
    ...  
    pin(pin_name) { /* input pin */  
      ...  
      max_trans(template_name1string) {  
        index_1: ("float, float, ..., float");  
        values("float, float...");  
      }  
      ...  
    } /* pin */  
  }  
}
```

## Download Current Versions

- Synopsys Open Source Formats:
  - [www.synopsys.com/partners/tapin](http://www.synopsys.com/partners/tapin)
  - Liberty™ V2004.06 (V2004.12 available Q1'2005)
  - SAIF 2.0
    - V2004.06 vcd2saif translator available
      - Improves capacity
  - SDC 1.4
  - OpenVera®: [www.open-vera.com](http://www.open-vera.com)
    - 1.3 Testbench & Assertions LRMs
    - 2.3 Testbench & Assertions LRMs

## Download Current Versions

- Milkyway™ Access Program (MAP-in):
  - MDE/C-API V2004.06

[www.synopsys.com/partners/mapin](http://www.synopsys.com/partners/mapin)

- Open SystemC™ Initiative:
  - V2.0.1 LRM
    - Donated to IEEE for standarization
  - V2.0.1 Reference Implementation
  - SystemC 2.1 library available for public review to licensees

[www.SystemC.org](http://www.SystemC.org)

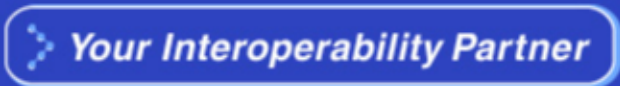


- Join Synopsys' SystemVerilog Catalyst Program
  - Advancing SystemVerilog-based tool and IP interoperability and availability
  - Open to: EDA vendors, Verification IP companies and Training services providers
  - Qualified access to Synopsys' SystemVerilog-based tools: VCS<sup>®</sup>, HDL Compiler<sup>™</sup>, LEDA<sup>®</sup>

[www.synopsys.com/partners/systemverilog](http://www.synopsys.com/partners/systemverilog)

- Visit Accellera's SystemVerilog web site
  - Download version 3.1a LRM and reference documents
  - Post your company's product information

[www.SystemVerilog.org](http://www.SystemVerilog.org)





# SystemVerilog Catalyst Program Members



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## 4<sup>th</sup> Annual Tenzing Norgay Interoperability Achievement Award

- Presented at DAC 2004 to an EDA company that
  - Surpasses common levels of interoperability
  - Contributes to overall industry advancement
  - Provides a new view of the future
  - Ensures customer success



*Tenzing Norgay  
atop Mt. Everest*

## Tenzing Norgay Award

### ■ Previous winners:

- CoWare (2001)
- Mentor Graphics (2002)
- Silicon Metrics (2003)

### ■ 2004 Nominees

- @HDL
- Artisan Components
- Atrenta
- Electronic Tools Company
- Library Technologies
- Novas Software
- Synchronicity
- Verific Design Automation



And the winner is...



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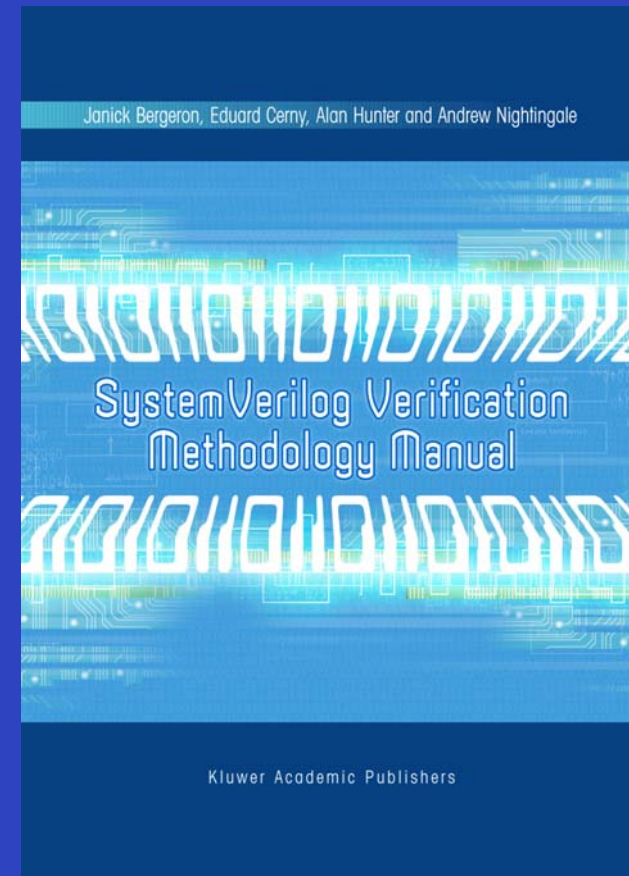
## 5<sup>th</sup> Tenzing Norgay Award



- Will be presented at DAC 2004 breakfast event
  - Wednesday, June 15, 2005
- Nominations are active for 3 years
- Call for nominations now until March 12<sup>th</sup>  
<http://www.synopsys.com/tapin/tnorgay>

## Win a VMM!

- Look for the “Free VMM” voucher to win a Verification Methodology Manual, authored by Synopsys and ARM
- Bring the voucher and completed order form to the registration table during the break
- Books available in Q1 2005




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# 15<sup>th</sup> EDA Interoperability Developers' Forum

- Thursday, April 7, 2005
- Located in Silicon Valley
- Invite your colleagues
- Want to speak?

See you then!

**Fill out your evaluations in the afternoon tracks to  
be eligible for today's prize drawings!**

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